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Micron Serial NOR Flash Memory

3V, Multiple I/O, 4KB, 32KB, 64KB Sector Erase

MT25QL02GCBB

Features

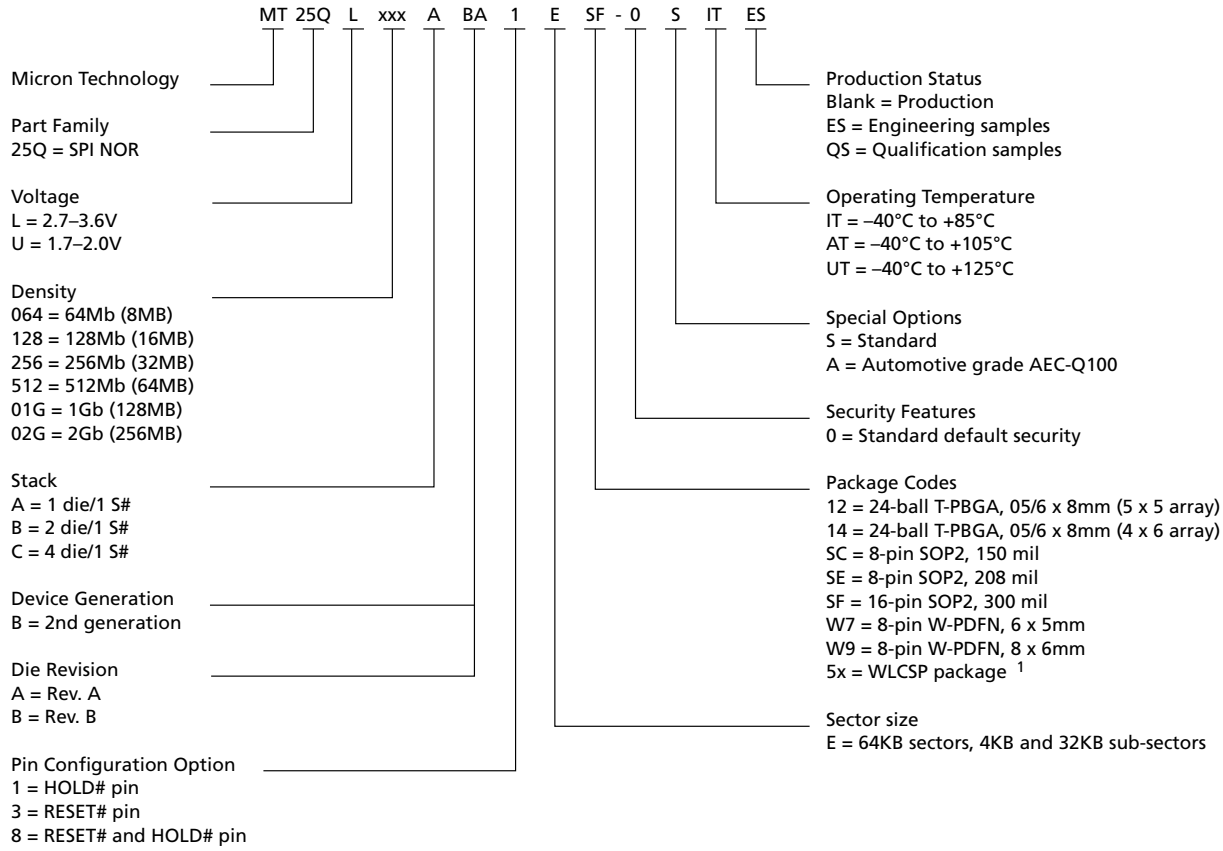
- Stacked device (four 512Mb die)
- SPI-compatible serial bus interface
- Single and double transfer rate (STR/DTR)
- Clock frequency
  - 133 MHz (MAX) for all protocols in STR
  - 90 MHz (MAX) for all protocols in DTR
- Dual/quad I/O commands for increased throughput up to 90 MB/s
- Supported protocols in both STR and DTR
  - Extended I/O protocol
  - Dual I/O protocol
  - Quad I/O protocol
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Additional reset pin for selected part numbers
- 3-byte and 4-byte address modes: enable memory access beyond 128Mb
- Dedicated 64-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with PROGRAM OTP command
- Erase capability
  - Die erase
  - Sector erase 64KB uniform granularity
  - Subsector erase 4KB, 32KB granularity
- Security and write protection
  - Volatile and nonvolatile locking and software write protection for each 64KB sector
  - Nonvolatile configuration locking
  - Password protection
  - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
  - Program/erase protection during power-up
  - CRC detects accidental changes to raw data
- Electronic signature
  - JEDEC-standard 3-byte signature (BA22h)
  - Extended device ID: two additional bytes identify device factory options
- JESD47H-compliant
  - Minimum 100,000 ERASE cycles per sector
  - Data retention: 20 years (TYP)

Options	Marking
• Voltage	
– 2.7–3.6V	L
• Density	
– 2Gb	02G
• Device stacking	
– 4 die stacked	C
• Device generation	B
• Die revision	B
• Pin configuration	
– RESET# and HOLD#	8
• Sector Size	
– 64KB	E
• Packages – JEDEC-standard, RoHS-compliant	
– 24-ball T-PBGA 05/6mm x 8mm (TBGA24)	12
• Standard security	0
• Special options	
– Standard	S
– Automotive	A
• Operating temperature range	
– From –40°C to +85°C	IT
– From –40°C to +105°C	AT

Part Number Ordering

Micron Serial NOR Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Ordering Information



Note: 1. WLCSP package codes, package size, and availability are density-specific. Contact the factory for availability.

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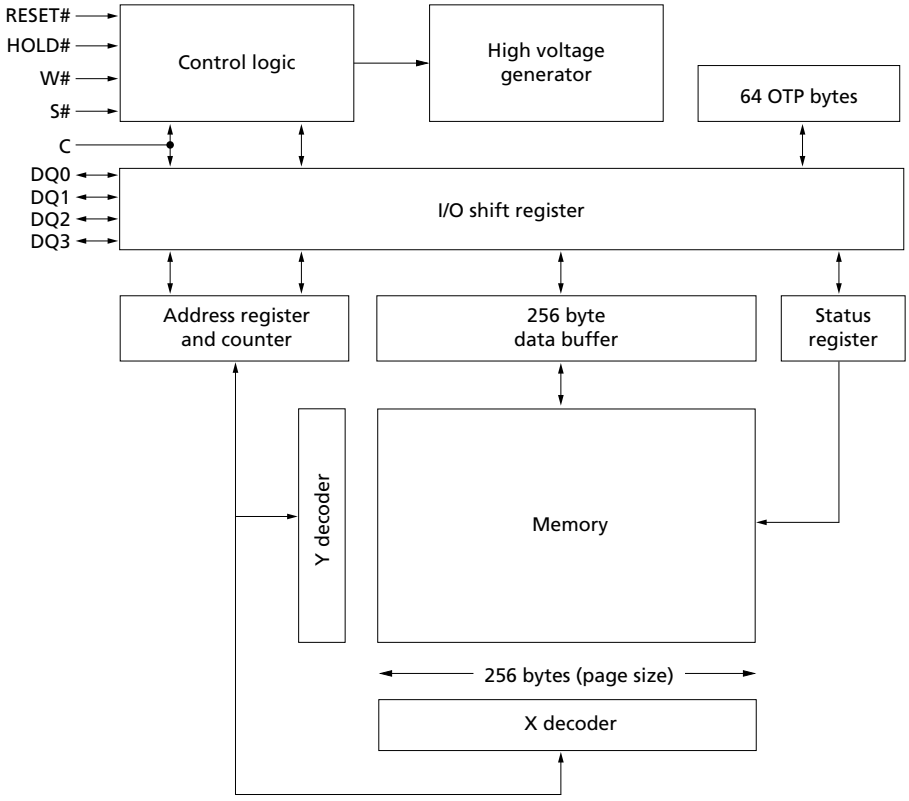
Device Description

The MT25Q is a high-performance multiple input/output serial Flash memory device. It features a high-speed SPI-compatible bus interface, execute-in-place (XIP) functionality, advanced write protection mechanisms, and extended address access. Innovative, high-performance, dual and quad input/output commands enable double or quadruple the transfer bandwidth for READ and PROGRAM operations.

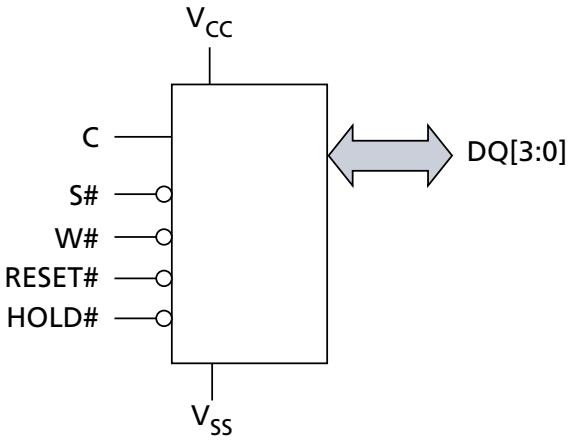
Figure 2: Block Diagram



Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

Device Logic Diagram

Figure 3: Logic Diagram



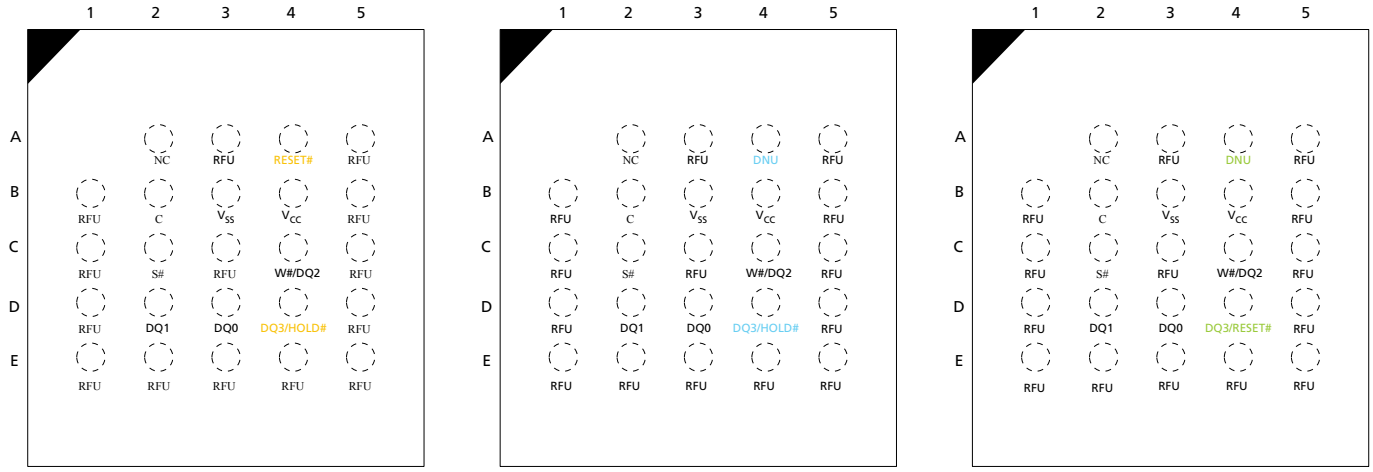
Notes:
1. Depending on the selected device (see Part Numbering Ordering Information), DQ3 = DQ3/RESET# or DQ3/HOLD#.
2. A separate RESET pin is available on dedicated part numbers (see Part Numbering Ordering Information).

Advanced Security Protection

The device offers an advanced security protection scheme where each sector can be independently locked, by either volatile or nonvolatile locking features. The nonvolatile locking configuration can also be locked, as well password-protected. See Block Protection Settings and Sector and Password Protection for more details.

Signal Assignments – Package Code: 12

Figure 4: 24-Ball T-BGA, 5 × 5 (Balls Down)



Notes:
1. RESET# or HOLD# signals can share Ball D4 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Ball A4 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Descriptions

The signal description table below is a comprehensive list of signals for the MT25Q family devices. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

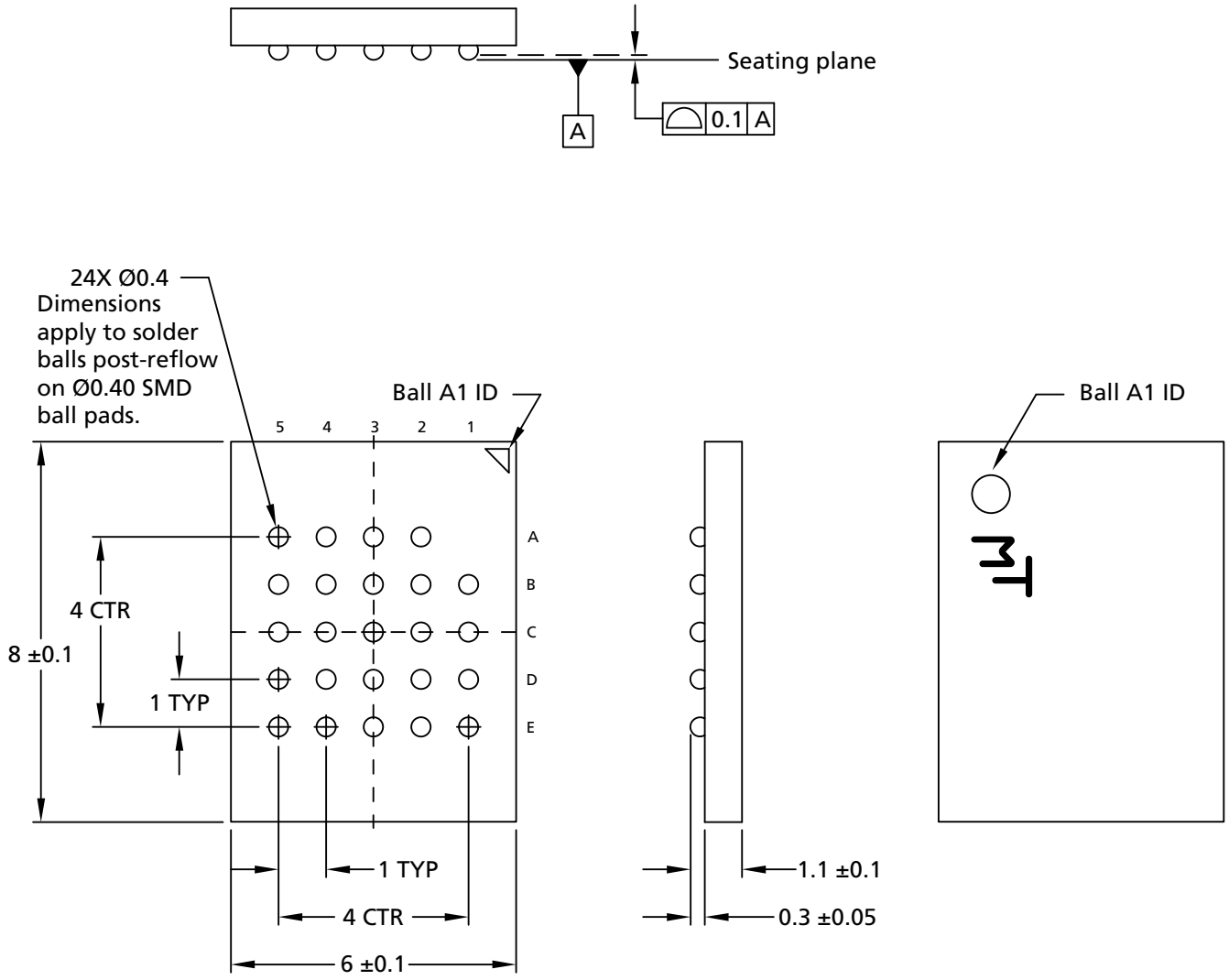
Symbol	Type	Description
S#	Input	**Chip select:** When S# is driven HIGH, the device will enter standby mode, unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress. All other input pins are ignored and the output pins are tri-stated. On parts with the pin configuration offering a dedicated RESET# pin, however, the RESET# input pin remains active even when S# is HIGH. Driving S# LOW enables the device, placing it in the active mode. After power-up, a falling edge on S# is required prior to the start of any command.
C	Input	**Clock:** Provides the timing of the serial interface. Command inputs are latched on the rising edge of the clock. In STR commands or protocol, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DTR commands or protocol, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
RESET#	Input	**RESET#:** When RESET# is driven LOW, the device is reset and the outputs are tri-stated. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost. The RESET# functionality can be disabled using bit 4 of the nonvolatile configuration register or bit 4 of the enhanced volatile configuration register. For pin configurations that share the DQ3 pin with RESET#, the RESET# functionality is disabled in QIO-SPI mode.
HOLD#	Input	**HOLD:** Pauses serial communications with the device without deselecting or resetting the device. Outputs are tri-stated and inputs are ignored. The HOLD# functionality can be disabled using bit 4 of the nonvolatile configuration register or bit 4 of the enhanced volatile configuration register. For pin configurations that share the DQ3 pin with HOLD#, the HOLD# functionality is disabled in QIO-SPI mode or when DTR operation is enabled.
W#	Input	**Write protect:** Freezes the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and the W# signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. During the extended-SPI protocol with QOFR and QIOFR instructions, and with QIO-SPI protocol, this pin function is an input/output as DQ2 functionality. This signal does not have internal pull-ups, it cannot be left floating and must be driven, even if none of W#/DQ2 function is used.
DQ[3:0]	I/O	**Serial I/O:** The bidirectional DQ signals transfer address, data, and command information. When using legacy (x1) SPI commands in extended I/O protocol (XIO-SPI), DQ0 is an input and DQ1 is an output. DQ[3:2] are not used. When using dual commands in XIO-SPI or when using DIO-SPI, DQ[1:0] are I/O. DQ[3:2] are not used. When using quad commands in XIO-SPI or when using QIO-SPI, DQ[3:0] are I/O.
V_{CC}	Supply	Core and I/O power supply.

Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
V_{SS}	Supply	Core and I/O ground connection.
DNU	–	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
RFU	–	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. Recommend that these be left floating. May be connected internally, but external connections will not affect operation.
NC	–	**No connect :** No internal connection; can be driven or floated.

Package Dimensions – Package Code: 12

Figure 5: 24-Ball T-PBGA (5 × 5 ball grid array) – 6mm × 8mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Memory Map – 2Gb Density

Table 2: Memory Map

Sector	Subsector (32KB)	Subsector (4KB)	Address Range	
			Start	End
4095	8191	65535	0FFF F000h	0FFF FFFFh
		⋮	⋮	⋮
		65528	0FFF 8000h	0FFF 8FFFh
	8190	65527	0FFF 7000h	0FFF 7FFFh
		⋮	⋮	⋮
		65520	0FFF 0000h	0FFF 0FFFh
⋮	⋮	⋮	⋮	⋮
2047	4095	32767	07FF F000h	07FF FFFFh
		⋮	⋮	⋮
		32760	07FF 8000h	07FF 8FFFh
	4094	32759	07FF 7000h	07FF 7FFFh
		⋮	⋮	⋮
		32752	07FF 0000h	07FF 0FFFh
⋮	⋮	⋮	⋮	⋮
1023	2047	16383	03FF F000h	03FF FFFFh
		⋮	⋮	⋮
		16376	03FF 8000h	03FF 8FFFh
	2046	16375	03FF 7000h	03FF 7FFFh
		⋮	⋮	⋮
		16368	03FF 0000h	03FF 0FFFh
⋮	⋮	⋮	⋮	⋮
0	1	15	0000 F000h	0000 FFFFh
		⋮	⋮	⋮
		8	0000 8000h	0000 8FFFh
	0	7	0000 7000h	0000 7FFFh
		⋮	⋮	⋮
		0	0000 0000h	0000 0FFFh

Note: 1. See Part Number Ordering Information, Sector Size – Part Numbers table for options.

Status Register

Status register bits can be read from or written to using READ STATUS REGISTER or WRITE STATUS REGISTER commands, respectively. When the status register enable/disable bit (bit 7) is set to 1 and W# is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. The only way to exit this hardware-protected mode is to drive W# HIGH.

Table 3: Status Register

Bit	Name	Settings	Description	Notes
7	Status register write enable/disable	0 = Enabled (Default) 1 = Disabled	**Nonvolatile control bit:** Used with W# to enable or disable writing to the status register.	
5	Top/bottom	0 = Top (Default) 1 = Bottom	**Nonvolatile control bit:** Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	
6, 4:2	BP[3:0]	See Protected Area tables	**Nonvolatile control bit:** Defines memory to be software protected against PROGRAM or ERASE operations. When one or more block protect bits is set to 1, a designated memory area is protected from PROGRAM and ERASE operations.	1
1	Write enable latch	0 = Clear (Default) 1 = Set	**Volatile control bit:** The device always powers up with this bit cleared to prevent inadvertent WRITE, PROGRAM, or ERASE operations. To enable these operations, the WRITE ENABLE operation must be executed first to set this bit.	
0	Write in progress	0 = Ready 1 = Busy	**Status bit:** Indicates if one of the following command cycles is in progress: WRITE STATUS REGISTER WRITE NONVOLATILE CONFIGURATION REGISTER PROGRAM ERASE	2

Notes:
1. The DIE ERASE command is executed only if all bits = 0.
2. Status register bit 0 is the inverse of flag status register bit 7.

Block Protection Settings

Table 4: Protected Area

Status Register Content					Protected Area (Sectors)	Unprotected Area (Sectors)
Top/Bottom	BP3	BP2	BP1	BP0		
0	0	1	0	0	4095:4088	4087:0
0	0	1	0	1	4095:4080	4079:0
0	0	1	1	0	4095:4064	4063:0
0	0	1	1	1	4095:4032	4031:0
0	1	0	0	0	4095:3968	3967:0
0	1	0	0	1	4095:3840	3839:0
0	1	0	1	0	4095:3584	3583:0
0	1	0	1	1	4095:3072	3071:0
0	1	1	0	0	4095:2048	2047:0
0	1	1	0	1	All	None
0	1	1	1	0	All	None
0	1	1	1	1	All	None
1	0	0	0	0	None	All
1	0	0	0	1	0	4095:1
1	0	0	1	0	1:0	4095:2
1	0	0	1	1	3:0	4095:4
1	0	1	0	0	7:0	4095:8
1	0	1	0	1	15:0	4095:16
1	0	1	1	0	31:0	4095:32
1	0	1	1	1	63:0	4095:32
1	1	0	0	0	127:0	4095:64
1	1	0	0	1	255:0	4095:256
1	1	0	1	0	511:0	4095:512
1	1	0	1	1	1023:0	4095:1024
1	1	1	0	0	2047:0	4095:2048
1	1	1	0	1	All	None
1	1	1	1	0	All	None
1	1	1	1	1	All	None

Flag Status Register

Flag status register bits are read by using READ FLAG STATUS REGISTER command. All bits are volatile and are reset to zero on power-up.

Status bits are set and reset automatically by the internal controller. Error bits must be cleared through the CLEAR STATUS REGISTER command.

Table 5: Flag Status Register

Bit	Name	Settings	Description
7	Program or erase controller	0 = Busy 1 = Ready	**Status bit:** Indicates whether one of the following command cycles is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE.
6	Erase suspend	0 = Clear 1 = Suspend	**Status bit:** Indicates whether an ERASE operation has been or is going to be suspended.
5	Erase	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE operation has succeeded or failed.
4	Program	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether a PROGRAM operation has succeeded or failed. It indicates, also, whether a CRC check has succeeded or failed.
3	Reserved	0	Reserved
2	Program suspend	0 = Clear 1 = Suspend	**Status bit:** Indicates whether a PROGRAM operation has been or is going to be suspended.
1	Protection	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.
0	Addressing	0 = 3-byte addressing 1 = 4-byte addressing	**Status bit:** Indicates whether 3-byte or 4-byte address mode is enabled.

Extended Address Register

The 3-byte address mode can only access 128Mb of memory. To access the full device in 3-byte address mode, the device includes an extended address register that indirectly provides a fourth address byte A[31:24]. The extended address register bits [3:0] operate as memory address bit A[27:24] to select one of the sixteen 128Mb segments of the memory array.

If 4-byte addressing is enabled, the extended address register settings are ignored.

Table 6: Extended Address Register

Bit	Name	Settings	Description
7:4	A[31:28]	0000	Reserved
3:0	A[27:24]	1111 = Highest 128Mb segment 1110 = 15th 128Mb segment 1101 = 14th 128Mb segment 1100 = 13th 128Mb segment 1011 = 12th 128Mb segment 1010 = 11th 128Mb segment 1001 = 10th 128Mb segment 1000 = 9th 128Mb segment 0111 = 8th 128Mb segment 0110 = 7th 128Mb segment 0101 = 6th 128Mb segment 0100 = 5th 128Mb segment 0011 = 4th 128Mb segment 0010 = 3rd 128Mb segment 0001 = 2nd 128Mb segment 0000 = Lowest 128Mb segment	Enables specified 128Mb memory segment. The default setting (lowest) can be changed to the highest 128Mb segment using bit 1 of the nonvolatile configuration register.

PROGRAM and ERASE operations act upon the 128Mb segment selected in the extended address register. The DIE ERASE operation erases the selected die.

The READ operation begins reading in the selected 128Mb segment, but is not bound by it.

In a continuous READ, when the last byte of the segment is read, the next byte output is the first byte of the next segment. The operation wraps to 0000000h; therefore, a download of the entire array is possible with one READ operation.

The value of the extended address register does not change when a READ operation crosses the selected 128Mb boundary.

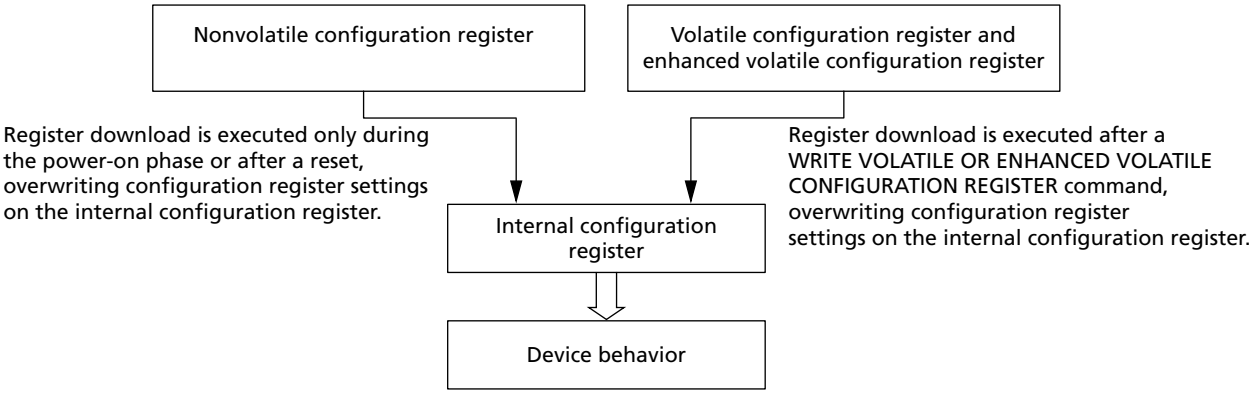
Internal Configuration Register

The memory configuration is set by an internal configuration register that is not directly accessible to users.

The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power-on or after a reset.

The user can change the configuration during operation by using the WRITE VOLATILE CONFIGURATION REGISTER or the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER commands. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.

Figure 6: Internal Configuration Register



Nonvolatile Configuration Register

This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. A register download is executed during power-on or after reset, overwriting the internal configuration register settings that determine device behavior.

Table 7: Nonvolatile Configuration Register

Bit	Name	Settings	Description	Notes
15:12	Number of dummy clock cycles	0000 = Identical to 1111 0001 = 1 0010 = 2 ⋮ 1101 = 13 1110 = 14 1111 = Default	Sets the number of dummy clock cycles subsequent to all FAST READ commands. (See the Command Set Table for default setting values.)	1
11:9	XIP mode at power-on reset	000 = XIP: Fast read 001 = XIP: Dual output fast read 010 = XIP: Dual I/O fast read 011 = XIP: Quad output fast read 100 = XIP: Quad I/O fast read 101 = Reserved 110 = Reserved 111 = Disabled (Default)	Enables the device to operate in the selected XIP mode immediately after power-on reset.	
8:6	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = Reserved 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = Reserved 111 = 30 Ohms (Default)	Optimizes the impedance at $V_{CC}/2$ output voltage.	
5	Double transfer rate protocol	0 = Enabled 1 = Disabled (Default)	Set DTR protocol as current one. Once enabled, all commands will work in DTR.	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables HOLD# or RESET# on DQ3.	
3	Quad I/O protocol	0 = Enabled 1 = Disabled (Default)	Enables or disables quad I/O command input (4-4-4 mode).	2
2	Dual I/O protocol	0 = Enabled 1 = Disabled (Default)	Enables or disables dual I/O command input (2-2-2 mode).	2
1	128Mb segment select	0 = Highest 128Mb segment 1 = Lowest 128Mb segment (Default)	Selects the power-on default 128Mb segment for 3-byte address operations. See also the extended address register.	

Table 7: Nonvolatile Configuration Register (Continued)

Bit	Name	Settings	Description	Notes
0	Number of address bytes during command entry	0 = Enable 4-byte address mode 1 = Enable 3-byte address mode (Default)	Defines the number of address bytes for a command.	

Notes:
1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ command (See Supported Clock Frequencies table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data.
2. When bits 2 and 3 are both set to 0, the device operates in quad I/O protocol.

Volatile Configuration Register

This register is read from and written to by the READ VOLATILE CONFIGURATION REGISTER and the WRITE VOLATILE CONFIGURATION REGISTER commands, respectively. A register download is executed after these commands, overwriting the internal configuration register settings that determine device memory behavior.

Table 8: Volatile Configuration Register

Bit	Name	Settings	Description	Notes
7:4	Number of dummy clock cycles	0000 = Identical to 1111 0001 = 1 0010 = 2 ⋮ 1101 = 13 1110 = 14 1111 = Default	Sets the number of dummy clock cycles subsequent to all FAST READ commands. (See the Command Set Table for default setting values.)	1
3	XIP	0 = Enable 1 = Disable (Default)	Enables or disables XIP.	
2	Reserved	0	0b = Fixed value.	
1:0	Wrap	00 = 16-byte boundary aligned	16-byte wrap: Output data wraps within an aligned 16-byte boundary starting from the 3-byte address issued after the command code.	2
		01 = 32-byte boundary aligned	32-byte wrap: Output data wraps within an aligned 32-byte boundary starting from the 3-byte address issued after the command code.	
		10 = 64-byte boundary aligned	64-byte wrap: Output data wraps within an aligned 64-byte boundary starting from the 3-byte address issued after the command code.	
		11 = Continuous (Default)	Continuously sequences addresses through the entire array.	

Notes:
1. The number of cycles must be set according to and sufficient for the clock frequency, which varies by the type of FAST READ command, as shown in the Supported Clock Frequencies table. An insufficient number of dummy clock cycles for the operating frequency causes the memory to read incorrect data.
2. See the Sequence of Bytes During Wrap table.

Table 9: Sequence of Bytes During Wrap

Starting Address	16-Byte Wrap	32-Byte Wrap	64-Byte Wrap
0	0-1-2- . . . -15-0-1- . .	0-1-2- . . . -31-0-1- . .	0-1-2- . . . -63-0-1- . .
1	1-2- . . . -15-0-1-2- . .	1-2- . . . -31-0-1-2- . .	1-2- . . . -63-0-1-2- . .
....	....	....	....
15	15-0-1-2-3- . . . -15-0-1- . .	15-16-17- . . . -31-0-1- . .	15-16-17- . . . -63-0-1- . .
....	....	....	....
31	-	31-0-1-2-3- . . . -31-0-1- . .	31-32-33- . . . -63-0-1- . .
....	....	....	....
63	-	-	63-0-1- . . . -63-0-1- . .

Supported Clock Frequencies

Table 10: Clock Frequencies – STR (in MHz) for IT parts

Notes apply to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	94	79	60	44	39
2	112	97	77	61	48
3	129	106	86	78	58
4	133	115	97	97	69
5	133	125	106	106	78
6	133	133	115	115	86
7	133	133	125	125	97
8	133	133	133	133	106
9	133	133	133	133	115
10	133	133	133	133	125
11 : 14	133	133	133	133	133

Notes:
1. Values are guaranteed by characterization and not 100% tested in production.
2. A tuning data pattern (TDP) capability provides applications with data patterns for adjusting the data latching point at the host end when the clock frequency is set higher than 133 MHz in STR mode and higher than 66 MHz in double transfer rate (DTR) mode. For additional details, refer to TN-25-07: Tuning Data Pattern for MT25Q and MT25T Devices.

Table 11: Clock Frequencies – STR (in MHz) for AT parts

Notes apply to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	94	79	60	44	39
2	112	97	77	61	48
3	129	106	86	78	58
4	133	115	97	97	69
5	133	125	106	106	78
6	133	133	115	108	86
7	133	133	125	108	97
8	133	133	133	108	106
9-14	133	133	133	108	108

Notes:
1. Values are guaranteed by characterization and not 100% tested in production.
2. A tuning data pattern (TDP) capability provides applications with data patterns for adjusting the data latching point at the host end when the clock frequency is set higher than 133 MHz in STR mode and higher than 66 MHz in double transfer rate (DTR) mode.

For additional details, refer to TN-25-07: Tuning Data Pattern for MT25Q and MT25T Devices.

Table 12: Clock Frequencies – DTR (in MHz) for IT parts

Notes apply to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	59	45	40	26	20
2	73	59	49	40	30
3	82	68	59	59	39
4	90	76	65	65	49
5	90	83	75	75	58
6	90	90	83	83	68
7	90	90	90	90	78
8	90	90	90	90	85
9	90	90	90	90	90
10 : 14	90	90	90	90	90

Notes:
1. Values are guaranteed by characterization and not 100% tested in production.
2. A tuning data pattern (TDP) capability provides applications with data patterns for adjusting the data latching point at the host end when the clock frequency is set higher than 133 MHz in STR mode and higher than 66 MHz in double transfer rate (DTR) mode. For additional details, refer to TN-25-07: Tuning Data Pattern for MT25Q and MT25T Devices.

Table 13: Clock Frequencies – DTR (in MHz) for AT parts

Notes apply to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	59	45	40	26	20
2	73	59	49	40	30
3	82	68	59	59	39
4	90	76	65	65	49
5	90	83	75	75	58
6	90	90	83	80	68
7	90	90	90	80	78
8-14	90	90	90	80	80

Notes:
1. Values are guaranteed by characterization and not 100% tested in production.
2. A tuning data pattern (TDP) capability provides applications with data patterns for adjusting the data latching point at the host end when the clock frequency is set higher than 133 MHz in STR mode and higher than 66 MHz in double transfer rate (DTR) mode.