



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





Micron Serial NOR Flash Memory

3V, Multiple I/O, 4KB, 32KB, 64KB, Sector Erase

MT25QL128ABA

Features

- SPI-compatible serial bus interface
- Single and double transfer rate (STR/DTR)
- Clock frequency
 - 133 MHz (MAX) for all protocols in STR
 - 90 MHz (MAX) for all protocols in DTR
- Dual/quad I/O commands for increased throughput up to 90 MB/s
- Supported protocols in both STR and DTR
 - Extended I/O protocol
 - Dual I/O protocol
 - Quad I/O protocol
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Additional reset pin for selected part numbers
- Dedicated 64-byte OTP area outside main memory
 - Readable and user-lockable
 - Permanent lock with PROGRAM OTP command
- Erase capability
 - Bulk erase
 - Sector erase 64KB uniform granularity
 - Subsector erase 4KB, 32KB granularity
- Security and write protection
 - Volatile and nonvolatile locking and software write protection for each 64KB sector
 - Nonvolatile configuration locking
 - Password protection
 - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
 - Program/erase protection during power-up
 - CRC detects accidental changes to raw data
- Electronic signature
 - JEDEC-standard 3-byte signature (BA18h)
 - Extended device ID: two additional bytes identify device factory options
- JESD47H-compliant
 - Minimum 100,000 ERASE cycles per sector
 - Data retention: 20 years (TYP)

Options

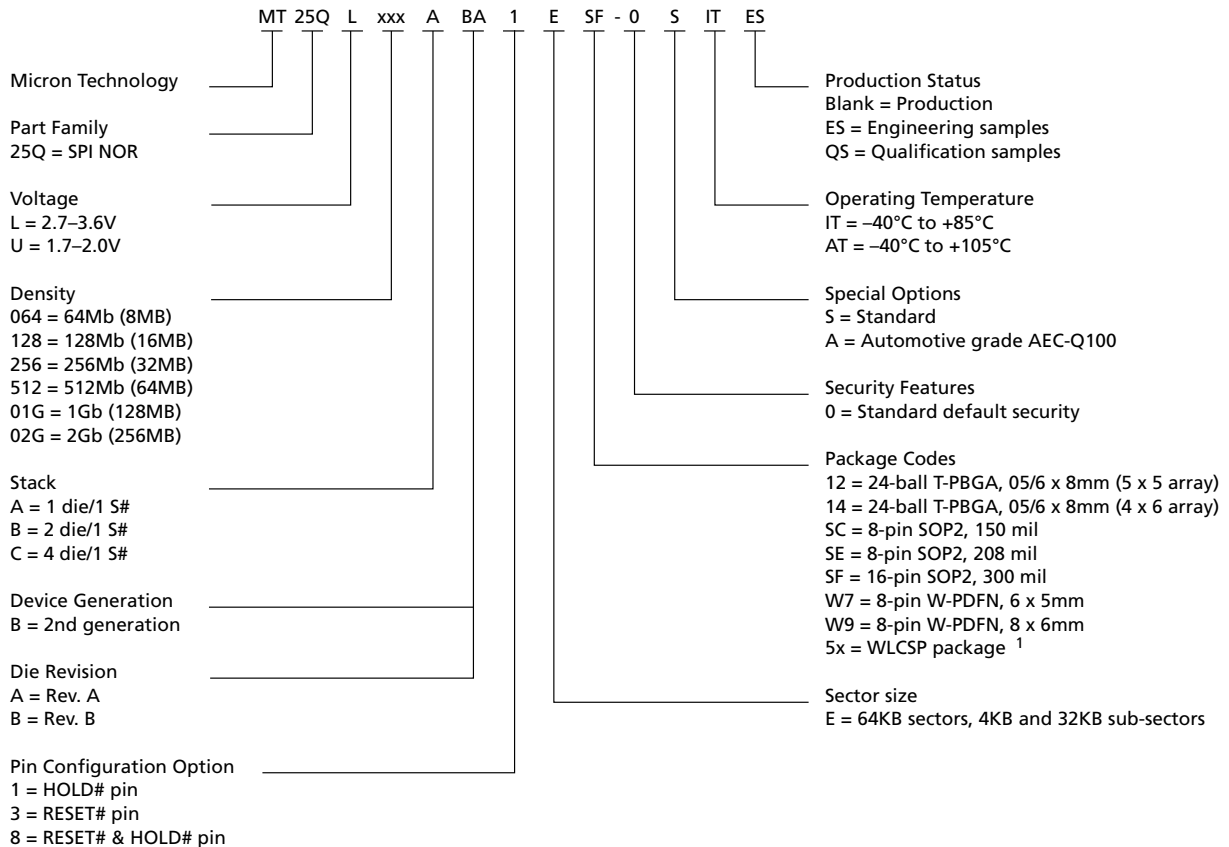
- Voltage
 - 2.7–3.6V
- Density
 - 128Mb
- Device stacking
 - Monolithic
- Device generation
 - A
- Die revision
 - B
- Pin configuration
 - RESET# and HOLD#
- Sector Size
 - 64KB
- Packages – JEDEC-standard, RoHS-compliant
 - 16-pin SOP2, 300 mils body width (SO16W) SF
 - 8-pin SOP2, 208 mils body width (SO8W) SE
 - 24-ball T-PBGA, 05/6mm x 8mm (TBGA24) 12
 - 24-ball T-PBGA 05/6mm x 8mm (4 x 6 array) 14
 - W-PDFN-8 8mm x 6mm (MLP8 8mm x 6mm) W9
 - W-PDFN-8 6mm x 5mm (MLP8 6mm x 5mm) W7
- Standard security
 - 0
- Special options
 - Standard S
 - Automotive A
- Operating temperature range
 - From –40°C to +85°C IT
 - From –40°C to +105°C AT

Marking

Part Number Ordering

Micron Serial NOR Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron’s part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Ordering Information



Note: 1. WLCSP package codes, package size, and availability are density-specific. Contact the factory for availability.



Contents

Device Description	8
Device Logic Diagram	9
Advanced Security Protection	9
Signal Assignments – Package Code: 12	10
Signal Assignments – Package Code: SE, W7, W9	10
Signal Assignments – Package Code: SF	11
Signal Descriptions	12
Package Dimensions – Package Code: 12	13
Package Dimensions – Package Code: SE	14
Package Dimensions – Package Code: SF	15
Package Dimensions – Package Code: W7	16
Package Dimensions – Package Code: W9	17
Memory Map – 128Mb Density	18
Status Register	19
Block Protection Settings	20
Flag Status Register	21
Internal Configuration Register	22
Nonvolatile Configuration Register	23
Volatile Configuration Register	24
Supported Clock Frequencies	25
Enhanced Volatile Configuration Register	27
Security Registers	28
Sector Protection Security Register	29
Nonvolatile and Volatile Sector Lock Bits Security	30
Volatile Lock Bit Security Register	30
Device ID Data	31
Serial Flash Discovery Parameter Data	32
Command Definitions	33
Software RESET Operations	38
RESET ENABLE and RESET MEMORY Commands	38
READ ID Operations	39
READ ID and MULTIPLE I/O READ ID Commands	39
READ SERIAL FLASH DISCOVERY PARAMETER Operation	40
READ SERIAL FLASH DISCOVERY PARAMETER Command	40
READ MEMORY Operations	41
READ MEMORY Operations Timings	41
WRITE ENABLE/DISABLE Operations	48
READ REGISTER Operations	49
WRITE REGISTER Operations	50
CLEAR FLAG STATUS REGISTER Operation	52
PROGRAM Operations	53
PROGRAM Operations Timings	54
ERASE Operations	57
SUSPEND/RESUME Operations	59
PROGRAM/ERASE SUSPEND Operations	59
PROGRAM/ERASE RESUME Operations	59
ONE-TIME PROGRAMMABLE Operations	61
READ OTP ARRAY Command	61
PROGRAM OTP ARRAY Command	61
QUAD PROTOCOL Operations	62



128Mb, 3V Multiple I/O Serial Flash Memory Features

ENTER or RESET QUAD INPUT/OUTPUT MODE Command	62
CYCLIC REDUNDANCY CHECK Operations	64
State Table	66
XIP Mode	67
Activate or Terminate XIP Using Volatile Configuration Register	67
Activate or Terminate XIP Using Nonvolatile Configuration Register	67
Confirmation Bit Settings Required to Activate or Terminate XIP	68
Terminating XIP After a Controller and Memory Reset	68
Power-Up and Power-Down	69
Power-Up and Power-Down Requirements	69
Power Loss and Interface Rescue	71
Recovery	71
Power Loss Recovery	71
Interface Rescue	71
Initial Delivery Status	72
Absolute Ratings and Operating Conditions	73
DC Characteristics and Operating Conditions	75
AC Characteristics and Operating Conditions	77
AC Reset Specifications	79
Program/Erase Specifications	82
Revision History	83
Rev. I - 09/16	83
Rev. H - 07/16	83
Rev. G - 06/16	83
Rev. F - 12/15	83
Rev. E - 10/15	83
Rev. D - 9/15	83
Rev. C - 7/15	83
Rev. B - 7/14	84
Rev. A - 01/14	84

List of Figures

Figure 1: Part Number Ordering Information	2
Figure 2: Block Diagram	8
Figure 3: Logic Diagram	9
Figure 4: 24-Ball T-BGA, 5 x 5 (Balls Down)	10
Figure 5: 8-Pin, SOP2 or W-PDFN (Top View)	10
Figure 6: 16-Pin, Plastic Small Outline – SO16 (Top View)	11
Figure 7: 24-Ball T-PBGA (5 x 5 ball grid array) – 6mm x 8mm	13
Figure 8: 8-Pin SOP2 (SO8W) – 208 Mils Body Width	14
Figure 9: 16-Pin SOP2 – 300 mils Body Width	15
Figure 10: W-PDFN-8 (MLP8) – 6mm x 5mm	16
Figure 11: W-PDFN-8 (MLP8) – 8mm x 6mm	17
Figure 12: Internal Configuration Register	22
Figure 13: Sector and Password Protection	28
Figure 14: RESET ENABLE and RESET MEMORY Command	38
Figure 15: READ ID and MULTIPLE I/O READ ID Commands	39
Figure 16: READ SERIAL FLASH DISCOVERY PARAMETER Command – 5Ah	40
Figure 17: READ – 03h	41
Figure 18: FAST READ – 0Bh	42
Figure 19: DUAL OUTPUT FAST READ – 3Bh	42
Figure 20: DUAL INPUT/OUTPUT FAST READ – BBh	43
Figure 21: QUAD OUTPUT FAST READ – 6Bh	43
Figure 22: QUAD INPUT/OUTPUT FAST READ – EBh	44
Figure 23: QUAD INPUT/OUTPUT WORD READ – E7h	44
Figure 24: DTR FAST READ – 0Dh	45
Figure 25: DTR DUAL OUTPUT FAST READ – 3Dh	45
Figure 26: DTR DUAL INPUT/OUTPUT FAST READ – BDh	46
Figure 27: DTR QUAD OUTPUT FAST READ – 6Dh	46
Figure 28: DTR QUAD INPUT/OUTPUT FAST READ – EDh	47
Figure 29: WRITE ENABLE and WRITE DISABLE Timing	48
Figure 30: READ REGISTER Timing	49
Figure 31: WRITE REGISTER Timing	51
Figure 32: CLEAR FLAG STATUS REGISTER Timing	52
Figure 33: PAGE PROGRAM Command	54
Figure 34: DUAL INPUT FAST PROGRAM Command	55
Figure 35: EXTENDED DUAL INPUT FAST PROGRAM Command	55
Figure 36: QUAD INPUT FAST PROGRAM Command	56
Figure 37: EXTENDED QUAD INPUT FAST PROGRAM Command	56
Figure 38: SUBSECTOR and SECTOR ERASE Timing	58
Figure 39: BULK ERASE Timing	58
Figure 40: PROGRAM/ERASE SUSPEND or RESUME Timing	60
Figure 41: READ OTP Command	61
Figure 42: PROGRAM OTP Command	62
Figure 43: XIP Mode Directly After Power-On	67
Figure 44: Power-Up Timing	70
Figure 45: AC Timing Input/Output Reference Levels	74
Figure 46: Reset AC Timing During PROGRAM or ERASE Cycle	80
Figure 47: Reset Enable and Reset Memory Timing	80
Figure 48: Serial Input Timing	80
Figure 49: Write Protect Setup and Hold During WRITE STATUS REGISTER Operation (SRWD = 1)	81
Figure 50: Hold Timing	81



Figure 51: Output Timing 81

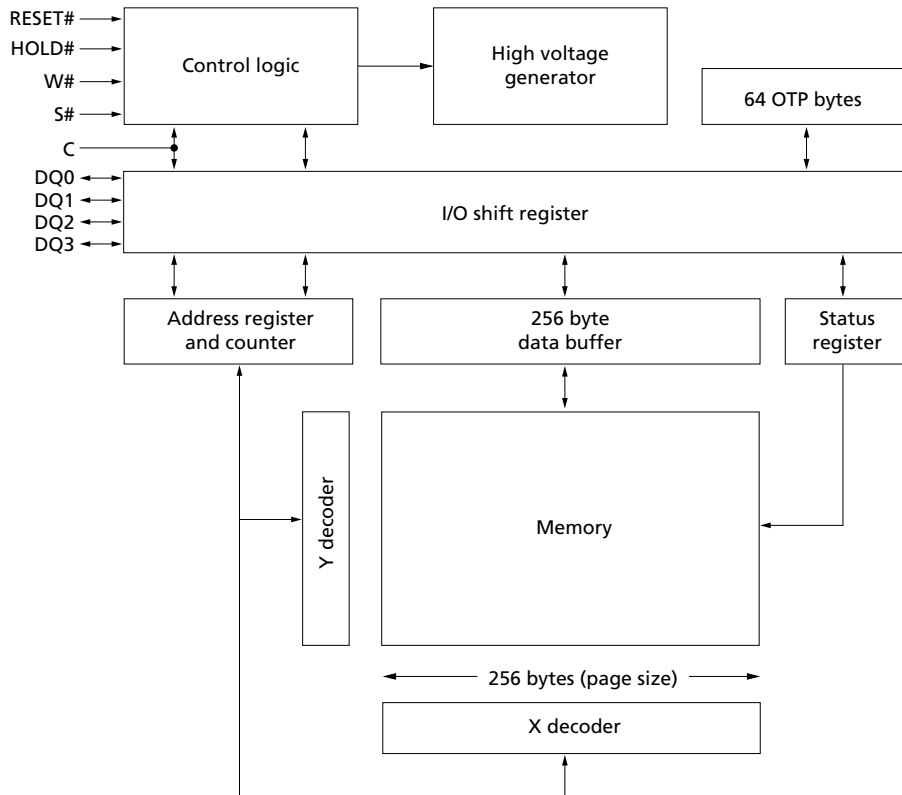
List of Tables

Table 1: Signal Descriptions	12
Table 2: Memory Map	18
Table 3: Status Register	19
Table 4: Protected Area	20
Table 5: Flag Status Register	21
Table 6: Nonvolatile Configuration Register	23
Table 7: Volatile Configuration Register	24
Table 8: Sequence of Bytes During Wrap	24
Table 9: Clock Frequencies – STR (in MHz)	25
Table 10: Clock Frequencies – DTR (in MHz)	26
Table 11: Enhanced Volatile Configuration Register	27
Table 12: Sector Protection Register	29
Table 13: Global Freeze Bit	29
Table 14: Nonvolatile and Volatile Lock Bits	30
Table 15: Volatile Lock Bit Register	30
Table 16: Device ID Data	31
Table 17: Extended Device ID Data, First Byte	31
Table 18: Command Set	33
Table 19: RESET ENABLE and RESET MEMORY Operations	38
Table 20: READ ID and MULTIPLE I/O READ ID Operations	39
Table 21: READ MEMORY Operations	41
Table 22: WRITE ENABLE/DISABLE Operations	48
Table 23: READ REGISTER Operations	49
Table 24: WRITE REGISTER Operations	50
Table 25: CLEAR FLAG STATUS REGISTER Operation	52
Table 26: PROGRAM Operations	53
Table 27: ERASE Operations	57
Table 28: SUSPEND/RESUME Operations	59
Table 29: OTP Control Byte (Byte 64)	62
Table 30: ENTER and RESET QUAD PROTOCOL Operations	63
Table 31: CRC Command Sequence on Entire Device	64
Table 32: CRC Command Sequence on a Range	65
Table 33: Operations Allowed/Disallowed During Device States	66
Table 34: XIP Confirmation Bit	68
Table 35: Effects of Running XIP in Different Protocols	68
Table 36: Power-Up Timing and V_{WI} Threshold	70
Table 37: Absolute Ratings	73
Table 38: Operating Conditions	73
Table 39: Input/Output Capacitance	73
Table 40: AC Timing Input/Output Conditions	74
Table 41: DC Current Characteristics and Operating Conditions	75
Table 42: DC Voltage Characteristics and Operating Conditions	75
Table 43: AC Characteristics and Operating Conditions	77
Table 44: AC RESET Conditions	79
Table 45: Program/Erase Specifications	82

Device Description

The MT25Q is a high-performance multiple input/output serial Flash memory device. It features a high-speed SPI-compatible bus interface, execute-in-place (XIP) functionality, advanced write protection mechanisms, and extended address access. Innovative, high-performance, dual and quad input/output commands enable double or quadruple the transfer bandwidth for READ and PROGRAM operations.

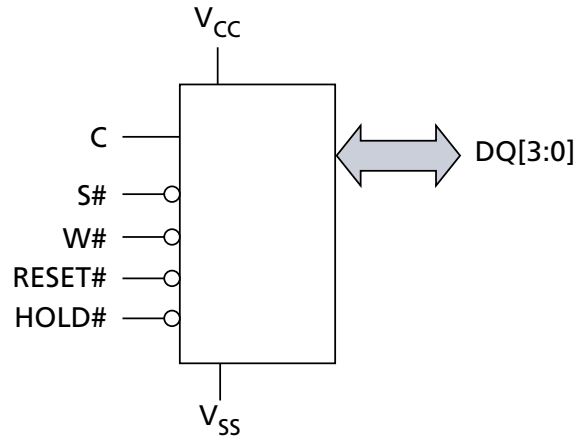
Figure 2: Block Diagram



Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

Device Logic Diagram

Figure 3: Logic Diagram



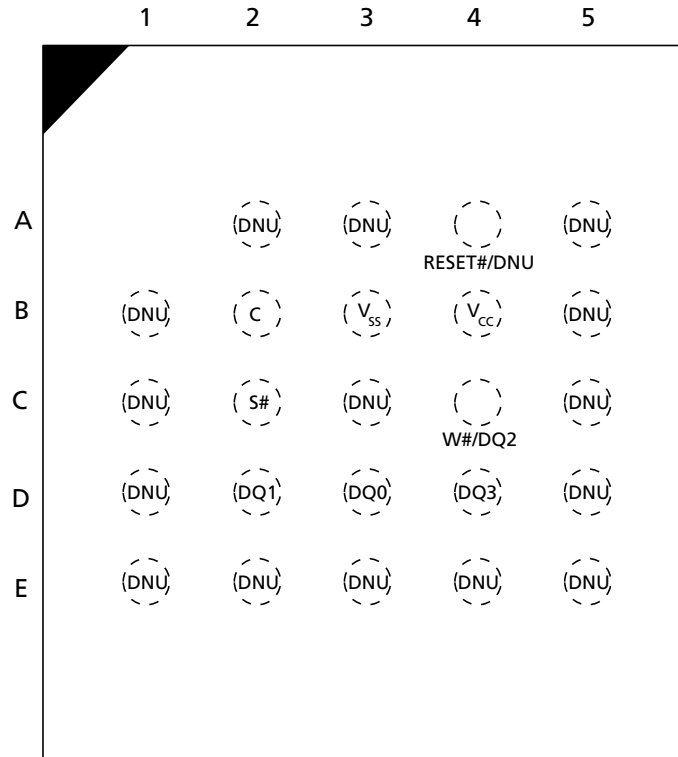
- Notes:
1. Depending on the selected device (see Part Numbering Ordering Information), $DQ3 = DQ3/RESET\#$ or $DQ3/HOLD\#$.
 2. A separate $RESET$ pin is available on dedicated part numbers (see Part Numbering Ordering Information).

Advanced Security Protection

The device offers an advanced security protection scheme where each sector can be independently locked, by either volatile or nonvolatile locking features. The nonvolatile locking configuration can also be locked, as well password-protected. See Block Protection Settings and Sector and Password Protection for more details.

Signal Assignments – Package Code: 12

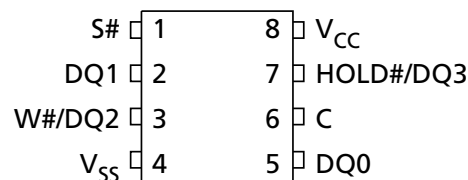
Figure 4: 24-Ball T-BGA, 5 x 5 (Balls Down)



- Notes:
1. RESET# or HOLD# signals can share Ball D4 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
 2. Ball A4 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Assignments – Package Code: SE, W7, W9

Figure 5: 8-Pin, SOP2 or W-PDFN (Top View)

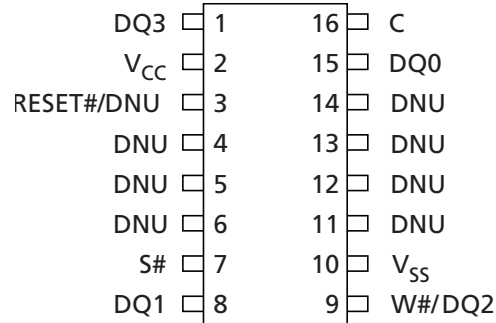


- Notes:
1. RESET# or HOLD# signals can share Pin 7 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.

- On the underside of the W-PDFN package, there is an exposed central pad that is pulled internally to V_{SS} . It can be left floating or can be connected to V_{SS} . It must not be connected to any other voltage or signal line on the PCB.

Signal Assignments – Package Code: SF

Figure 6: 16-Pin, Plastic Small Outline – SO16 (Top View)



- Notes:
- RESET# or HOLD# signals can share Pin 1 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
 - Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Descriptions

The signal description table below is a comprehensive list of signals for the MT25Q family devices. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

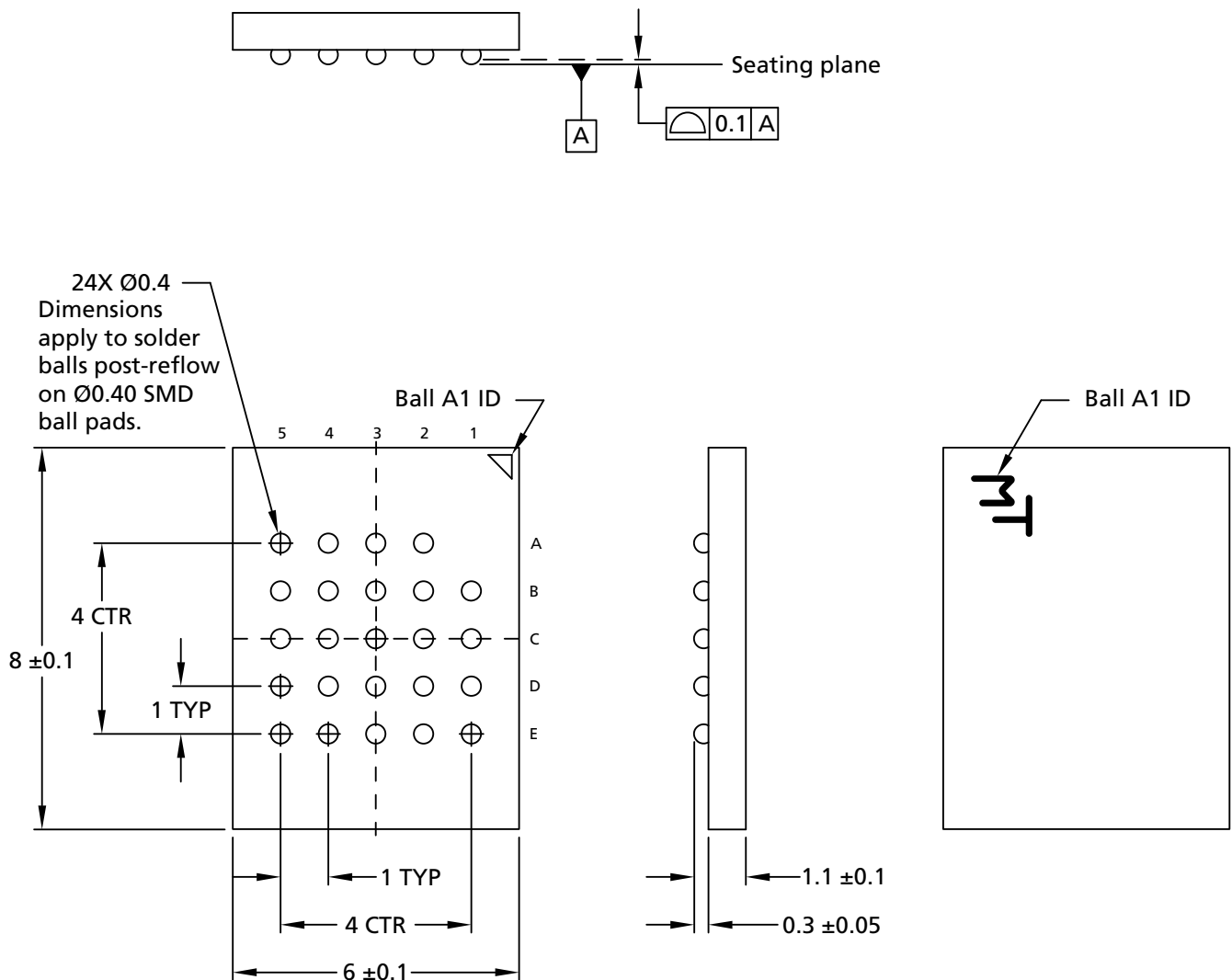
Symbol	Type	Description
S#	Input	<p>Chip select: When S# is driven HIGH, the device will enter standby mode, unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress. All other input pins are ignored and the output pins are tri-stated. On parts with the pin configuration offering a dedicated RESET# pin, however, the RESET# input pin remains active even when S# is HIGH.</p> <p>Driving S# LOW enables the device, placing it in the active mode.</p> <p>After power-up, a falling edge on S# is required prior to the start of any command.</p>
C	Input	<p>Clock: Provides the timing of the serial interface. Command inputs are latched on the rising edge of the clock. In STR commands or protocol, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DTR commands or protocol, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.</p>
RESET#	Input	<p>RESET#: When RESET# is driven LOW, the device is reset and the outputs are tri-stated. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost. The RESET# functionality can be disabled using bit 4 of the nonvolatile configuration register or bit 4 of the enhanced volatile configuration register.</p> <p>For pin configurations that share the DQ3 pin with RESET#, the RESET# functionality is disabled in QIO-SPI mode.</p>
HOLD#	Input	<p>HOLD: Pauses serial communications with the device without deselecting or resetting the device. Outputs are tri-stated and inputs are ignored. The HOLD# functionality can be disabled using bit 4 of the nonvolatile configuration register or bit 4 of the enhanced volatile configuration register.</p> <p>For pin configurations that share the DQ3 pin with HOLD#, the HOLD# functionality is disabled in QIO-SPI mode or when DTR operation is enabled.</p>
W#	Input	<p>Write protect: Freezes the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and the W# signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. During the Extended-SPI protocol with QOFR and QIOFR instructions, and with QIO-SPI protocol, this pin functions as an input/output (DQ2 functionality). This signal does not have internal pull-ups, it cannot be left floating and must be driven, even if none of W#/DQ2 function is used.</p>
DQ[3:0]	I/O	<p>Serial I/O: The bidirectional DQ signals transfer address, data, and command information.</p> <p>When using legacy (x1) SPI commands in extended I/O protocol (XIO-SPI), DQ0 is an input and DQ1 is an output. DQ[3:2] are not used.</p> <p>When using dual commands in XIO-SPI or when using DIO-SPI, DQ[1:0] are I/O. DQ[3:2] are not used.</p> <p>When using quad commands in XIO-SPI or when using QIO-SPI, DQ[3:0] are I/O.</p>
V _{CC}	Supply	Core and I/O power supply.

Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
V _{SS}	Supply	Core and I/O ground connection.
DNU	–	Do not use. Must be left floating.
NC	–	No connect. Not internally connected.

Package Dimensions – Package Code: 12

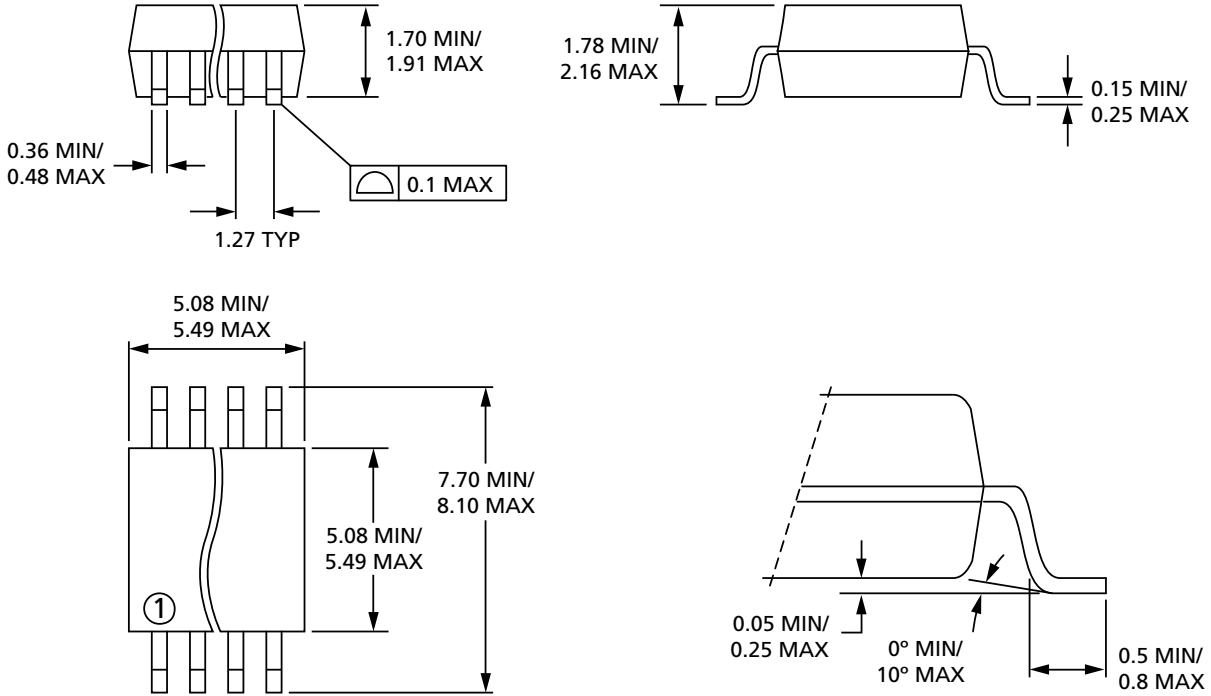
Figure 7: 24-Ball T-PBGA (5 x 5 ball grid array) – 6mm x 8mm



- Notes: 1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: SE

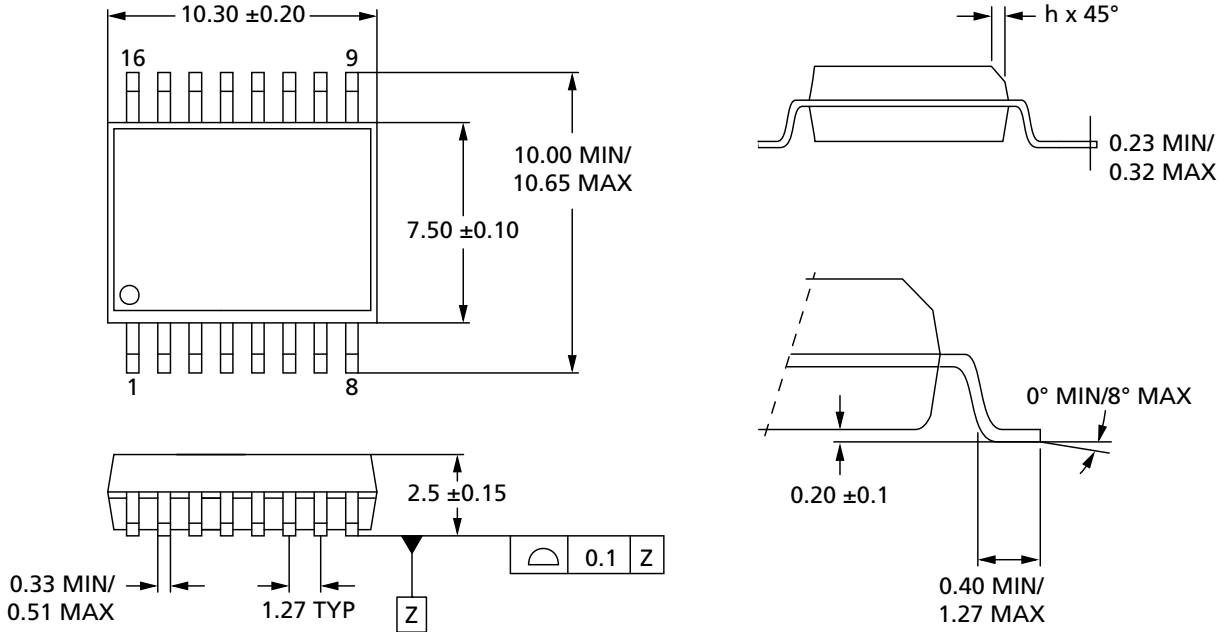
Figure 8: 8-Pin SOP2 (S08W) – 208 Mils Body Width



- Notes: 1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: SF

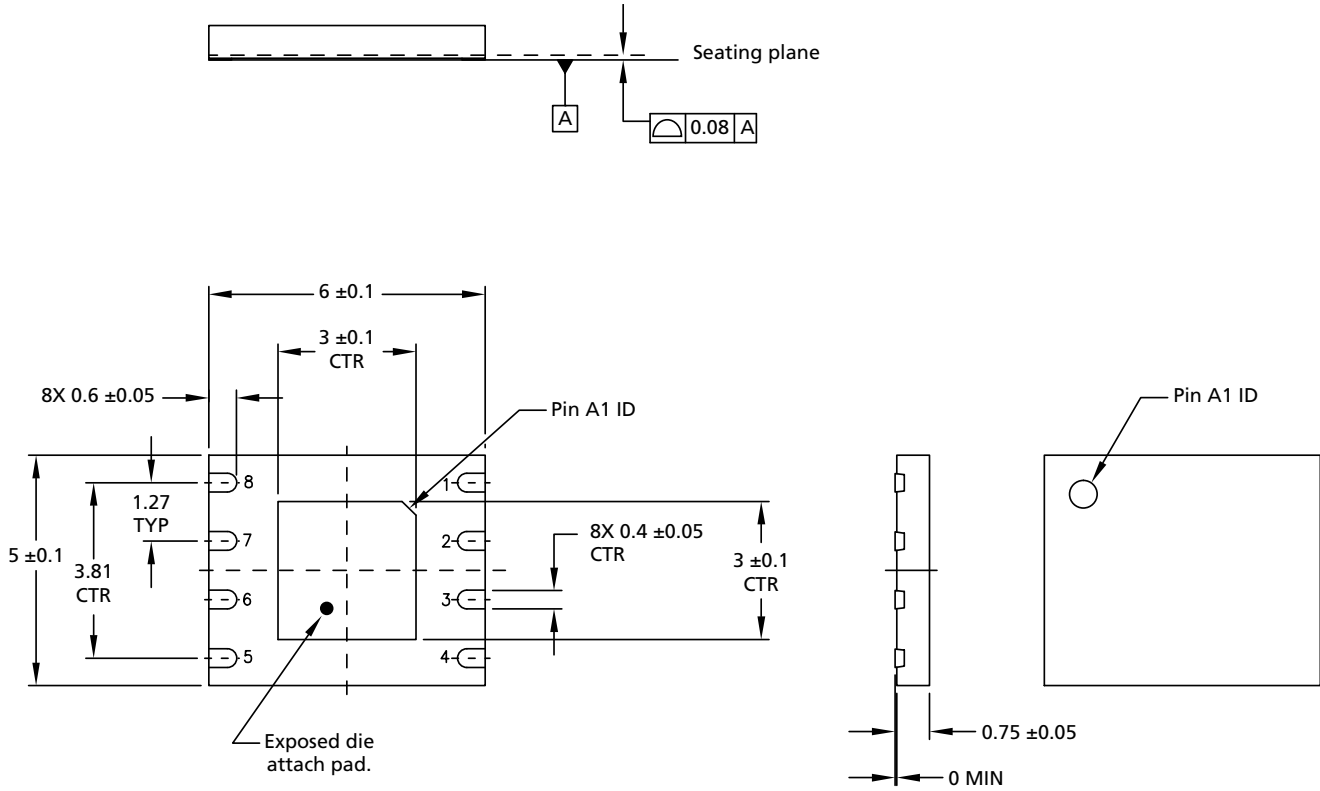
Figure 9: 16-Pin SOP2 – 300 mils Body Width



- Notes:
1. All dimensions are in millimeters.
 2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: W7

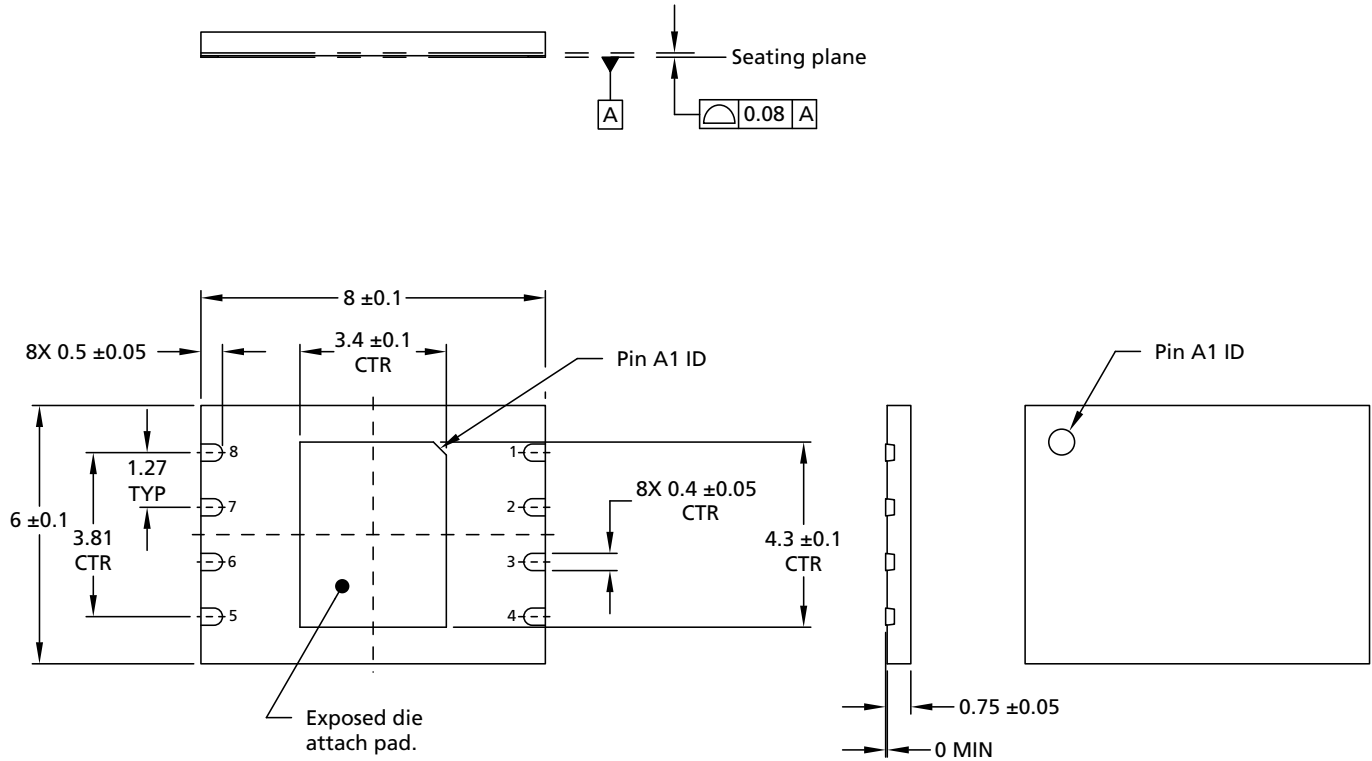
Figure 10: W-PDFN-8 (MLP8) – 6mm x 5mm



- Notes:
1. All dimensions are in millimeters.
 2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: W9

Figure 11: W-PDFN-8 (MLP8) – 8mm x 6mm



- Notes: 1. All dimensions are in millimeters.
 2. See Part Number Ordering Information for complete package names and details.



Memory Map – 128Mb Density

Table 2: Memory Map

Sector	Subsector (32KB)	Subsector (4KB)	Address Range	
			Start	End
255	511	4095	00FF F000h	00FF FFFFh
		⋮	⋮	⋮
		4088	00FF 8000h	00FF 8FFFh
	510	4087	00FF 7000h	00FF 7FFFh
		⋮	⋮	⋮
		4080	00FF 0000h	00FF 0FFFh
⋮	⋮	⋮	⋮	⋮
127	255	2047	007F F000h	007F FFFFh
		⋮	⋮	⋮
		2040	007F 8000h	007F 8FFFh
	254	2039	007F 7000h	007F 7FFFh
		⋮	⋮	⋮
		2032	007F 0000h	007F 0FFFh
⋮	⋮	⋮	⋮	⋮
63	127	1023	003F F000h	003F FFFFh
		⋮	⋮	⋮
		1016	003F 8000h	003F 8FFFh
	126	1015	003F 7000h	003F 7FFFh
		⋮	⋮	⋮
		1008	003F 0000h	003F 0FFFh
⋮	⋮	⋮	⋮	⋮
0	1	15	0000 F000h	0000 FFFFh
		⋮	⋮	⋮
		8	0000 8000h	0000 8FFFh
	0	7	0000 7000h	0000 7FFFh
		⋮	⋮	⋮
		0	0000 0000h	0000 0FFFh

Note: 1. See Part Number Ordering Information, Sector Size – Part Numbers table for options.

Status Register

Status register bits can be read from or written to using READ STATUS REGISTER or WRITE STATUS REGISTER commands, respectively. When the status register enable/disable bit (bit 7) is set to 1 and W# is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. The only way to exit this hardware-protected mode is to drive W# HIGH.

Table 3: Status Register

Bit	Name	Settings	Description	Notes
7	Status register write enable/disable	0 = Enabled (default) 1 = Disabled	Nonvolatile control bit: Used with W# to enable or disable writing to the status register.	–
5	Top/bottom	0 = Top (default) 1 = Bottom	Nonvolatile control bit: Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	–
6, 4:2	BP[3:0]	See Protected Area tables	Nonvolatile control bit: Defines memory to be software protected against PROGRAM or ERASE operations. When one or more block protect bits is set to 1, a designated memory area is protected from PROGRAM and ERASE operations.	1
1	Write enable latch	0 = Clear (default) 1 = Set	Volatile control bit: The device always powers up with this bit cleared to prevent inadvertent WRITE, PROGRAM, or ERASE operations. To enable these operations, the WRITE ENABLE operation must be executed first to set this bit.	–
0	Write in progress	0 = Ready (default) 1 = Busy	Volatile status bit: Indicates if one of the following command cycles is in progress: WRITE STATUS REGISTER WRITE NONVOLATILE CONFIGURATION REGISTER PROGRAM ERASE	2

- Notes:
1. The BULK ERASE command is executed only if all bits = 0.
 2. Status register bit 0 is the inverse of flag status register bit 7.



Block Protection Settings

Table 4: Protected Area

Status Register Content					Protected Area
Top/Bottom	BP3	BP2	BP1	BP0	64KB Sectors
0	0	0	0	0	None
0	0	0	0	1	255:255
0	0	0	1	0	255:254
0	0	0	1	1	255:252
0	0	1	0	0	255:248
0	0	1	0	1	255:240
0	0	1	1	0	255:224
0	0	1	1	1	255:192
0	1	0	0	0	255:128
0	1	0	0	1	255:0
0	1	0	1	0	255:0
0	1	0	1	1	255:0
0	1	1	0	0	255:0
0	1	1	1	0	255:0
0	1	1	1	1	255:0
1	0	0	0	0	None
1	0	0	0	1	0:0
1	0	0	1	0	1:0
1	0	0	1	1	3:0
1	0	1	0	0	7:0
1	0	1	0	1	15:0
1	0	1	1	0	31:0
1	0	1	1	1	63:0
1	1	0	0	0	127:0
1	1	0	0	1	255:0
1	1	0	1	0	255:0
1	1	0	1	1	255:0
1	1	1	0	0	255:0
1	1	1	0	1	255:0
1	1	1	1	0	255:0
1	1	1	1	0	255:0
1	1	1	1	1	255:0

Flag Status Register

Flag status register bits are read by using READ FLAG STATUS REGISTER command. All bits are volatile and are reset to zero on power up.

Status bits are set and reset automatically by the internal controller. Error bits must be cleared through the CLEAR STATUS REGISTER command.

Table 5: Flag Status Register

Bit	Name	Settings	Description
7	Program or erase controller	0 = Busy 1 = Ready	Status bit: Indicates whether one of the following command cycles is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE.
6	Erase suspend	0 = Clear 1 = Suspend	Status bit: Indicates whether an ERASE operation has been or is going to be suspended.
5	Erase	0 = Clear 1 = Failure or protection error	Error bit: Indicates whether an ERASE operation has succeeded or failed.
4	Program	0 = Clear 1 = Failure or protection error	Error bit: Indicates whether a PROGRAM operation has succeeded or failed. It indicates, also, whether a CRC check has succeeded or failed.
3	Reserved	0	Reserved
2	Program suspend	0 = Clear 1 = Suspend	Status bit: Indicates whether a PROGRAM operation has been or is going to be suspended.
1	Protection	0 = Clear 1 = Failure or protection error	Error bit: Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.
0	Reserved	0	Reserved

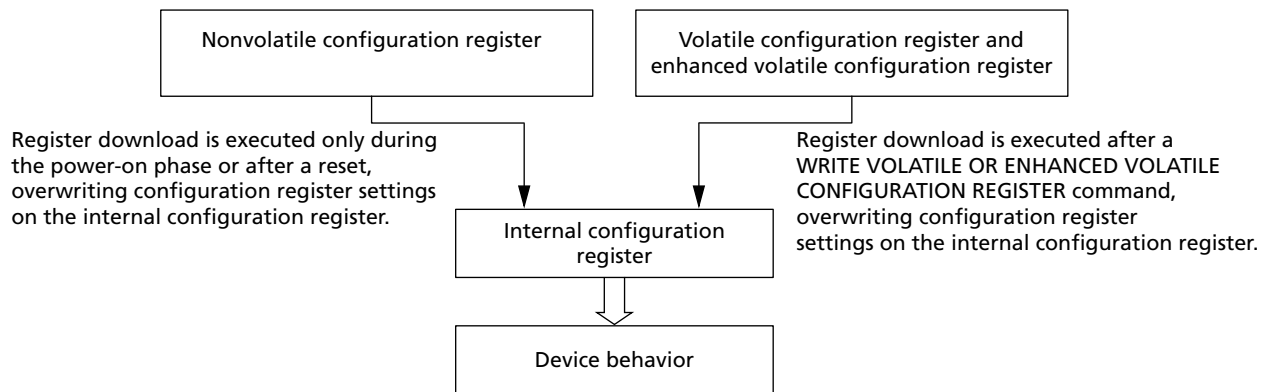
Internal Configuration Register

The memory configuration is set by an internal configuration register that is not directly accessible to users.

The user can change the default configuration at power up by using the WRITE NON-VOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset.

The user can change the configuration during operation by using the WRITE VOLATILE CONFIGURATION REGISTER or the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER commands. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.

Figure 12: Internal Configuration Register



Nonvolatile Configuration Register

This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. A register download is executed during power-on or after reset, overwriting the internal configuration register settings that determine device behavior.

Table 6: Nonvolatile Configuration Register

Bit	Name	Settings	Description	Notes
15:12	Number of dummy clock cycles	0000 = identical to 1111 0001 = 1 0010 = 2 . . 1101 = 13 1110 = 14 1111 = Default	Sets the number of dummy clock cycles subsequent to all FAST READ commands (See the Command Set Table for default setting values).	1
11:9	XIP mode at power-on reset	000 = XIP: Fast read 001 = XIP: Dual output fast read 010 = XIP: Dual I/O fast read 011 = XIP: Quad output fast read 100 = XIP: Quad I/O fast read 101 = Reserved 110 = Reserved 111 = Disabled (Default)	Enables the device to operate in the selected XIP mode immediately after power-on reset.	
8:6	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = Reserved 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = Reserved 111 = 30 Ohms (Default)	Optimizes the impedance at $V_{CC}/2$ output voltage.	
5	Double transfer rate protocol	0 = Enabled 1 = Disabled (Default)	Set DTR protocol as current one. Once enabled, all commands will work in DTR.	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables HOLD# or RESET# on DQ3.	
3	Quad I/O protocol	0 = Enabled 1 = Disabled (Default)	Enables or disables quad I/O command input (4-4-4 mode).	2
2	Dual I/O protocol	0 = Enabled 1 = Disabled (Default)	Enables or disables dual I/O command input (2-2-2 mode).	2
1	Reserved	0	Reserved	
0	Reserved	0	Reserved	

- Notes:
1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ command (See Supported Clock Frequencies table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data.
 2. When bits 2 and 3 are both set to 0, the device operates in quad I/O protocol.

Volatile Configuration Register

This register is read from and written to by the READ VOLATILE CONFIGURATION REGISTER and the WRITE VOLATILE CONFIGURATION REGISTER commands, respectively. A register download is executed after these commands, overwriting the internal configuration register settings that determine device memory behavior.

Table 7: Volatile Configuration Register

Bit	Name	Settings	Description	Notes
7:4	Number of dummy clock cycles	0000 = Identical to 1111 0001 = 1 0010 = 2 : 1101 = 13 1110 = 14 1111 = Default	Sets the number of dummy clock cycles subsequent to all FAST READ commands. (See the Command Set Table for default setting values.)	1
3	XIP	0 = Enable 1 = Disable (Default)	Enables or disables XIP.	
2	Reserved	0	0b = Fixed value.	
1:0	Wrap	00 = 16-byte boundary aligned	16-byte wrap: Output data wraps within an aligned 16-byte boundary starting from the 3-byte address issued after the command code.	2
		01 = 32-byte boundary aligned	32-byte wrap: Output data wraps within an aligned 32-byte boundary starting from the 3-byte address issued after the command code.	
		10 = 64-byte boundary aligned	64-byte wrap: Output data wraps within an aligned 64-byte boundary starting from the 3-byte address issued after the command code.	
		11 = Continuous (Default)	Continuously sequences addresses through the entire array.	

- Notes:
1. The number of cycles must be set according to and sufficient for the clock frequency, which varies by the type of FAST READ command, as shown in the Supported Clock Frequencies table. An insufficient number of dummy clock cycles for the operating frequency causes the memory to read incorrect data.
 2. See the Sequence of Bytes During Wrap table.

Table 8: Sequence of Bytes During Wrap

Starting Address	16-Byte Wrap	32-Byte Wrap	64-Byte Wrap
0	0-1-2- ... -15-0-1- ..	0-1-2- ... -31-0-1- ..	0-1-2- ... -63-0-1- ..
1	1-2- ... -15-0-1-2- ..	1-2- ... -31-0-1-2- ..	1-2- ... -63-0-1-2- ..
....
15	15-0-1-2-3- ... -15-0-1- ..	15-16-17- ... -31-0-1- ..	15-16-17- ... -63-0-1- ..
....
31	-	31-0-1-2-3- ... -31-0-1- ..	31-32-33- ... -63-0-1- ..
....
63	-	-	63-0-1- ... -63-0-1- ..

Supported Clock Frequencies

Table 9: Clock Frequencies – STR (in MHz)

Notes apply to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	94	79	60	44	39
2	112	97	77	61	48
3	129	106	86	78	58
4	133	115	97	97	69
5	133	125	106	106	78
6	133	133	115	115	86
7	133	133	125	125	97
8	133	133	133	133	106
9	133	133	133	133	115
10	133	133	133	133	125
11 : 14	133	133	133	133	133

- Notes:
1. Values are guaranteed by characterization and not 100% tested in production.
 2. A tuning data pattern (TDP) capability provides applications with data patterns for adjusting the data latching point at the host end when the clock frequency is set higher than 133 MHz in STR mode and higher than 66 MHz in double transfer rate (DTR) mode. For additional details, refer to TN-25-07: Tuning Data Pattern for MT25Q and MT25T Devices.