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Micron Serial NOR Flash Memory

3V, Multiple I/O, 4KB, 32KB, 64KB, Sector Erase

MT25QL256ABA

Features

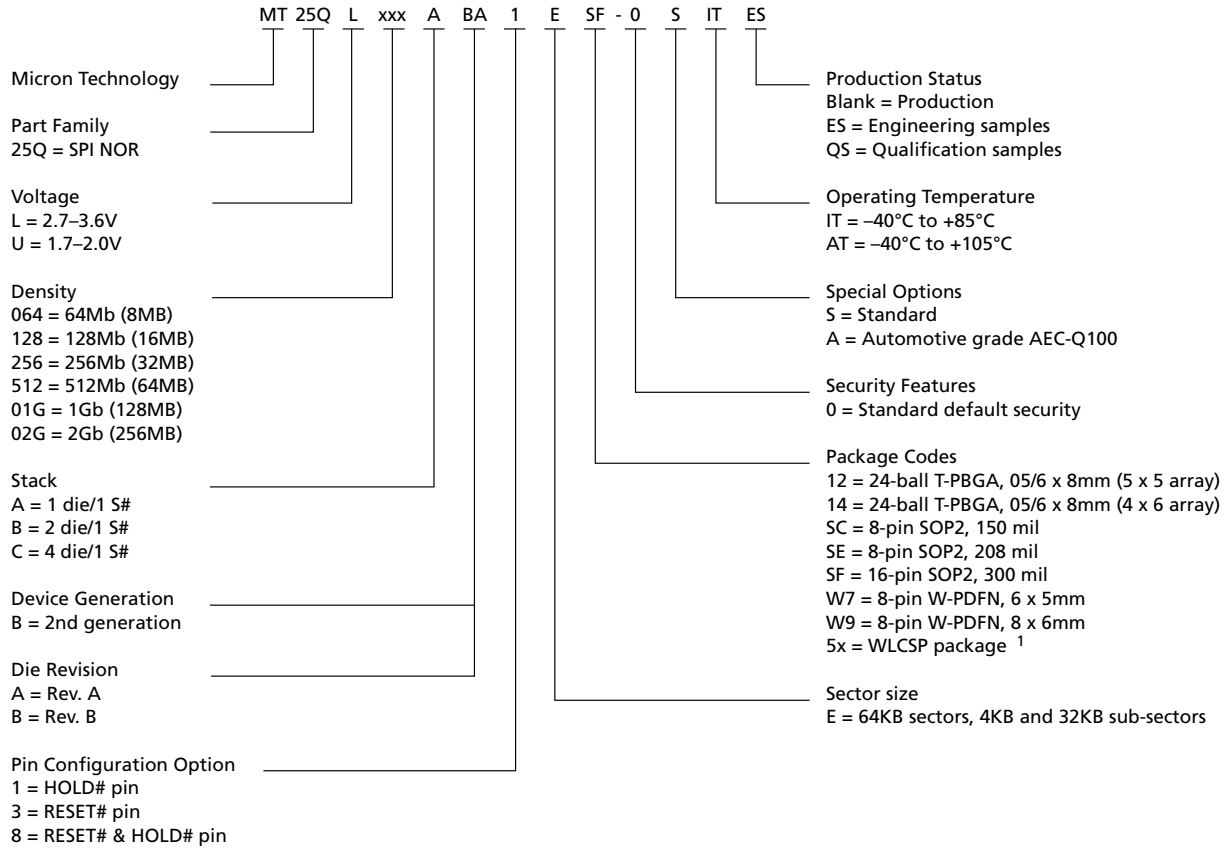
- SPI-compatible serial bus interface
- Single and double transfer rate (STR/DTR)
- Clock frequency
  - 133 MHz (MAX) for all protocols in STR
  - 90 MHz (MAX) for all protocols in DTR
- Dual/quad I/O commands for increased throughput up to 90 MB/s
- Supported protocols in both STR and DTR
  - Extended I/O protocol
  - Dual I/O protocol
  - Quad I/O protocol
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Additional reset pin for selected part numbers
- 3-byte and 4-byte address modes – enable memory access beyond 128Mb
- Dedicated 64-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with PROGRAM OTP command
- Erase capability
  - Bulk erase
  - Sector erase 64KB uniform granularity
  - Subsector erase 4KB, 32KB granularity
- Security and write protection
  - Volatile and nonvolatile locking and software write protection for each 64KB sector
  - Nonvolatile configuration locking
  - Password protection
  - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
  - Program/erase protection during power-up
  - CRC detects accidental changes to raw data
- Electronic signature
  - JEDEC-standard 3-byte signature (BA19h)
  - Extended device ID: two additional bytes identify device factory options
- JESD47H-compliant
  - Minimum 100,000 ERASE cycles per sector
  - Data retention: 20 years (TYP)

Options	Marking
• Voltage	
– 2.7–3.6V	L
• Density	
– 256Mb	256
• Device stacking	
– Monolithic	A
• Device generation	B
• Die revision	A
• Pin configuration	
– RESET and HOLD#	8
• Sector Size	
– 64KB	E
• Packages – JEDEC-standard, RoHS-compliant	
– 24-ball T-PBGA 05/6mm x 8mm (5 x 5 array)	12
– 24-ball T-PBGA 05/6mm x 8mm (4 x 6 array)	14
– 16-pin SOP2, 300 mil (SO16W, SO16-Wide, SOIC-16)	SF
– W-PDFN-8 6mm x 5mm (MLP8 6mm x 5mm)	W7
– W-PDFN-8 8mm x 6mm (MLP8 8mm x 6mm)	W9
• Standard security	0
• Special options	
– Standard	S
– Automotive	A
• Operating temperature range	
– From –40°C to +85°C	IT
– From –40°C to +105°C	AT

Part Number Ordering

Micron Serial NOR Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Ordering Information



Note: 1. WLCSP package codes, package size, and availability are density-specific. Contact the factory for availability.

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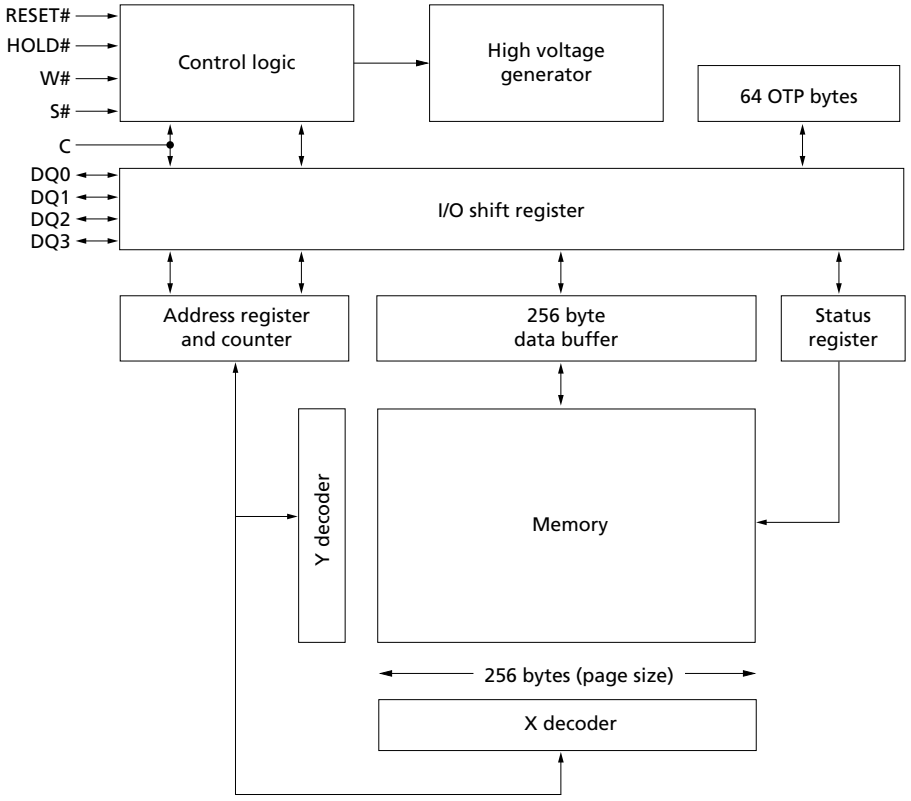
Device Description

The MT25Q is a high-performance multiple input/output serial Flash memory device. It features a high-speed SPI-compatible bus interface, execute-in-place (XIP) functionality, advanced write protection mechanisms, and extended address access. Innovative, high-performance, dual and quad input/output commands enable double or quadruple the transfer bandwidth for READ and PROGRAM operations.

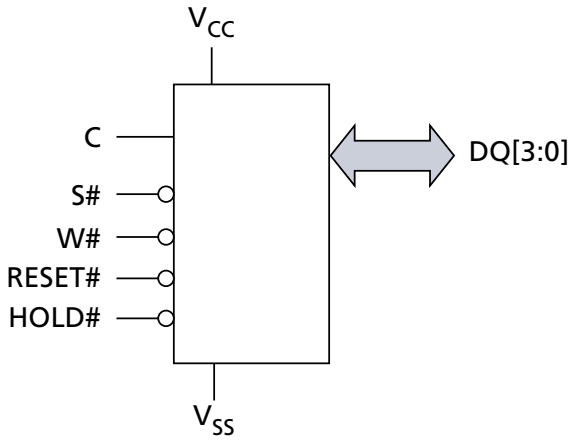
Figure 2: Block Diagram



Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

Device Logic Diagram

Figure 3: Logic Diagram



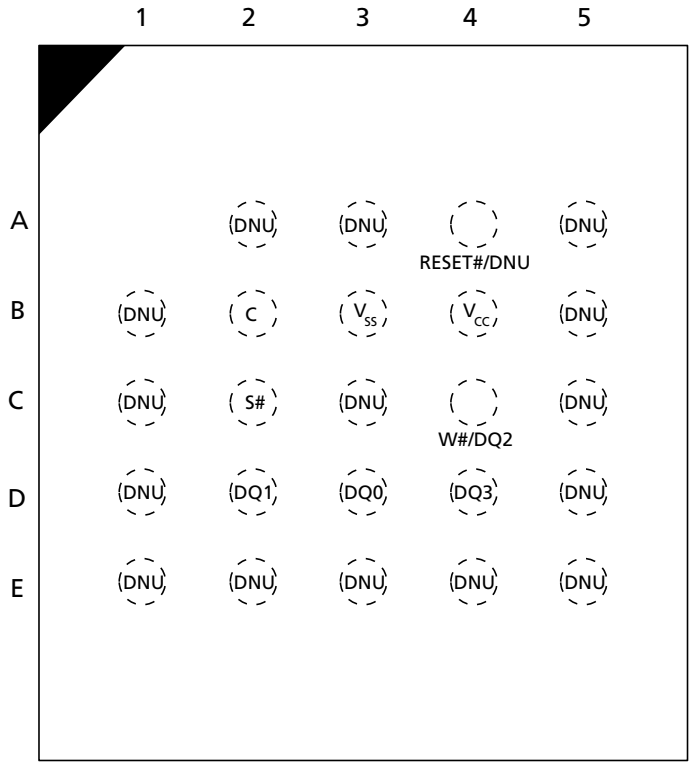
Notes:
1. Depending on the selected device (see Part Numbering Ordering Information), DQ3 = DQ3/RESET# or DQ3/HOLD#.
2. A separate RESET pin is available on dedicated part numbers (see Part Numbering Ordering Information).

Advanced Security Protection

The device offers an advanced security protection scheme where each sector can be independently locked, by either volatile or nonvolatile locking features. The nonvolatile locking configuration can also be locked, as well password-protected. See Block Protection Settings and Sector and Password Protection for more details.

Signal Assignments – Package Code: 12

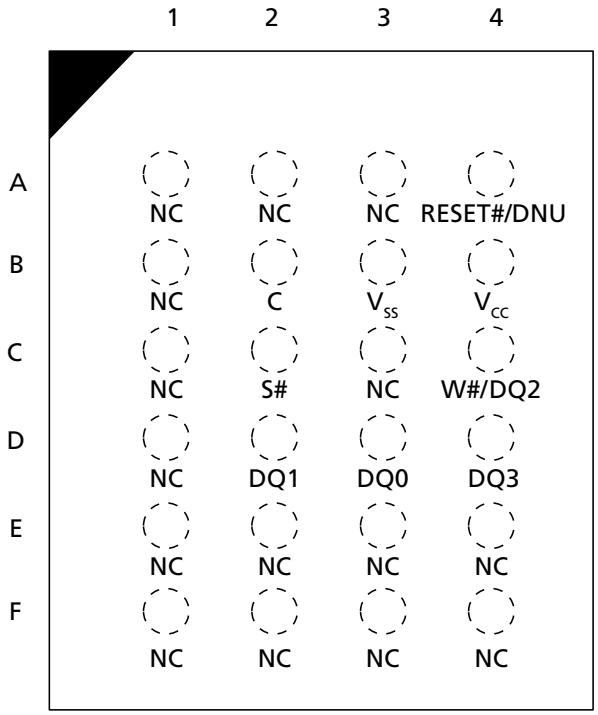
Figure 4: 24-Ball T-BGA, 5 x 5 (Balls Down)



Notes:
1. RESET# or HOLD# signals can share Ball D4 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Ball A4 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Assignments – Package Code: 14

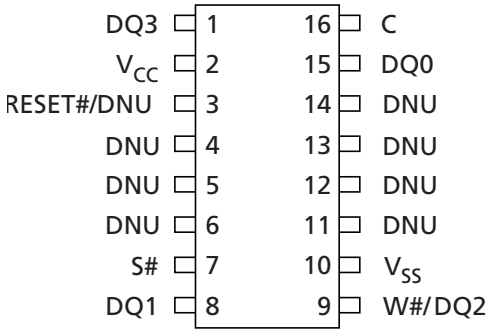
Figure 5: 24-Ball TBGA, 4 x 6 (Balls Down)



Notes:
1. RESET# or HOLD# signals can share Ball D4 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Ball A4 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Assignments – Package Code: SF

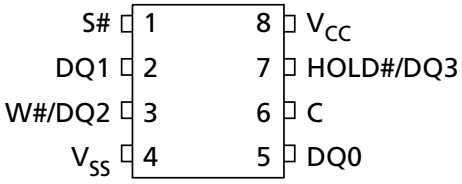
Figure 6: 16-Pin, Plastic Small Outline – SO16 (Top View)



Notes:
1. RESET# or HOLD# signals can share Pin 1 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Assignments – Package Code: W7, W9

Figure 7: 8-Pin, SOP2 or W-PDFN (Top View)



Notes:
1. RESET# or HOLD# signals can share Pin 7 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. On the underside of the W-PDFN package, there is an exposed central pad that is pulled internally to V_{SS}. It can be left floating or can be connected to V_{SS}. It must not be connected to any other voltage or signal line on the PCB.

Signal Descriptions

The signal description table below is a comprehensive list of signals for the MT25Q family devices. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

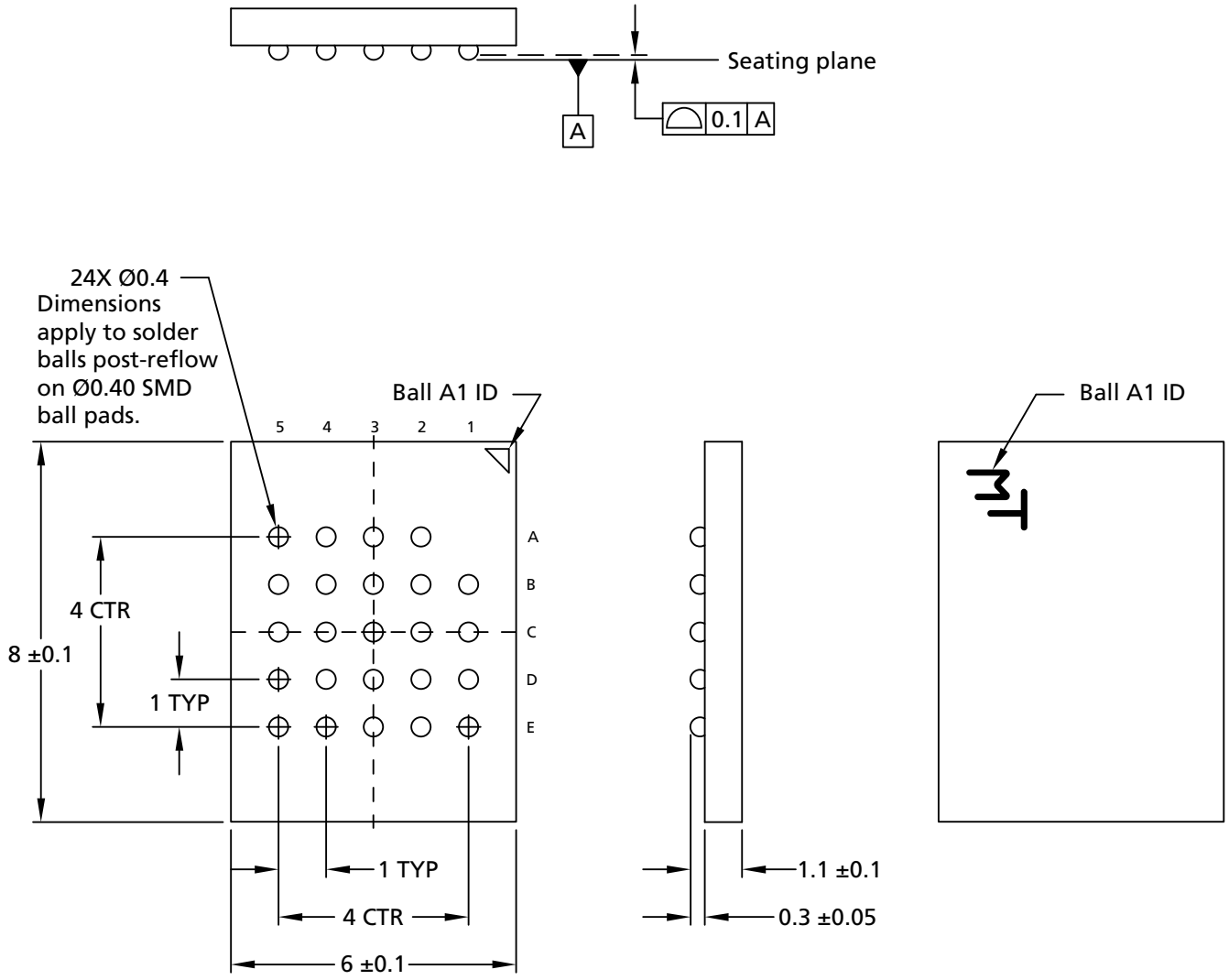
Symbol	Type	Description
S#	Input	**Chip select:** When S# is driven HIGH, the device will enter standby mode, unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress. All other input pins are ignored and the output pins are tri-stated. On parts with the pin configuration offering a dedicated RESET# pin, however, the RESET# input pin remains active even when S# is HIGH. Driving S# LOW enables the device, placing it in the active mode. After power-up, a falling edge on S# is required prior to the start of any command.
C	Input	**Clock:** Provides the timing of the serial interface. Command inputs are latched on the rising edge of the clock. In STR commands or protocol, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DTR commands or protocol, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
RESET#	Input	**RESET#:** When RESET# is driven LOW, the device is reset and the outputs are tri-stated. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost. The RESET# functionality can be disabled using bit 4 of the nonvolatile configuration register or bit 4 of the enhanced volatile configuration register. For pin configurations that share the DQ3 pin with RESET#, the RESET# functionality is disabled in QIO-SPI mode.
HOLD#	Input	**HOLD:** Pauses serial communications with the device without deselecting or resetting the device. Outputs are tri-stated and inputs are ignored. The HOLD# functionality can be disabled using bit 4 of the nonvolatile configuration register or bit 4 of the enhanced volatile configuration register. For pin configurations that share the DQ3 pin with HOLD#, the HOLD# functionality is disabled in QIO-SPI mode or when DTR operation is enabled.
W#	Input	**Write protect:** Freezes the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and the W# signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. During the Extended-SPI protocol with QOFR and QIOFR instructions, and with QIO-SPI protocol, this pin functions as an input/output (DQ2 functionality). This signal does not have internal pull-ups, it cannot be left floating and must be driven, even if none of W#/DQ2 function is used.
DQ[3:0]	I/O	**Serial I/O:** The bidirectional DQ signals transfer address, data, and command information. When using legacy (x1) SPI commands in extended I/O protocol (XIO-SPI), DQ0 is an input and DQ1 is an output. DQ[3:2] are not used. When using dual commands in XIO-SPI or when using DIO-SPI, DQ[1:0] are I/O. DQ[3:2] are not used. When using quad commands in XIO-SPI or when using QIO-SPI, DQ[3:0] are I/O.
V_{CC}	Supply	Core and I/O power supply.

Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
V_{SS}	Supply	Core and I/O ground connection.
DNU	–	Do not use. Must be left floating.
NC	–	No connect. Not internally connected.

Package Dimensions – Package Code: 12

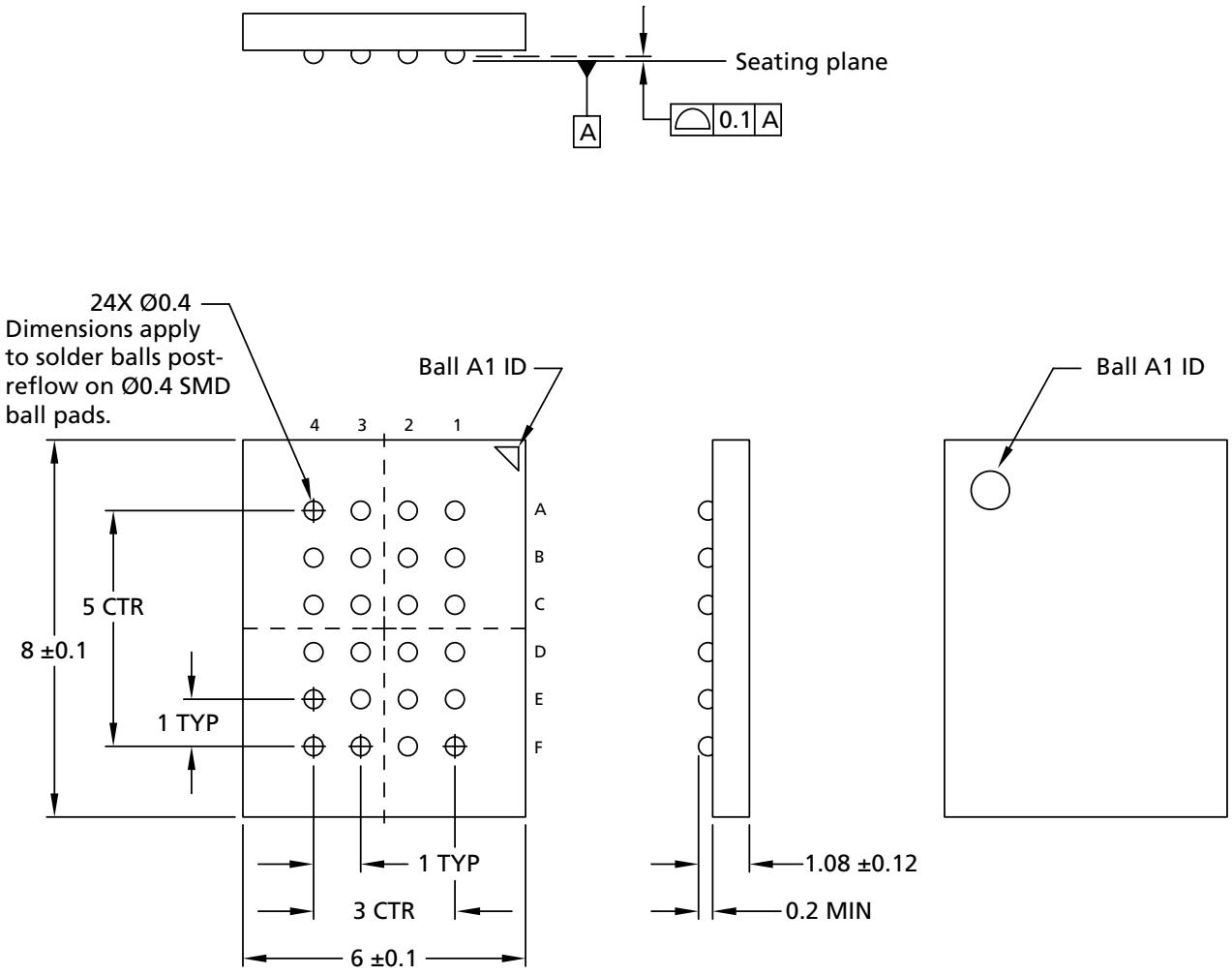
Figure 8: 24-Ball T-PBGA (5 x 5 ball grid array) – 6mm x 8mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: 14

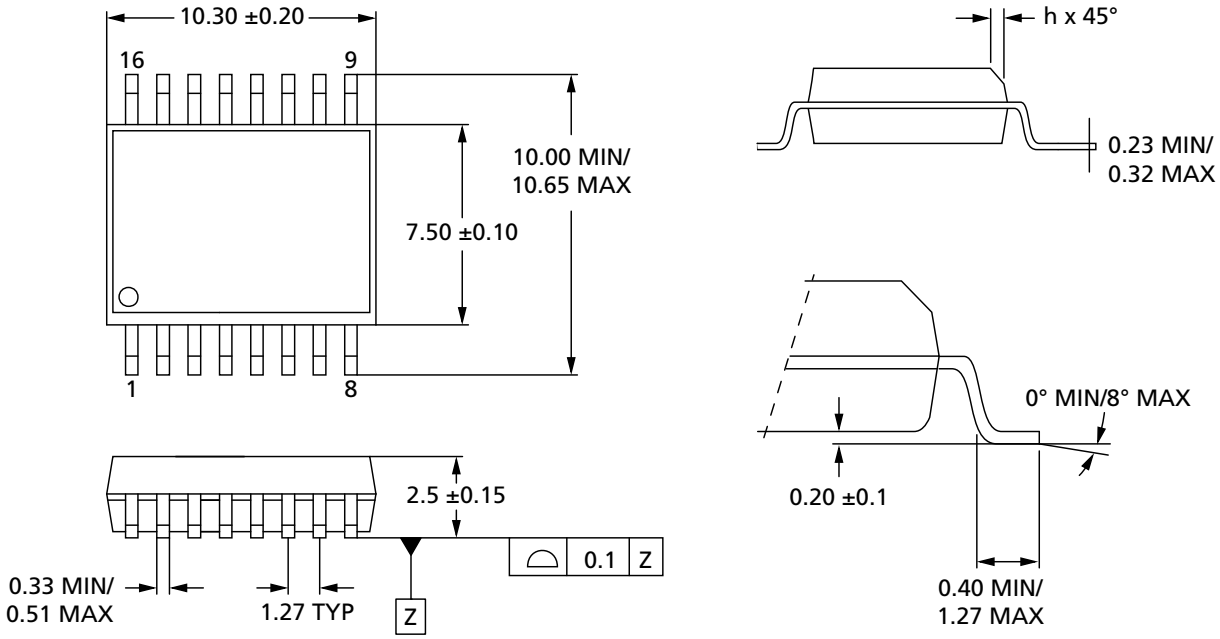
Figure 9: 24-Ball T-PBGA (24b05) – 6mm x 8mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: SF

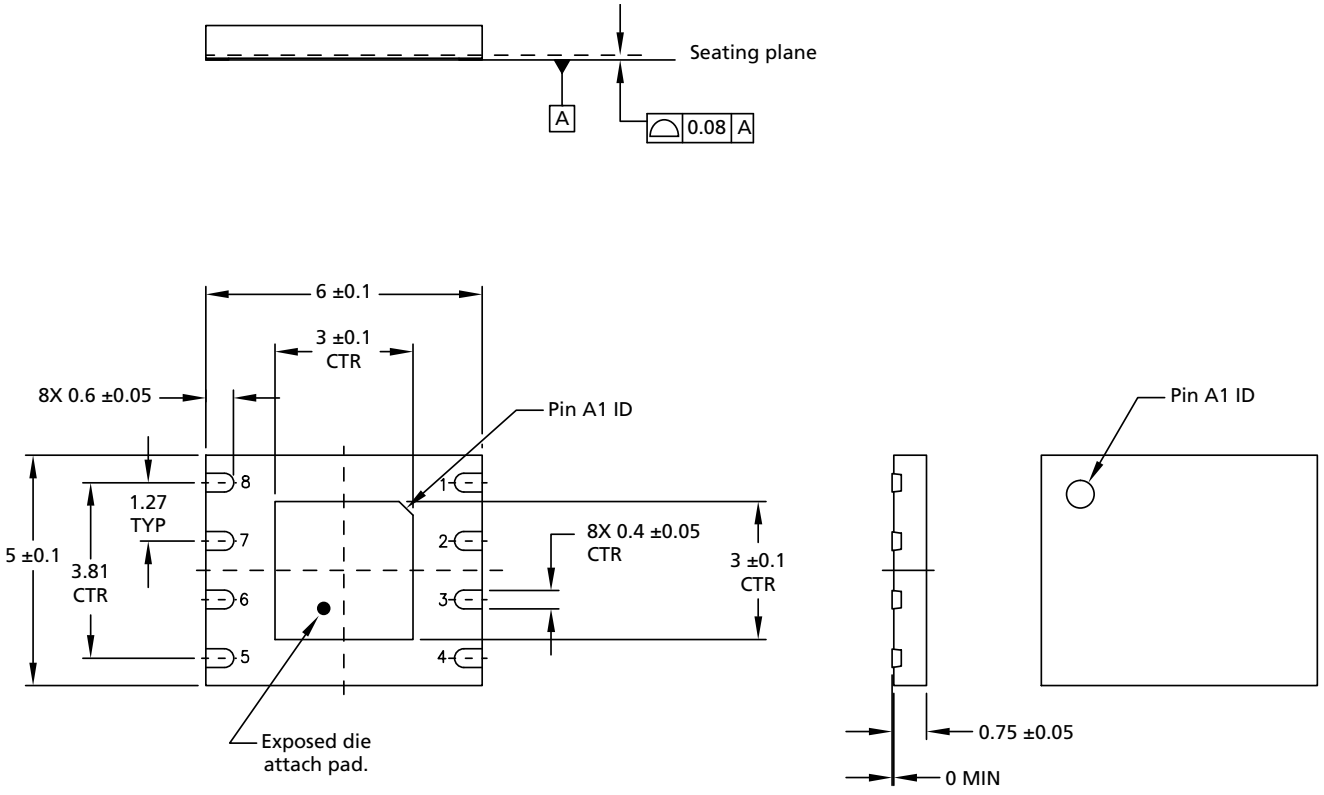
Figure 10: 16-Pin SOP2 – 300 mil Body Width



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: W7

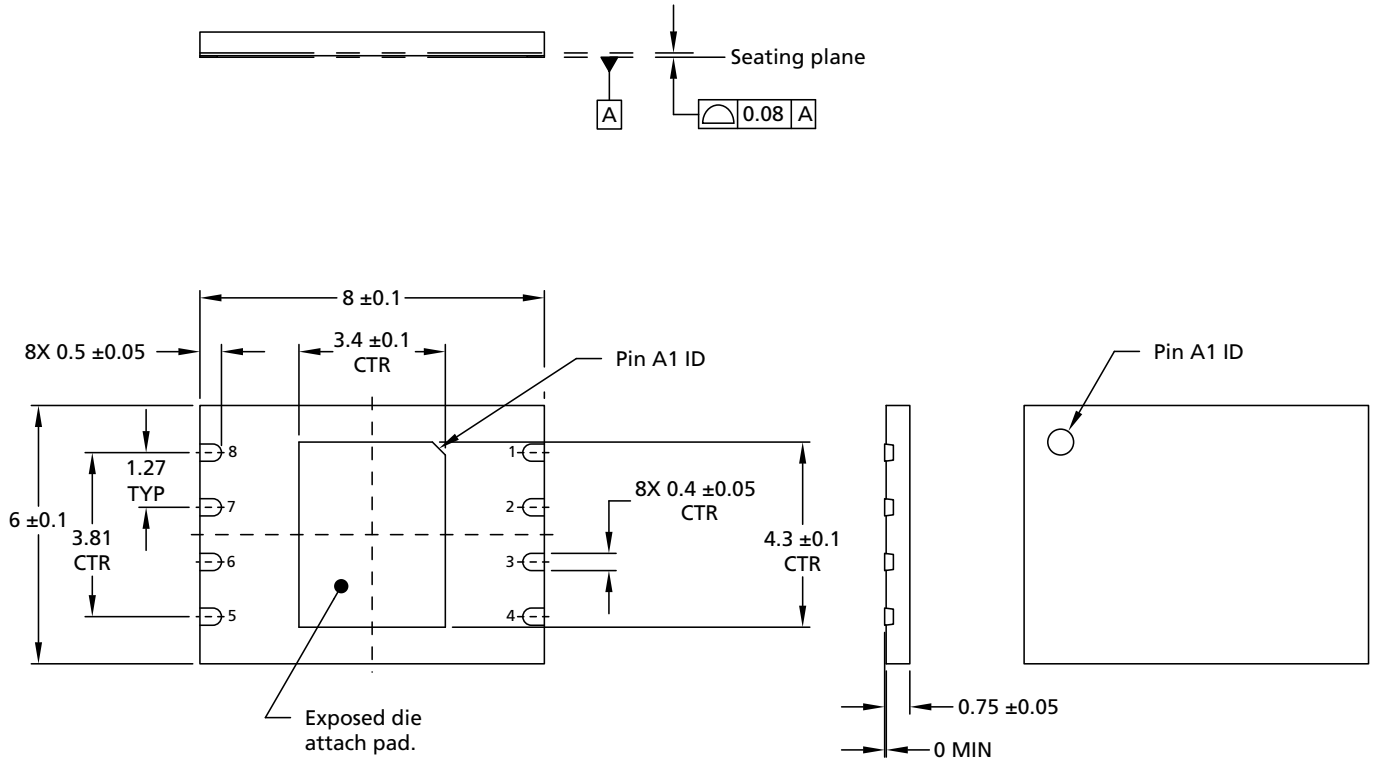
Figure 11: W-PDFN-8 (MLP8) – 6mm x 5mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: W9

Figure 12: W-PDFN-8 (MLP8) – 8mm x 6mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Memory Map – 256Mb Density

Table 2: Memory Map

Sector	Subsector (32KB)	Subsector (4KB)	Address Range	
			Start	End
511	1023	8191	01FF F000h	01FF FFFFh
		⋮	⋮	⋮
		8184	01FF 8000h	01FF 8FFFh
	1022	8183	01FF 7000h	01FF 7FFFh
		⋮	⋮	⋮
		8176	01FF 0000h	01FF 0FFFh
⋮	⋮	⋮	⋮	⋮
255	511	4095	00FF F000h	00FF FFFFh
		⋮	⋮	⋮
		4088	00FF 8000h	00FF 8FFFh
	510	4087	00FF 7000h	00FF 7FFFh
		⋮	⋮	⋮
		4080	00FF 0000h	00FF 0FFFh
⋮	⋮	⋮	⋮	⋮
127	255	2047	007F F000h	007F FFFFh
		⋮	⋮	⋮
		2040	007F 8000h	007F 8FFFh
	254	2039	007F 7000h	007F 7FFFh
		⋮	⋮	⋮
		2032	007F 0000h	007F 0FFFh
⋮	⋮	⋮	⋮	⋮
0	1	15	0000 F000h	0000 FFFFh
		⋮	⋮	⋮
		8	0000 8000h	0000 8FFFh
	0	7	0000 7000h	0000 7FFFh
		⋮	⋮	⋮
		0	0000 0000h	0000 0FFFh

Note: 1. See Part Number Ordering Information, Sector Size – Part Numbers table for options.

Status Register

Status register bits can be read from or written to using READ STATUS REGISTER or WRITE STATUS REGISTER commands, respectively. When the status register enable/disable bit (bit 7) is set to 1 and W# is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. The only way to exit this hardware-protected mode is to drive W# HIGH.

Table 3: Status Register

Bit	Name	Settings	Description	Notes
7	Status register write enable/disable	0 = Enabled (default) 1 = Disabled	**Nonvolatile control bit:** Used with W# to enable or disable writing to the status register.	–
5	Top/bottom	0 = Top (default) 1 = Bottom	**Nonvolatile control bit:** Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	–
6, 4:2	BP[3:0]	See Protected Area tables	**Nonvolatile control bit:** Defines memory to be software protected against PROGRAM or ERASE operations. When one or more block protect bits is set to 1, a designated memory area is protected from PROGRAM and ERASE operations.	1
1	Write enable latch	0 = Clear (default) 1 = Set	**Volatile control bit:** The device always powers up with this bit cleared to prevent inadvertent WRITE, PROGRAM, or ERASE operations. To enable these operations, the WRITE ENABLE operation must be executed first to set this bit.	–
0	Write in progress	0 = Ready (default) 1 = Busy	**Volatile status bit:** Indicates if one of the following command cycles is in progress: WRITE STATUS REGISTER WRITE NONVOLATILE CONFIGURATION REGISTER PROGRAM ERASE	2

Notes:
1. The BULK ERASE command is executed only if all bits = 0.
2. Status register bit 0 is the inverse of flag status register bit 7.

Block Protection Settings

Table 4: Protected Area

Status Register Content					Protected Area
Top/Bottom	BP3	BP2	BP1	BP0	64KB Sectors
0	0	0	0	0	None
0	0	0	0	1	511:511
0	0	0	1	0	511:510
0	0	0	1	1	511:508
0	0	1	0	0	511:504
0	0	1	0	1	511:496
0	0	1	1	0	511:480
0	0	1	1	1	511:448
0	1	0	0	0	511:384
0	1	0	0	1	511:256
0	1	0	1	0	511:0
0	1	0	1	1	511:0
0	1	1	0	0	511:0
0	1	1	0	1	511:0
0	1	1	1	0	511:0
0	1	1	1	1	511:0
1	0	0	0	0	None
1	0	0	0	1	0:0
1	0	0	1	0	1:0
1	0	0	1	1	3:0
1	0	1	0	0	7:0
1	0	1	0	1	15:0
1	0	1	1	0	31:0
1	0	1	1	1	63:0
1	1	0	0	0	127:0
1	1	0	0	1	255:0
1	1	0	1	0	511:0
1	1	0	1	1	511:0
1	1	1	0	0	511:0
1	1	1	0	1	511:0
1	1	1	1	0	511:0
1	1	1	1	1	511:0

Flag Status Register

Flag status register bits are read by using READ FLAG STATUS REGISTER command. All bits are volatile and are reset to zero on power up.

Status bits are set and reset automatically by the internal controller. Error bits must be cleared through the CLEAR STATUS REGISTER command.

Table 5: Flag Status Register

Bit	Name	Settings	Description
7	Program or erase controller	0 = Busy 1 = Ready	**Status bit:** Indicates whether one of the following command cycles is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE.
6	Erase suspend	0 = Clear 1 = Suspend	**Status bit:** Indicates whether an ERASE operation has been or is going to be suspended.
5	Erase	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE operation has succeeded or failed.
4	Program	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether a PROGRAM operation has succeeded or failed. It indicates, also, whether a CRC check has succeeded or failed.
3	Reserved	0	Reserved
2	Program suspend	0 = Clear 1 = Suspend	**Status bit:** Indicates whether a PROGRAM operation has been or is going to be suspended.
1	Protection	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.
0	Addressing	0 = 3-byte addressing 1 = 4-byte addressing	**Status bit:** Indicates whether 3-byte or 4-byte address mode is enabled.

Extended Address Register

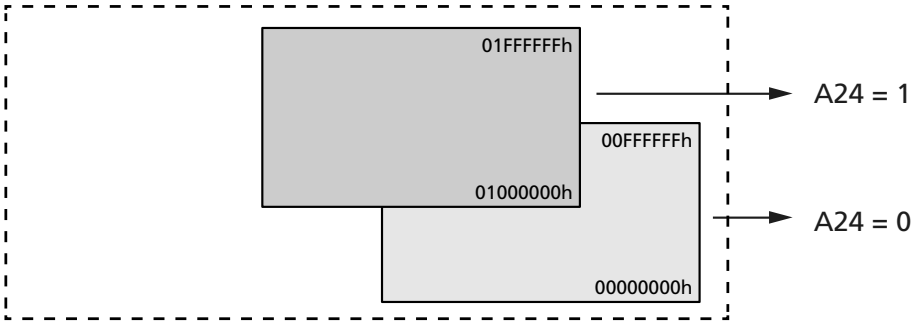
The 3-byte address mode can only access 128Mb of memory. To access the full device in 3-byte address mode, the device includes an extended address register that indirectly provides a fourth address byte A[31:25]. The extended address register bit A0 operates as memory address bit A24 to select one of the two 128Mb segments of the memory array.

If 4-byte addressing is enabled, the extended address register settings are ignored.

Table 6: Extended Address Register

Bit	Name	Settings	Description
7:1	A[31:25]	0000000	Reserved
0	A24	1 = Highest 128Mb segment 0 = Lowest 128Mb segment (default)	Enables specified 128Mb memory segment. The default (lowest) setting can be changed to the highest 128Mb segment using bit 1 of the nonvolatile configuration register.

Figure 13: Memory Array Segments



The PROGRAM and ERASE operations act upon the 128Mb segment selected in the extended address register. The BULK ERASE operation erases the entire device.

The READ operation begins reading in the selected 128Mb segment, but is not bound by it.

In a continuous READ, when the last byte of the segment is read, the next byte output is the first byte of the next segment. The operation wraps to 0000000h; therefore, a download of the whole array is possible with one READ operation.

The value of the extended address register does not change when a READ operation crosses the selected 128Mb boundary.

Internal Configuration Register

The memory configuration is set by an internal configuration register that is not directly accessible to users.

The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset.

The user can change the configuration during operation by using the WRITE VOLATILE CONFIGURATION REGISTER or the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER commands. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.

Figure 14: Internal Configuration Register