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Micron Serial NOR Flash Memory

3V, Twin-Quad I/O, 4KB, 32KB, 64KB, Sector Erase

MT25TL01GBBB, MT25TL01GHBB

Features

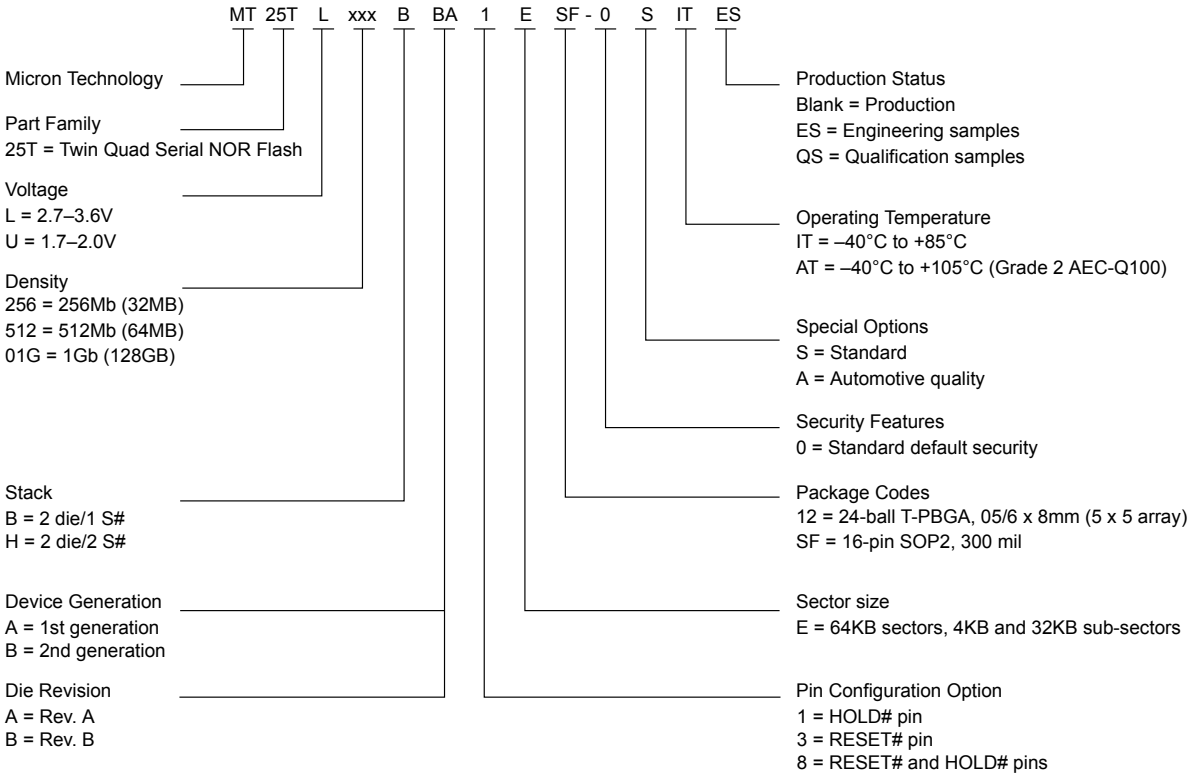
- Stacked device (two 512Mb die)
- SPI-compatible serial bus interface
- Single and double transfer rate (STR/DTR)
- Clock frequency
  - 133 MHz (MAX) for all protocols in STR
  - 90 MHz (MAX) for all protocols in DTR
- Dual/quad I/O instruction provides increased throughput up to 90 MB/s for each die corresponding to 180 MB/s for the twin-quad device
- Supported protocols in both STR and DTR
  - Extended I/O protocol
  - Dual I/O protocol
  - Quad I/O protocol
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Additional reset pin for selected part numbers
- 3-byte and 4-byte addressability mode supported
- Dedicated 64-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with PROGRAM OTP command
- Erase capability
  - Die erase
  - Sector erase 64KB uniform granularity
  - Subsector erase 4KB, 32KB granularity
- Security and write protection
  - Volatile and nonvolatile locking and software write protection for each 64KB sector
  - Nonvolatile configuration locking
  - Password protection
  - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
  - Program/erase protection during power-up
  - CRC detects accidental changes to raw data
- Electronic signature
  - JEDEC-standard 3-byte signature (BA20h)
  - Extended device ID: two additional bytes identify device factory options
- JESD47H-compliant
  - Minimum 100,000 ERASE cycles per sector
  - Data retention: 20 years (TYP)

Options	Marking
• Voltage	
– 2.7–3.6V	L
• Density	
– 1Gb	01G
• Device stacking	
– B = 2 die and 1 S# pin	B
– H = 2 die and 2 S# pins	H
• Device generation	B
• Die revision	B
• Pin configuration	
– RESET# and HOLD#	8
• Sector Size	
– 64KB	E
• Packages – JEDEC-standard, RoHS-compliant	
– 16-pin SOP2, 300 mils body width (SO16W)	SF
– 24-ball T-PBGA, 05/6mm x 8mm (TBGA24)	12
• Security Features	
– Standard	0
• Special options	
– Standard	S
– Automotive	A
• Standard security	0
• Operating temperature range	
– From –40°C to +85°C	IT
– From –40°C to +105°C	AT

Part Number Ordering

Micron Serial NOR Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Ordering Information



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Device Description

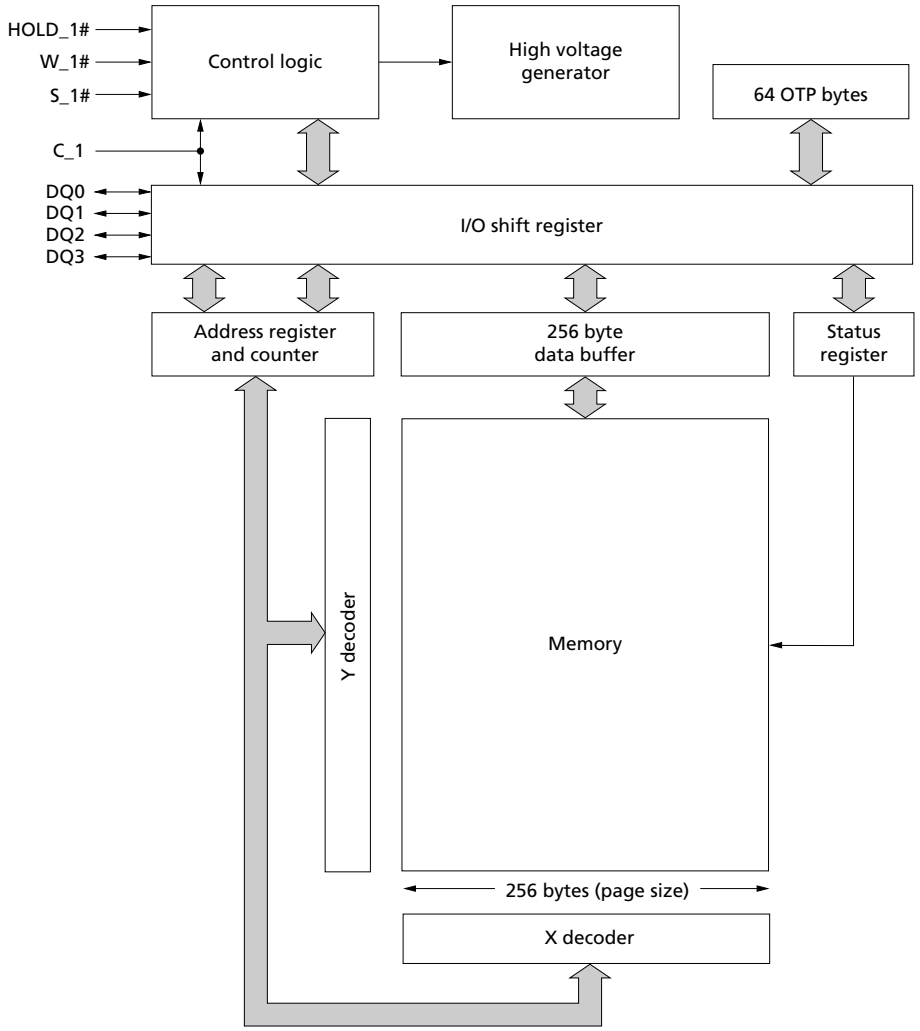
The MT25T is a high-performance, multiple input/output, serial NOR Flash memory device. It features a high-speed SPI-compatible bus interface, execute-in-place (XIP) functionality, advanced write protection mechanisms, and extended address access. Innovative, high-performance, dual and quad input/output commands enable double or quadruple the transfer bandwidth for READ and PROGRAM operations.

The device contains two quad I/O die, each able to operate independently for a total of eight I/Os. The memory map applies to each die. Each die has internal registers for status, configuration, and device protection that can be set and read independently from one other. Micron recommends that internal configuration settings for the two die be set identically.

The device is offered in two ways: One way is each die with its own S# and CLK signals, as represented in the "Separate Chip Select and Clock Signals" figure, and enabling each die to function independently. The other is an S# signal and a CLK signal shared between the two die, as represented in the "Shared Chip Select and Clock Signals" figure, and enabling the two die to function as one with higher bandwidth operations. Contact the factory for more information.

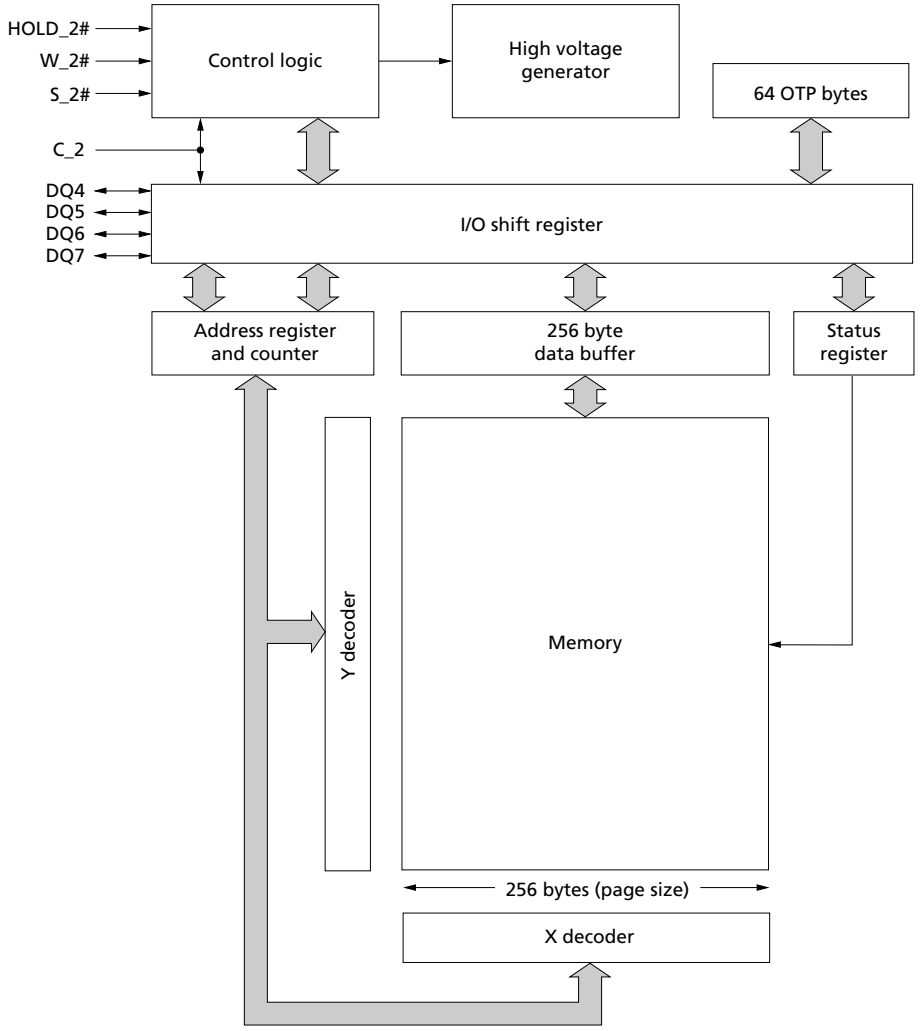
Block Diagram

Figure 2: Block Diagram – Flash Die 1



Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

Figure 3: Block Diagram – Flash Die 2



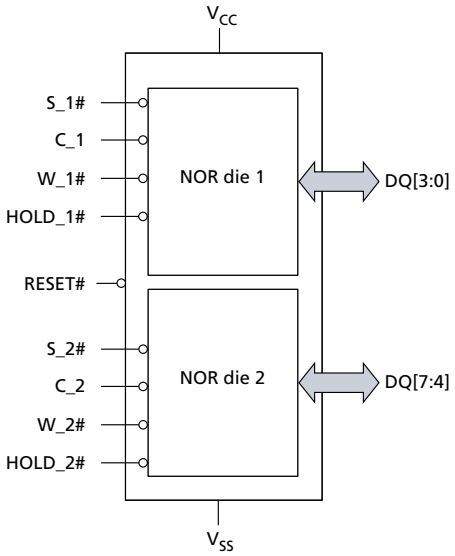
Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

Advanced Security Protection

The device offers an advanced security protection scheme where each sector can be independently locked, by either volatile or nonvolatile locking features. The nonvolatile locking configuration can also be locked, as well password-protected. See Block Protection Settings and Sector and Password Protection for more details.

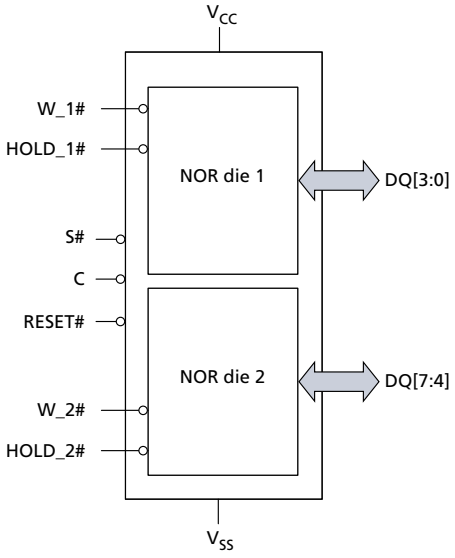
Device Logic Diagram

Figure 4: Logic Diagram – Separate Chip-Select and Clock Signals



Note: 1. The RESET# pin is available on dedicated part numbers. See the Part Numbering Ordering Information section for more details.

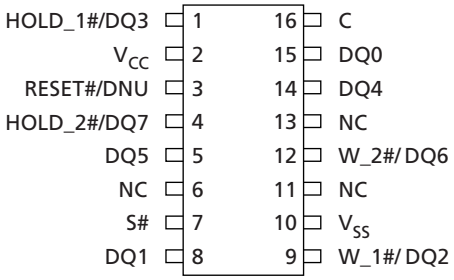
Figure 5: Logic Diagram – Shared Chip-Select and Clock Signals



Note: 1. The RESET# pin is available on dedicated part numbers. See the Part Numbering Ordering section for more details.

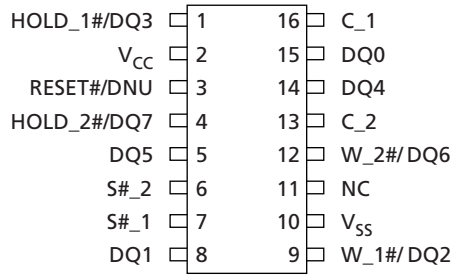
Signal Assignments

Figure 6: 16-Pin, Plastic Small Outline – SO16 (Top View) (Single Chip-Select and Clock)



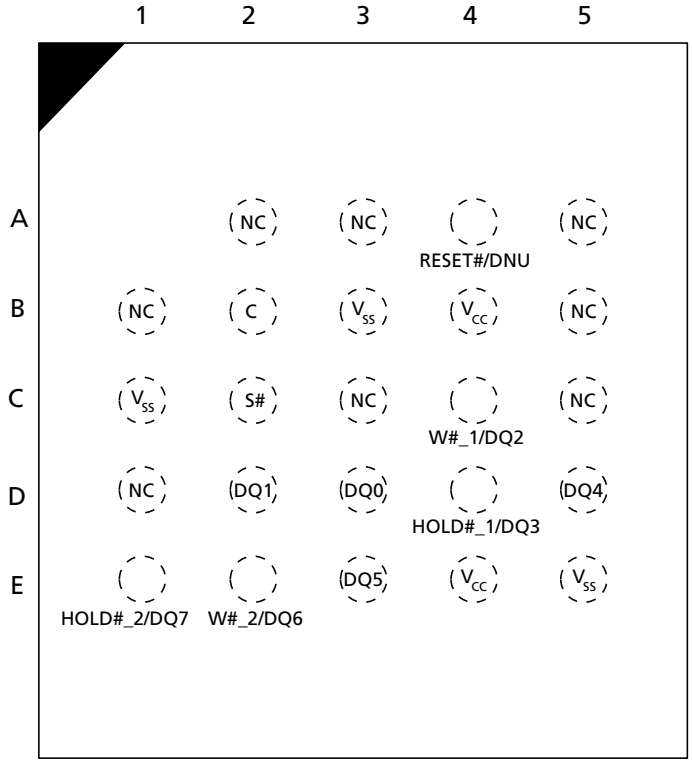
Notes:
1. RESET# or HOLD# signals can share Pin 1 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Figure 7: 16-Pin, Plastic Small Outline – SO16 (Top View) (Dual Chip-Select and Clock)



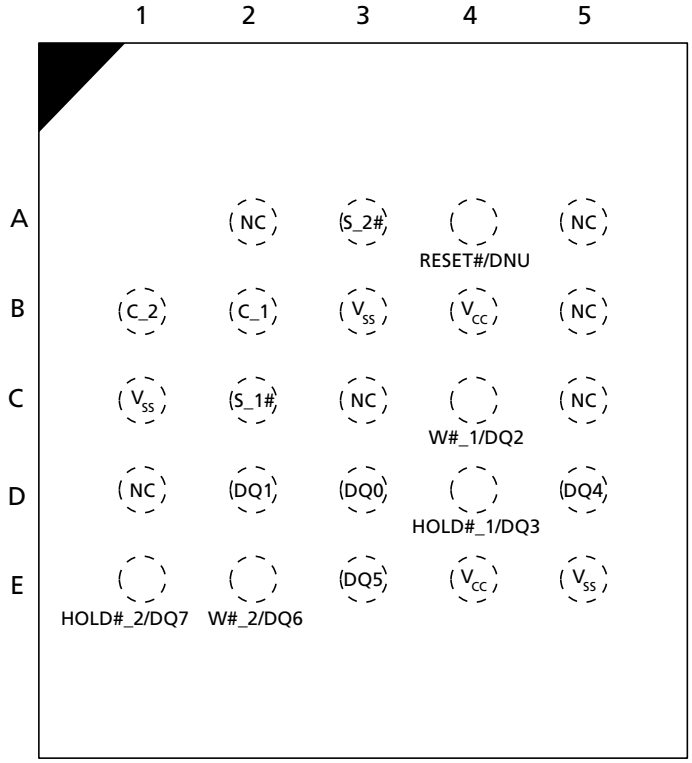
Notes:
1. RESET# or HOLD# signals can share Pin 1 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Figure 8: 24-Ball TBGA – 5 x 5 (Balls Down) (Single Chip-Select and Clock)



Notes:
1. RESET# or HOLD# signals can share Ball D4 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Ball A4 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Figure 9: 24-Ball TBGA – 5 x 5 (Balls Down) (Double Chip-Select and Clock)



Notes:
1. RESET# or HOLD# signals can share Ball D4 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Ball A4 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Descriptions

The signal description table below is a comprehensive list of signals for the MT25T family devices. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

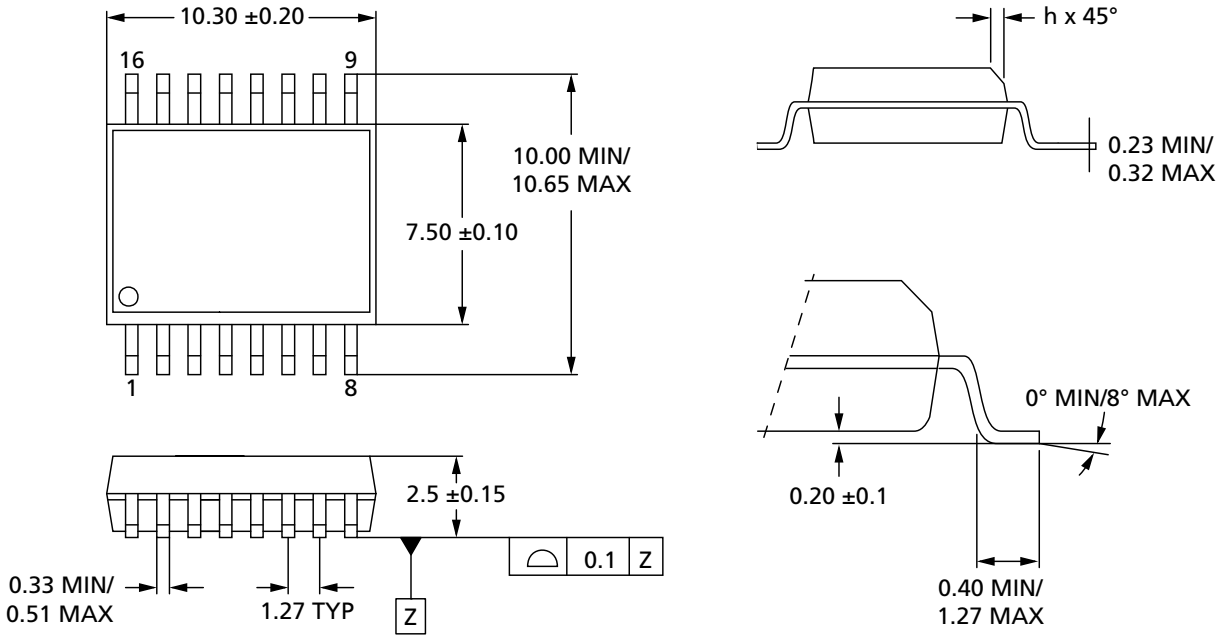
Symbol	Type	Description
C	Input	**Clock:** Provides the timing of the serial interface. Commands are latched on the rising edge of the clock. In STR commands or protocol, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DTR commands or protocol, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock. In single clock C configuration, C_1 and C_2 are connected together internally at package level.
C_1		Associated to die 1
C_2		Associated to die 2
S#	Input	**Chip select:** Because each die has its own DQ signals, each die can work independently. When S# is driven HIGH, the device enters standby mode, unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress. All other input pins are ignored and the output pins are tri-stated. On parts where the pin configuration offers a dedicated RESET# pin, however, the RESET# input pin remains active when S# is HIGH. Driving S# LOW enables the device, placing it in the active mode. After power-up, a falling edge on S# is required prior to the start of any command. In single S# configuration, S_1# and S_2# are connected together internally at package level.
S_1#		Associated to die 1
S_2#		Associated to die 2.
DQ[3:0], DQ[7:4]	I/O	**Serial data:** Bidirectional signals that transfer address, data, and command information. When using legacy (x1) SPI commands in extended I/O protocol (XIO-SPI), DQ0/DQ4 is an input and DQ1/DQ5 is an output. DQ[3:2]/DQ[7:6] are not used. When using dual commands in XIO SPI or when using DIO-SPI, DQ[1:0]/DQ[5:4] are I/O. DQ[3:2]/DQ[7:6] are not used. When using quad commands in XIO-SPI or when using QIO-SPI, DQ[3:0]/DQ[7:4] are I/O.
RESET#	Input	**RESET:** Hardware RESET# signal shared by both die. When RESET# is driven LOW, the device is reset and the outputs are tri-stated. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost. The RESET# functionality can be disabled using bit 4 of the nonvolatile configuration register or bit 4 of the enhanced volatile configuration register.The RESET# has an internal pull-up resistor and may be left floating if not used. For pin configurations that share the DQ3/DQ7 pins with RESET#, the RESET# functionality is disabled in QIO-SPI mode.
HOLD_1#, HOLD_2#	Input	**HOLD_1# (die 1), HOLD_2# (die 2):** Pauses any serial communications with the related die without deselecting the device. Outputs are tri-stated and inputs are ignored. To enable HOLD, the related die must be selected by its associated S# being driven LOW. In QIO-SPI, HOLD# acts as an I/O (DQ3/DQ7 functionality), and the HOLD# functionality is disabled when the device is selected. Because each die has its own nonvolatile configuration register, the HOLD# functionality for each die can be disabled using bit 4 of its associated nonvolatile configuration register or bit 4 of its associated enhanced volatile configuration register. HOLD# functionality is disabled in QIO-SPI mode or when DTR operation is enabled.

Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
W_1#, W_2#	Control Input	**Write protect:** W_1# (die 1) and W_2# (die 2) can be used as a protection control input or in QIO-SPI operations. When LOW, the blocks defined by the block protection bits BP[3:0] are protected against PROGRAM or ERASE operations. Status register bit 7 should be set to 1 to enable write protection.
V_{CC}	Supply	**Core and IO power supply:** All V_{CC} pins must be connected to system power supply.
V_{SS}	Supply	**Core and IO ground connection:** All V_{SS} pins must be connected to system ground.
DNU	–	Do not use. Must be left floating.
NC	–	No connect. Not internally connected.

Package Dimensions – Package Code: SF

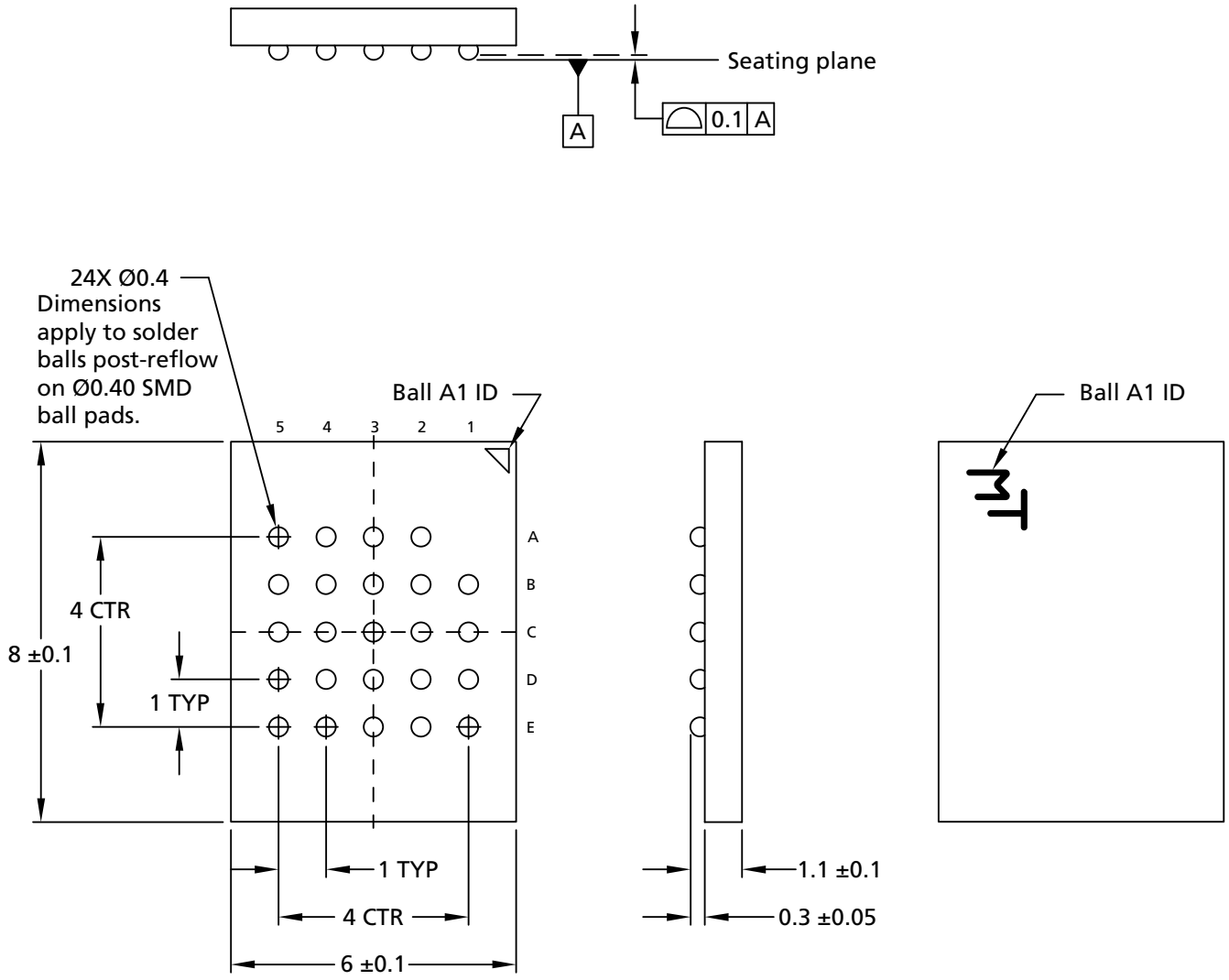
Figure 10: 16-Pin SOP2 – 300 mils Body Width



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: 12

Figure 11: 24-Ball T-PBGA (5 x 5 ball grid array) – 6mm x 8mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Memory Map – 512Mb Density

Table 2: Sectors[1023:0]

Sector	32KB Subsector	4KB Subsector	Address Range	
			Start	End
1023	2047	16383	03FF F000h	03FF FFFFh
		⋮	⋮	⋮
	2046	⋮	⋮	⋮
		16368	03FF 0000h	03FF 0FFFh
⋮		⋮	⋮	⋮
511	1023	8191	01FF F000h	01FF FFFFh
	1022	⋮	⋮	⋮
		8176	01FF 0000h	01FF 0FFFh
⋮		⋮	⋮	⋮
255	511	4095	00FF F000h	00FF FFFFh
		⋮	⋮	⋮
	510	⋮	⋮	⋮
		4080	00FF 0000h	00FF 0FFFh
⋮		⋮	⋮	⋮
0	1	15	0000 F000h	0000 FFFFh
		⋮	⋮	⋮
	0	⋮	⋮	⋮
		0	0000 0000h	0000 0FFFh

Note: 1. See Part Number Ordering Information, Sector Size–Part Numbers table for options.

Status Register

Status register bits can be read from or written to using READ STATUS REGISTER or WRITE STATUS REGISTER commands, respectively. When the status register enable/disable bit (bit 7) is set to 1 and W# is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. The only way to exit this hardware-protected mode is to drive W# HIGH.

Table 3: Status Register

Bit	Name	Settings	Description	Notes
7	Status register write enable/disable	0 = Enabled (default) 1 = Disabled	**Nonvolatile control bit:** Used with W# to enable or disable writing to the status register.	
5	Top/bottom	0 = Top (default) 1 = Bottom	**Nonvolatile control bit:** Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	
6, 4:2	BP[3:0]	See Protected Area tables	**Nonvolatile control bit:** Defines memory to be software protected against PROGRAM or ERASE operations. When one or more block protect bits is set to 1, a designated memory area is protected from PROGRAM and ERASE operations.	1
1	Write enable latch	0 = Clear (default) 1 = Set	**Volatile control bit:** The device always powers up with this bit cleared to prevent inadvertent WRITE, PROGRAM, or ERASE operations. To enable these operations, the WRITE ENABLE operation must be executed first to set this bit.	
0	Write in progress	0 = Ready 1 = Busy	**Status bit:** Indicates if one of the following command cycles is in progress: WRITE STATUS REGISTER WRITE NONVOLATILE CONFIGURATION REGISTER PROGRAM ERASE	2

Notes:
1. The DIE ERASE command is executed only if all bits = 0.
2. Status register bit 0 is the inverse of flag status register bit 7.

Block Protection Settings

Table 4: Protected Area

Status Register Content					Protected Area
Top/Bottom	BP3	BP2	BP1	BP0	64KB Sectors
0	0	0	0	0	None
0	0	0	0	1	1023:1023
0	0	0	1	0	1023:1022
0	0	0	1	1	1023:1020
0	0	1	0	0	1023:1016
0	0	1	0	1	1023:1008
0	0	1	1	0	1023:992
0	0	1	1	1	1023:960
0	1	0	0	0	1023:896
0	1	0	0	1	1023:768
0	1	0	1	0	1023:512
0	1	0	1	1	1023:0
0	1	1	0	0	1023:0
0	1	1	0	1	1023:0
0	1	1	1	0	1023:0
0	1	1	1	1	1023:0
1	0	0	0	0	None
1	0	0	0	1	0:0
1	0	0	1	0	1:0
1	0	0	1	1	3:0
1	0	1	0	0	7:0
1	0	1	0	1	15:0
1	0	1	1	0	31:0
1	0	1	1	1	63:0
1	1	0	0	0	127:0
1	1	0	0	1	255:0
1	1	0	1	0	511:0
1	1	0	1	1	1023:0
1	1	1	0	0	1023:0
1	1	1	0	1	1023:0
1	1	1	1	0	1023:0
1	1	1	1	1	1023:0

Flag Status Register

Flag status register bits are read by using READ FLAG STATUS REGISTER command. All bits are volatile and are reset to zero on power up.

Status bits are set and reset automatically by the internal controller. Error bits must be cleared through the CLEAR STATUS REGISTER command.

Table 5: Flag Status Register

Bit	Name	Settings	Description
7	Program or erase controller	0 = Busy 1 = Ready	**Status bit:** Indicates whether one of the following command cycles is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE.
6	Erase suspend	0 = Clear 1 = Suspend	**Status bit:** Indicates whether an ERASE operation has been or is going to be suspended.
5	Erase	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE operation has succeeded or failed.
4	Program	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether a PROGRAM operation has succeeded or failed. It indicates, also, whether a CRC check has succeeded or failed.
3	Reserved	0	Reserved
2	Program suspend	0 = Clear 1 = Suspend	**Status bit:** Indicates whether a PROGRAM operation has been or is going to be suspended.
1	Protection	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.
0	Addressing	0 = 3-byte addressing 1 = 4-byte addressing	**Status bit:** Indicates whether 3-byte or 4-byte address mode is enabled.

Extended Address Register

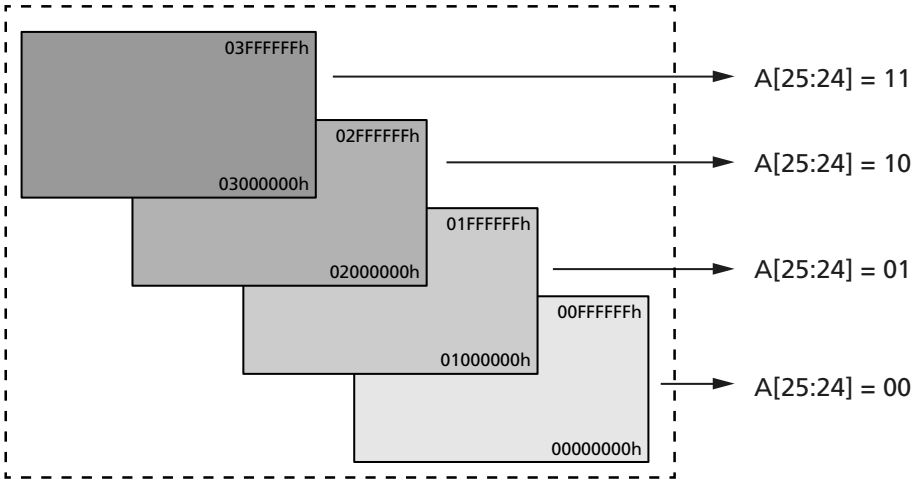
The 3-byte address mode can only access 128Mb of memory. To access the full device in 3-byte address mode, the device includes an extended address register that indirectly provides a fourth address byte A[31:24]. The extended address register bits [1:0] operate as memory address bit A[25:24] to select one of the four 128Mb segments of the memory array.

If 4-byte addressing is enabled, the extended address register settings are ignored.

Table 6: Extended Address Register

Bit	Name	Settings	Description
7:2	A[31:26]	000000	Reserved
1:0	A[25:24]	11 = Highest 128Mb segment 10 = Third 128Mb segment 01 = Second 128Mb segment 00 = Lowest 128Mb segment (default)	Enables specified 128Mb memory segment. The default (lowest) setting can be changed to the highest 128Mb segment using bit 1 of the nonvolatile configuration register.

Figure 12: Memory Array Segments



The PROGRAM and ERASE operations act upon the 128Mb segment selected in the extended address register. The BULK ERASE operation erases the entire device.

The READ operation begins reading in the selected 128Mb segment, but is not bound by it.

In a continuous READ, when the last byte of the segment is read, the next byte output is the first byte of the next segment. The operation wraps to 0000000h; therefore, a download of the whole array is possible with one READ operation.

The value of the extended address register does not change when a READ operation crosses the selected 128Mb boundary.

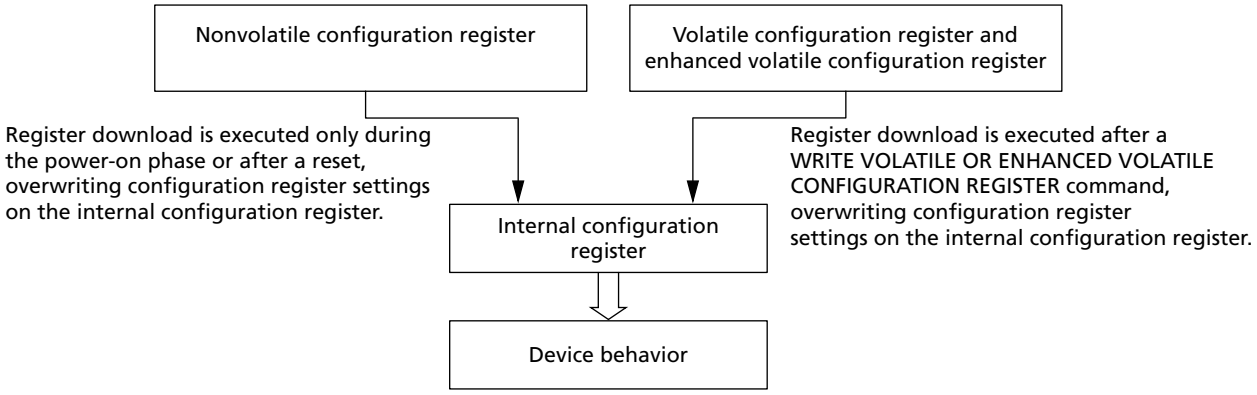
Internal Configuration Register

The memory configuration is set by an internal configuration register that is not directly accessible to users.

The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset.

The user can change the configuration during operation by using the WRITE VOLATILE CONFIGURATION REGISTER or the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER commands. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.

Figure 13: Internal Configuration Register



Nonvolatile Configuration Register

This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. A register download is executed during power-on or after reset, overwriting the internal configuration register settings that determine device behavior.

Table 7: Nonvolatile Configuration Register

Bit	Name	Settings	Description	Notes
15:12	Number of dummy clock cycles	0000 = Identical to 1111 0001 = 1 0010 = 2 ⋮ 1101 = 13 1110 = 14 1111 = Default	Sets the number of dummy clock cycles subsequent to all FAST READ commands. (See the Command Set Table for default setting values.)	1
11:9	XIP mode at power-on reset	000 = XIP: Fast read 001 = XIP: Dual output fast read 010 = XIP: Dual I/O fast read 011 = XIP: Quad output fast read 100 = XIP: Quad I/O fast read 101 = Reserved 110 = Reserved 111 = Disabled (default)	Enables the device to operate in the selected XIP mode immediately after power-on reset.	
8:6	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = Reserved 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = Reserved 111 = 30 Ohms (default)	Optimizes the impedance at V_{CC}/2 output voltage.	
5	Double transfer rate protocol	0 = Enabled 1 = Disabled (default)	Set DTR protocol as current one. Once enabled, all commands will work in DTR.	
4	Reset/hold	0 = Disabled 1 = Enabled (default)	Enables or disables HOLD# or RESET# on DQ3.	
3	Quad I/O protocol	0 = Enabled 1 = Disabled (default)	Enables or disables quad I/O command input (4-4-4 mode).	2
2	Dual I/O protocol	0 = Enabled 1 = Disabled (default)	Enables or disables dual I/O command input (2-2-2 mode).	2
1	128Mb segment select	0 = Highest 128Mb segment 1 = Lowest 128Mb segment (default)	Selects the power-on default 128Mb segment for 3-byte address operations. See also the extended address register.	

Table 7: Nonvolatile Configuration Register (Continued)

Bit	Name	Settings	Description	Notes
0	Number of address bytes during command entry	0 = Enable 4-byte address mode 1 = Enable 3-byte address mode (default)	Defines the number of address bytes for a command.	

Notes:
1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ command (See Supported Clock Frequencies table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data.
2. When bits 2 and 3 are both set to 0, the device operates in quad I/O protocol.