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Q-FLASH® MEMORY

MT28F128J3, MT28F640J3, MT28F320J3

Features

Memory Organization
- x8/x16
- One hundred twenty-eight 128KB erase blocks (128Mb)
- Sixty-four 128KB erase blocks (64Mb)
- Thirty-two 128KB erase blocks (32Mb)

V_{CC}, $V_{CC}Q$, and V_{PEN} voltages:
- 2.7V to 3.6V V_{CC} operation
- 2.7V to 3.6V application programming

Interface Asynchronous Page Mode Reads:
- 120ns/25ns read access time (128Mb)
- 115ns/25ns read access time (64Mb)
- 110ns/25ns read access time (32Mb)

Manufacturer's Identification Code (ManID)
- Micron® (0x2Ch)
- Intel® (0x89h)

Industry-standard pinout

Inputs and outputs are fully TTL-compatible

Common Flash Interface (CFI) and Scalable Command Set

Automatic write and erase algorithm

5.6µs-per-byte effective programming time using write buffer

128-bit protection register
- 64-bit unique device identifier
- 64-bit user-programmable OTP cells

Enhanced data protection feature with $V_{PEN} = V_{SS}$
- Flexible sector locking
- Sector erase/program lockout during power transition

Security block features
Contact factory for availability

100,000 ERASE cycles per block

Automatic suspend options:
- Block Erase Suspend-to-Read
- Block Erase Suspend-to-Program
- Program Suspend-to-Read

Figure 1: 56-Pin TSOP Type I

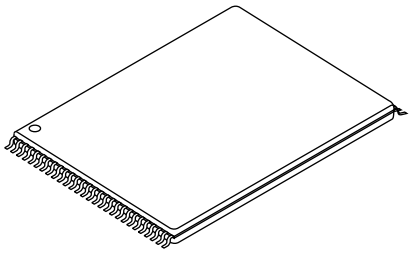
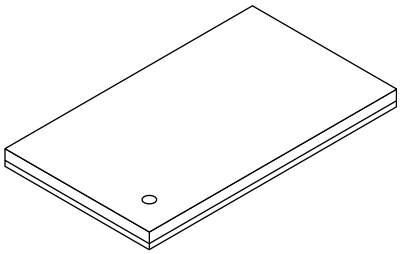


Figure 2: 64-Ball FBGA



Options	Mark
Timing	
• 110ns (32Mb)	-11
• 115ns (64Mb)	-115
• 120ns (128Mb)	-12
Operating Temperature Range	
• Extended Temperature: -40°C to +85°C	ET
Packages	
• 56-pin (standard) TSOP Type I	RG
• 56-pin (lead-free) TSOP Type I	RP
• 64-ball (standard) FBGA (1.00mm pitch)	FS
• 64-ball (lead-free) FBGA (1.00mm pitch)	BS
Manufacturer's Identification Code (ManID)	
• Micron (0x2Ch)	M
• Intel (0x89h)	

Part Number Example:
MT28F640J3RG-115ET

Table of Contents

List of Figures

List of Tables

General Description

The MT28F128J3 is a nonvolatile, electrically block-erasable (Flash), programmable memory containing 134,217,728 bits organized as 16,777,218 bytes (8 bits) or 8,388,608 words (16 bits). This 128Mb device is organized as one hundred twenty-eight 128KB erase blocks.

The MT28F640J3 contains 67,108,864 bits organized as 8,388,608 bytes (8 bits) or 4,194,304 words (16 bits). This 64Mb device is organized as sixty-four 128KB erase blocks.

Similarly, the MT28F320J3 contains 33,554,432 bits organized as 4,194,304 bytes (8 bits) or 2,097,152 words (16 bits). This 32Mb device is organized as thirty-two 128KB erase blocks.

These three devices feature in-system block locking. They also have common Flash interface (CFI) that permits software algorithms to be used for entire families of devices. The software is device-independent, JEDEC ID-independent with forward and backward compatibility.

Additionally, the scalable command set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant Flash memory devices. The SCS provides the fastest system/device data transfer rates and minimizes the device and system-level implementation costs.

To optimize the processor-memory interface, the device accommodates V_{PEN}, which is switchable during block erase, program, or lock bit configuration, or hard-wired to V_{CC}, depending on the application. V_{PEN} is treated as an input pin to enable erasing, programming, and block locking. When V_{PEN} is lower than the V_{CC} lockout voltage (V_{LKO}), all program functions are disabled. Block erase suspend mode enables the user to stop block erase to read data from or program data to any other blocks. Similarly, program suspend mode enables the user to suspend programming to read data or execute code from any unsuspended blocks.

V_{PEN} serves as an input with 2.7V or 3.3V for application programming. V_{PEN} in this Q-Flash® family can provide data protection when connected to ground. This pin also enables program or erase lockout during power transition.

Micron's even-sectored Q-Flash devices offer individual block locking that can lock and unlock a block using the sector lock bits command sequence.

Status (STS) is a logic signal output that gives an additional indicator of the internal state machine (ISM) activity by providing a hardware signal of both status and status masking. This status indicator minimizes central processing unit (CPU) overhead and system power consumption. In the default mode, STS acts as an RY/BY# pin. When LOW, STS indicates that the ISM is performing a block erase, program, or lock bit configuration. When HIGH, STS indicates that the ISM is ready for a new command.

Three chip enable (CE) pins are used for enabling and disabling the device by activating the device's control logic, input buffer, decoders, and sense amplifiers.

BYTE# enables the device to be used in x8 or x16 read/write mode; BYTE# = 0 selects an 8-bit mode, with address A0 selecting between the LOW and HIGH byte, while BYTE# = 1 selects a 16-bit mode. When BYTE# = 1, A1 becomes the lowest-order address line with A0 being a no connect.

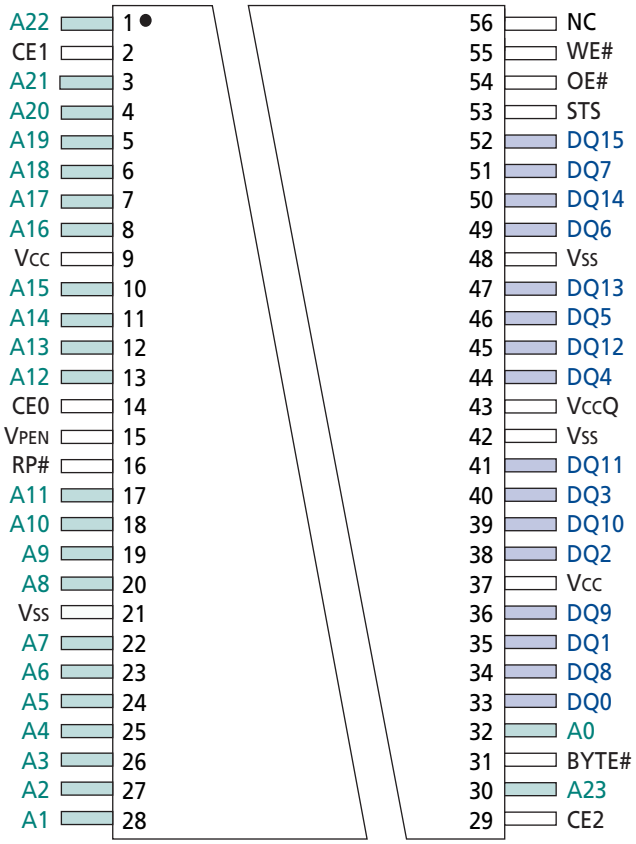
RP# is used to reset the device. When the device is disabled and RP# is at V_{CC}, the standby mode is enabled. A reset time (^{t}RWH) is required after RP# switches HIGH until outputs are valid. Likewise, the device has a wake time (^{t}RS) from RP# HIGH until writes to the command user interface (CUI) are recognized. When RP# is at GND, it provides write protection, resets the ISM, and clears the status register.

Variants of the MT28F320J3 and MT28F640J3 support the new security block lock features for additional code security. (Contact factory for availability.)

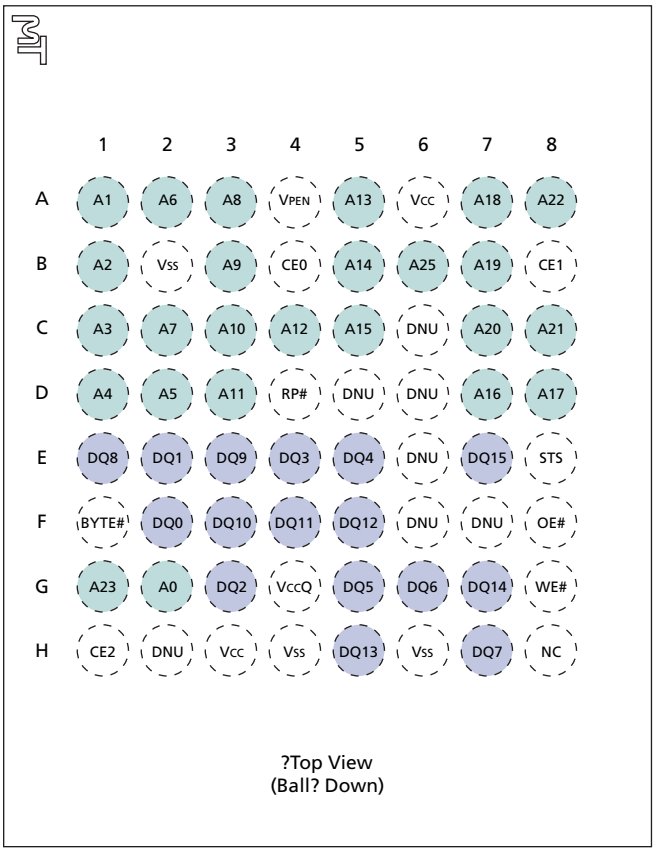
The MT28F320J3 is manufactured using 0.18µm process technology, the MT28F128J3 and the MT28F640J3 are manufactured using 0.15µm process technology.

Figure 3: Pin and Ball Assignment Diagrams

56-Pin TSOP Type I



64-Ball FBGA



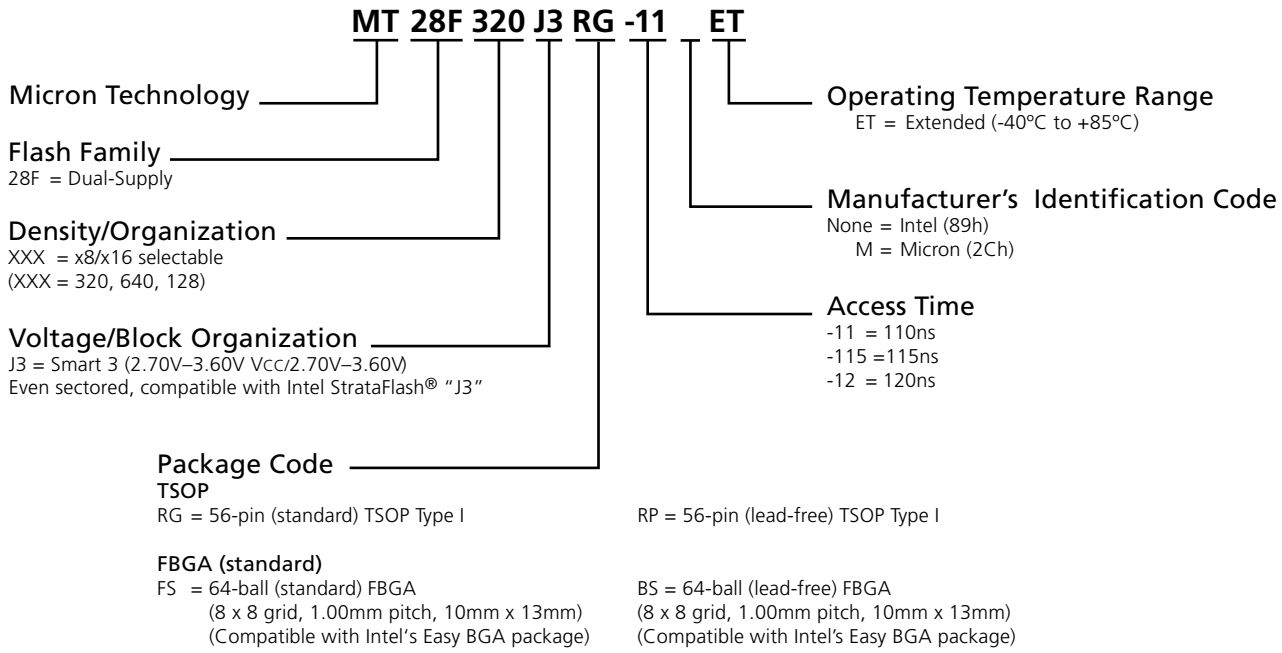
NOTE:

1. A22 only exists on the 64Mb and 128Mb devices. On the 32Mb, this pin/ball is a no connect (NC).
2. A23 only exists on the 128Mb device. On the 32Mb and 64Mb, this pin/ball is NC.
3. The # symbol indicates that the signal is active LOW.

Part Numbering Information

Micron's Flash devices are available with several different combinations of features (see Figure 4).

Figure 4: Part Number Chart



NOTE:

1. Lead-free packages are available. Contact factory for details.

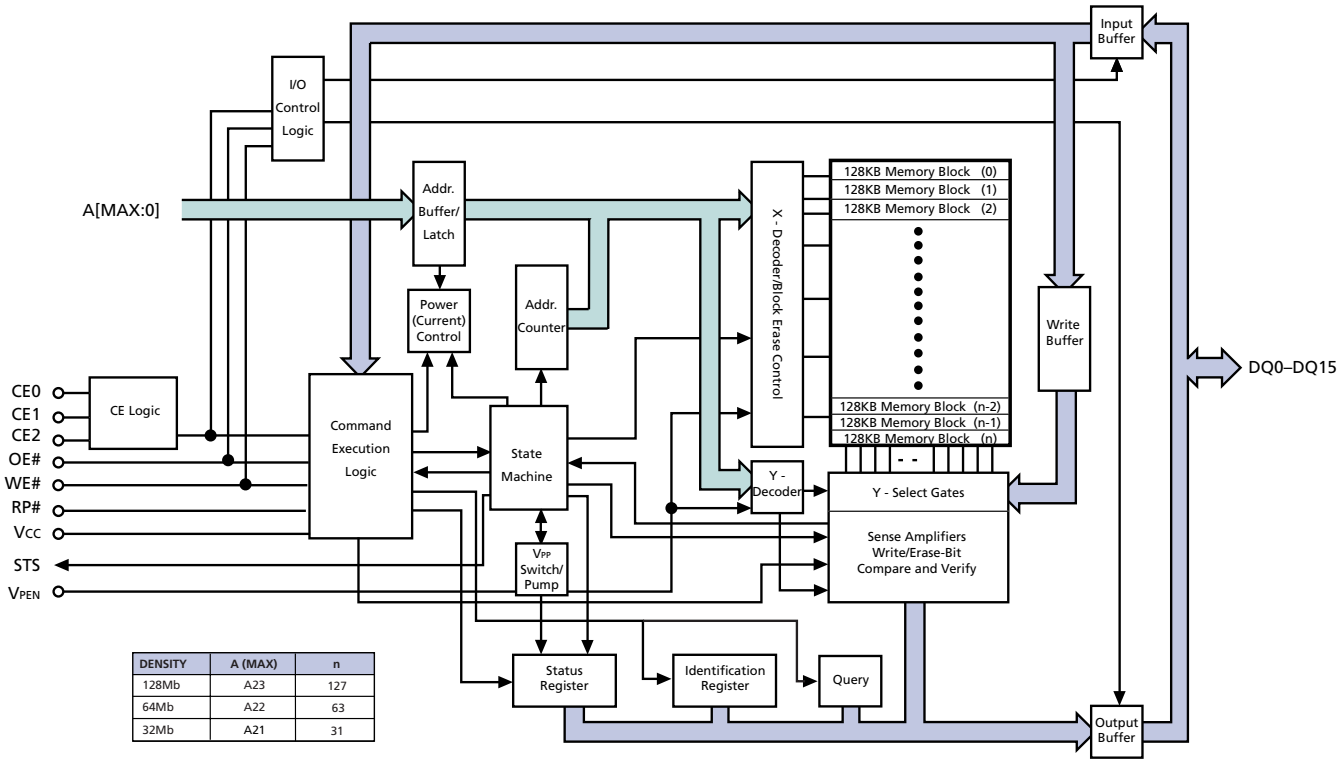
Valid Part Number Combinations

After building the part number from the part number chart above, please go to Micron's Part Marking Decoder Web site at www.micron.com/partsearch to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.

Device Marking

Due to the size of the package, the Micron standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at www.micron.com/partsearch. To view the location of the abbreviated mark on the device, please refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

Figure 5: Functional Block Diagram



DENSITY	A (MAX)	n
128Mb	A23	127
64Mb	A22	63
32Mb	A21	31

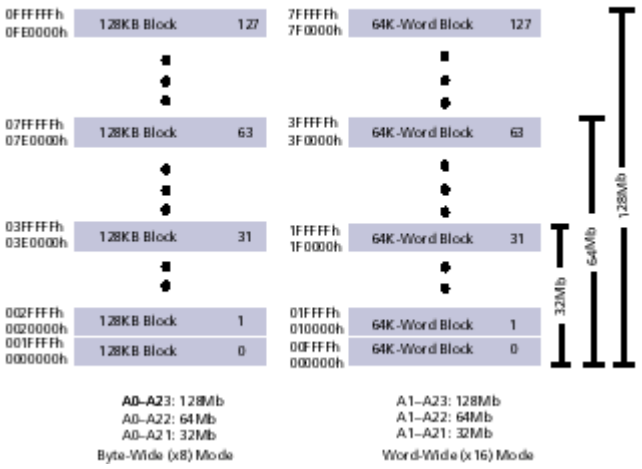
Table 1: Pin/Ball Descriptions

56-PIN TSOP NUMBERS	64-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
55	G8	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array. Addresses and data are latched on the rising edge of the WE# pulse.
14, 2, 29	B4, B8, H1	CE0, CE1, CE2	Input	Chip Enable: Three CE pins enable the use of multiple Flash devices in the system without requiring additional logic. The device can be configured to use a single CE signal by tying CE1 and CE2 to ground and then using CE0 as CE. Device selection occurs with the first edge of CE0, CE1, or CE2 (CEx) that enables the device. Device deselection occurs with the first edge of CEx that disables the device (see Table 2 on page 11).
16	D4	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the ISM to the array read mode, and places the device in deep power-down mode. All inputs, including CEx, are "Don't Care," and all outputs are High-Z. RP# must be held at V_{IH} during all other modes of operation.
54	F8	OE#	Input	Output Enables: Enables data ouput buffers when LOW. When OE# is HIGH, the output buffers are disabled.
32, 28, 27, 26, 25, 24, 23, 22, 20, 19, 18, 17, 13, 12, 11, 10, 8, 7, 6, 5, 4, 3, 1, 30	G2, A1, B1, C1, D1, D2, A2, C2, A3, B3, C3, D3, C4, A5, B5, C5, D7, D8, A7, B7, C7, C8, A8, G1	A0–A21/ (A22) (A23)	Input	Address inputs during READ and WRITE operations. A0 is only used in x8 mode and will be a NC in x16 mode (the input buffer is turned off when BYTE = HIGH). A22 (pin 1, ball A8) is only available on the 64Mb and 128Mb devices. A23 (pin 30, ball G1) is only available on the 128Mb device.
31	F1	BYTE#	Input	BYTE# low places the device in the x8 mode. BYTE# high places the device in the x16 mode and turns off the A0 input buffer. Address A1 becomes the lowest order address in x16 mode.
15	A4	V_{PEN}	Input	Necessary voltage for erasing blocks, programming data, or configuring lock bits. Typically, V_{PEN} is connected to V_{CC}. When $V_{PEN} \leq V_{PENLK}$, this pin enables hardware write protect.
33, 35, 38, 40, 44, 46, 49, 51, 34, 36, 39, 41, 45, 47, 50, 52	F2, E2, G3, E4, E5, G5, G6, H7, E1, E3, F3, F4, F5, H5, G7, E7	DQ0–DQ15	Input/ Output	Data I/O: Data output pins during any READ operation or data input pins during a WRITE. DQ8–DQ15 are not used in byte mode (BYTE = LOW).
53	E8	STS	Output	Status: Indicates the status of the ISM. When configured in level mode (default), STS acts as a RY/BY# pin. When configured in its pulse mode, it can pulse to indicate program and/or erase completion. Tie STS to V_{CCQ} through a pull-up resistor.
43	G4	V_{CCQ}	Supply	V_{CCQ} controls the output voltages. To obtain output voltage compatible with system data bus voltages, connect V_{CCQ} to the system supply voltage.
9, 37	H3, A6	V_{CC}	Supply	Power Supply: 2.7V to 3.6V.
21, 42, 48	B2, H4, H6	V_{SS}	Supply	Ground.
1, 30, 56	A1, G1, H8	NC	—	No Connect: These may be driven or left unconnected. Pin 1 and ball A8 are NCs on the 32Mb device. Pin 30 and ball G1 are NCs on the 32Mb and 64Mb devices.
—	B6, C6, D5, D6, E6, F6, F7, H2	DNU	—	Do Not Use: Must float to minimize noise.

Memory Architecture

The MT28F128J3, MT28F640J3, and MT28F320J3 memory array architecture is divided into one hundred twenty-eight, sixty-four, or thirty-two 128KB blocks, respectively (see Figure 6). The internal architecture allows greater flexibility when updating data because individual code portions can be updated independently of the rest of the code.

Figure 6: Memory Map



Read

Information can be read from any block, query, identifier codes, or status register, regardless of the VPEN voltage. The device automatically resets to read array mode upon initial device power-up or after exit from reset/power-down mode. To access other read mode commands (READ ARRAY, READ QUERY, READ IDENTIFIER CODES, or READ STATUS REGISTER), these commands should be issued to the CUI. Six control pins dictate the data flow in and out of the device: CE0, CE1, CE2, OE#, WE#, and RP#. In system designs using multiple Q-Flash devices, CE0, CE1, and CE2 (CEx) select the memory device (see Table 2). To drive data out of the device and onto the I/O bus, OE# must be active and WE# must be inactive (VIH).

Table 2: Chip-Enable Truth Table

CE2	CE1	CE0	DEVICE
VIL	VIL	VIL	Enabled
VIL	VIL	VIH	Disabled
VIL	VIH	VIL	Disabled
VIL	VIH	VIH	Disabled
VIH	VIL	VIL	Enabled
VIH	VIL	VIH	Enabled
VIH	VIH	VIL	Enabled
VIH	VIH	VIH	Disabled

NOTE:
For single-chip applications, CE2 and CE1 can be connected to GND.

When reading information in read array mode, the device defaults to asynchronous page mode, thus providing a high data transfer rate for memory subsystems. In this state, data is internally read and stored in a high-speed page buffer. A0–A2 select data in the page buffer. Asynchronous page mode, with a page size of four words or eight bytes, is supported with no additional commands required and can be used to access all blocks. Page mode can be used to access register information, but only one word is loaded into the page buffer.

Output Disable

The device outputs are disabled with OE# at a logic HIGH level (VIH). Output pins DQ0–DQ15 are placed in High-Z.

Standby

CE0, CE1, and CE2 can disable the device (see Table 2) and place it in standby mode, which substantially reduces device power consumption. DQ0–DQ15 outputs are placed in High-Z, independent of OE#. If deselected during block erase, program, or lock bit configuration, the ISM continues functioning and consuming active power until the operation completes.

Reset/Power-Down

RP# puts the device into the reset/power-down mode when set to VIL.

During read, RP# LOW deselects the memory, places output drivers in High-Z, and turns off internal circuitry. RP# must be held LOW for a minimum of ^{t}PLPH. ^{t}RWH is required after return from reset mode until initial memory access outputs are valid. After this

wake-up interval, normal operation is restored. The command execution logic (CEL) is reset to the read array mode and the status register is set to 80h.

During block erase, program, or lock bit configuration, RP# LOW aborts the operation. In default mode, STS transitions LOW and remains LOW for a maximum time of ^{t}PLPH + ^{t}PHRH, until the RESET operation is complete. Any memory content changes are no longer valid; the data may be partially corrupted after a program or partially changed after an erase or lock bit configuration. After RP# goes to logic HIGH (V_{IH}), and after ^{t}RS, another command can be written.

It is important to assert RP# during system reset. After coming out of reset, the system expects to read from the Flash memory. During block erase, program, or lock bit configuration mode, automated Flash memories provide status information when accessed. When a CPU reset occurs with no Flash memory reset, proper initialization may not occur because the Flash memory may be providing status information instead of array data. Micron Flash memories allow proper initialization following a system reset through the use of the RP# input. RP# should be controlled by the same RESET# signal that resets the system CPU.

Read Query

The READ QUERY operation produces block status information, CFI ID string, system interface information, device geometry information, and extended query information. READ QUERY information is only accessed by executing a single-word READ.

Read Identifier Codes

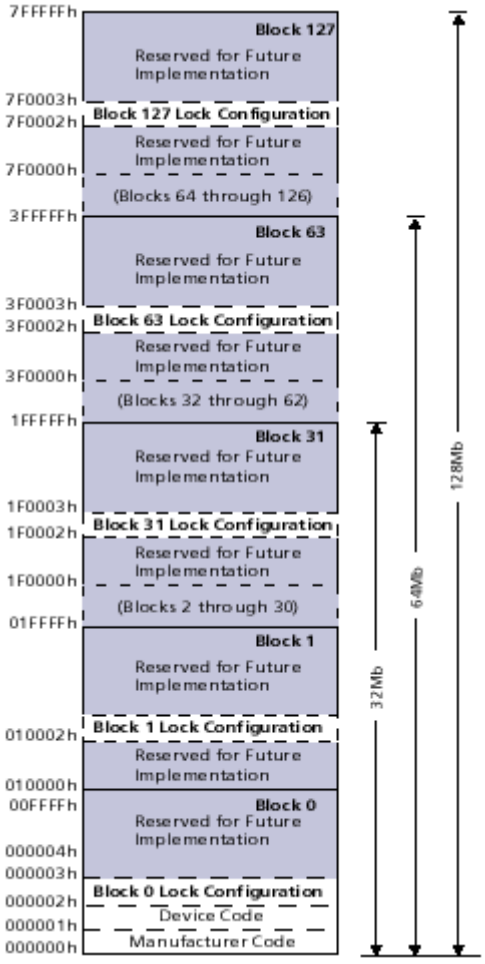
The READ IDENTIFIER CODES operation produces the manufacturer code, device code, and the block lock configuration codes for each block (see Figure 7). The block lock configuration codes identify locked and unlocked blocks.

Write

Writing commands to the CEL allows reading of device data, query, identifier codes, and reading and clearing of the status register. In addition, when V_{PEN} = V_{PENH}, block erasure, program, and lock bit configuration can also be performed.

The BLOCK ERASE command requires suitable command data and an address within the block. The BYTE/WORD PROGRAM command requires the command and address of the location to be written to. The CLEAR BLOCK LOCK BITS command requires the command and any address within the device. Set BLOCK LOCK BITS command requires the command and the block to be locked. The CEL does not occupy an addressable memory location. It is written to when the device is enabled and WE# is LOW. The address and data needed to execute a command are latched on the rising edge of WE# or the first edge of CEx that disables the device (see Table 2 on page 11). Standard microprocessor write timings are used.

Figure 7: Device Identifier Code Memory Map



NOTE:

When obtaining these identifier codes, A0 is not used in either x8 or x16 modes. Data is always given on the LOW byte in x16 mode (upper byte contains 00h).

Bus Operation

All bus cycles to and from the Flash memory must conform to the standard microprocessor bus cycles. The local CPU reads and writes Flash memory in-system.

Table 3: Bus Operations

MODE	RP#	CE0, CE1, CE2[1]	OE#[2]	WE#[2]	ADDRESS	VPEN	DQ[3]	STS DEFAULT MODE	NOTES
Read Array	VIH	Enabled	VIL	VIH	X	X	DOUT	High-Z[4]	5, 6, 7
Output Disable	VIH	Enabled	VIH	VIH	X	X	High-Z	X	
Standby	VIH	Disabled	X	X	X	X	High-Z	X	
Reset/Power-down Mode	VIL	X	X	X	X	X	High-Z	High-Z[4]	
Read Identifier Codes	VIH	Enabled	VIL	VIH	See Figure 7	X		High-Z[4]	8
Read Query	VIH	Enabled	VIL	VIH	See Table 7	X		High-Z[4]	9
Read Status (ISM off)	VIH	Enabled	VIL	VIH	X	X			
Read Status (ISM On) DQ 7 DQ15–DQ8 DQ6–DQ0	VIH	Enabled	VIL	VIH	X	X	 DOUT High-Z High-Z		
Write	VIH	Enabled	VIH	VIL	X	VPENH	DIN	X	7, 10, 11

NOTE:

1. See Table 2 on page 11 for valid CE configurations.
2. OE# and WE# should never be enabled simultaneously.
3. DQ refers to DQ0–DQ7 if BYTE# is LOW and DQ0–DQ15 if BYTE# is HIGH.
4. High-Z is VOH with an external pull-up resistor.
5. When Vpen £ Vpenlk, memory contents can be read, but not altered. Refer to the Recommended DC Electrical Characteristics table on page 43.
6. X can be VIL or VIH for control and address pins, and VPENLK or VPENH for VPEN. See DC Characteristics for VPENLK and VPENH voltages.
7. In default mode, STS is VOL when the ISM is executing internal block erase, program, or lock bit configuration algorithms. It is VOH when the ISM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or reset/power-down mode.
8. See Read Identifier Codes section for read identifier code data.
9. See Read Query Mode Command section for read query data.
10. Command writes involving block erase, program, or lock bit configuration are reliably executed when VPEN = VPENH and VCC is within specification.
11. Refer to Table 4 on page 14 for valid DIN during a WRITE operation.

Command Definitions

When the Vpen voltage is < Vpenlk, only READ operations from the status register, query, identifier codes, or blocks are enabled. Placing Vpenh on Vpen enables BLOCK ERASE, PROGRAM, and LOCK BIT CONFIGURATION operations. Device operations are selected by writing specific commands into the CEL, as seen in Table 4.

Table 4: Micron Q-Flash Memory Command Set Definitions

Note 1; notes appear on following page

COMMAND	SCALABLE OR BASIC COMMAND SET[2]	BUS CYCLES REQ'D	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTES
			OPER[3]	ADDR[4]	DATA[5, 6]	OPER[3]	ADDR[4]	DATA[5, 6]	
READ ARRAY	SCS/BCS	1	WRITE	X	FFh				
READ IDENTIFIER CODES	SCS/BCS	≥2	WRITE	X	90h	READ	IA	ID	7
READ QUERY	SCS	≥2	WRITE	X	98h	READ	QA	QD	
READ STATUS REGISTER	SCS/BCS	2	WRITE	X	70h	READ	X	SRD	8
CLEAR STATUS REGISTER	SCS/BCS	1	WRITE	X	50h				
WRITE TO BUFFER	SCS/BCS	> 2	WRITE	BA	E8h	WRITE	BA	N	9, 10, 11
WORD/BYTE PROGRAM	SCS/BCS	2	WRITE	X	40h or 10h	WRITE	PA	PD	12, 13
BLOCK ERASE	SCS/BCS	2	WRITE	BA	20h	WRITE	BA	D0h	11, 12
BLOCK ERASE/ PROGRAM SUSPEND	SCS/BCS	1	WRITE	X	B0h				14
BLOCK ERASE/ PROGRAM RESUME	SCS/BCS	1	WRITE	X	D0h				12
CONFIGURATION	SCS	2	WRITE	X	B8h	WRITE	X	CC	
SET BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	BA	01h	
CLEAR BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	X	D0h	
PROTECTION PROGRAM		2	WRITE	X	C0h	WRITE	PA	PD	

NOTE:

1. Commands other than those shown in Table 4 on page 14 are reserved for future device implementations and should not be used.
2. The SCS is also referred to as the extended command set.
3. Bus operations are defined in Table 3 on page 13.
4. X = Any valid address within the device
   BA = Address within the block
   IA = Identifier code address; see Figure 7 on page 12 and Table 16 on page 23
   QA = Query data base address
   PA = Address of memory location to be programmed
5. ID = Data read from identifier codes
   QD = Data read from query data base
   SRD = Data read from status register; see Table 17 on page 24 for a description of the status register bits
   PD = Data to be programmed at location PA; data is latched on the rising edge of WE#
   CC = Configuration code
6. The upper byte of the data bus (DQ8–DQ15) during command WRITEs is a "Don't Care" in x16 operation.
7. Following the READ IDENTIFIER CODES command, READ operations access manufacturer, device, and block lock codes. See Block Status Register section for read identifier code data.
8. If the ISM is running, only DQ7 is valid; DQ15–DQ8 and DQ6–DQ0 are placed in High-Z.
9. After the WRITE-to-BUFFER command is issued, check the XSR to make sure a buffer is available for writing.
10. The number of bytes/words to be written to the write buffer = *n* + 1, where *n* = byte/word count argument. Count ranges on this device for byte mode are *n* = 00h to *n* = 1Fh and for word mode, *n* = 0000h to *n* = 000Fh. The third and consecutive bus cycles, as determined by *n*, are for writing data into the write buffer. The CONFIRM command (D0h) is expected after exactly *n* + 1 WRITE cycles; any other command at that point in the sequence aborts the WRITE-to-BUFFER operation. Please see Figure 9 on page 31, WRITE-to-BUFFER Flowchart, for additional information.
11. The WRITE-to-BUFFER or ERASE operation does not begin until a CONFIRM command (D0h) is issued.
12. Attempts to issue a block erase or program to a locked block will fail.
13. Either 40h or 10h is recognized by the ISM as the byte/word program setup.
14. Program suspend can be issued after either the WRITE-to-BUFFER or WORD/BYTE PROGRAM operation is initiated. The CLEAR BLOCK LOCK BITS operation simultaneously clears all block lock bits.

READ ARRAY Command

The device defaults to read array mode upon initial device power-up and after exiting reset/power-down mode. The read configuration register defaults to asynchronous read page mode. Until another command is written, the READ ARRAY command also causes the device to enter read array mode. When the ISM has started a block erase, program, or lock bit configuration, the device does not recognize the READ ARRAY command until the ISM completes its operation, unless the ISM is suspended via an ERASE or PROGRAM SUSPEND command. The READ ARRAY command functions independently of the VPEN voltage.

READ QUERY MODE Command

This section is related to the definition of the data structure or "data base" returned by the CFI QUERY command. System software should retain this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. When this information has been obtained, the software knows which command sets to use to enable Flash writes or block erases, and otherwise control the Flash component.

Query Structure Output

The query "data base" enables system software to obtain information about controlling the Flash component. The device's CFI-compliant interface allows the host system to access query data. Query data are always located on the lowest-order data outputs (DQ0–DQ7) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the query table device starting address is a 10h, which is a word address for x16 devices.

For a x16 organization, the first two bytes of the query structure, "Q" and "R" in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00h data on upper bytes, thus making the device output ASCII "Q" on the LOW byte (DQ7–DQ0) and 00h on the HIGH byte (DQ15–DQ8). At query addresses containing two or more bytes of information, the least significant data byte is located at the lower address, and the most significant data byte is located at the higher address. This is summarized in Table 5. A more detailed example is provided in Table 6.

Table 5: Summary of Query-Structure Output as a Function of Device and Mode

DEVICE TYPE/MODE	QUERY START LOCATION IN MAXIMUM DEVICE BUS WIDTH ADDRESSES	QUERY DATA WITH MAXIMUM DEVICE BUS WIDTH ADDRESSING			QUERY DATA WITH BYTE ADDRESSING		
		HEX OFFSET	HEX CODE	ASCII VALUE	HEX OFFSET	HEX CODE	ASCII VALUE
x16 device x16 mode	10h	10 11 12	0051 0052 0059	Q R Y	20 21 22	51 00 52	Q Null R
x16 device x8 mode	N/A[1]	N/A[1]			20 21 22	51 51 52	Q Q R

NOTE:

1. The system must drive the lowest-order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing where these lower addresses are not toggled by the system is "Not Applicable" for x8-configured devices.

Query Structure Overview

The QUERY command makes the Flash component display the CFI query structure or data base. The structure subsections and address locations are outlined in Table 7.

Table 6: Example: Query Structure Output of x16- and x8-Capable Devices

WORD ADDRESSING			BYTE ADDRESSING		
OFFSET[1]	HEX CODE	VALUE	OFFSET	HEX CODE	VALUE
A16–A1	DQ15–DQ0		A7–A0	DQ7–DQ0	
0010h	0051	Q	20h	51	Q
0011h	0052	R	21h	51	Q
0012h	0059	Y	22h	52	R
0013h	P_ID LO	PrVendor	23h	52	R
0014h	P_ID HI	ID#	24h	59	Y
0015h	P LO	PrVendor	25h	59	Y
0016h	P HI	TblAdr	26h	P_ID LO	PrVendor
0017h	A_ID LO	AltVendor	27h	P_ID LO	PrVendor
0018h	A_ID HI	ID#	28h	P_ID HI	ID#
. . .	. . .	. . .	. . .	. . .	. . .

NOTE:
1. In word mode, A0 is not driven, so 0010h means that Address A5 = 1.

Table 7: Query Structure[1]

OFFSET	SUBSECTION NAME	DESCRIPTION
00h		Manufacturer compatibility code
01h		Device code
(BA+2)h[2]	Block Status Register	Block-specific information
03–0Fh	Reserved	Reserved for vendor-specific information
10h	CFI Query Identification String	Reserved for vendor-specific information
1Bh	System Interface Information	Command-set ID and vendor data offset
27h	Device Geometry Definition	Flash device layout
P[3]	Primary Extended Query Table	Vendor-defined additional information specific to the primary vendor algorithm

NOTE:
1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = Block address beginning location (i.e., 020000h is block two's beginning location when the block size is 64K-word).
3. Offset 15 defines "P," which points to the Primary Extended Query Table.

CFI Query Identification String

The CFI query identification string verifies whether the component supports the CFI specification. Additionally, it indicates the specification version and supported vendor-specified command set(s).

Table 8: Block Status Register

OFFSET	LENGTH	DESCRIPTION	ADDRESS[1]	VALUE
(BA+2)h[1]	1	Block Lock Status Register	(BA+2)h	
		BSR0 Block Lock Status 0 = Unlocked 1 = Locked	(BA+2)h	(Bit 0) 0 or 1
		BSR1–7 Reserved for Future Use	(BA+2)h	(Bit 1–7) 0

NOTE:
1. BA = the beginning location of a block address (i.e., 010000h is block one's [64K-word] beginning location in word mode).

Table 9: CFI Identification

OFFSET	LENGTH	DESCRIPTION	ADDRESS	HEX CODE	VALUE
10h	3	Query-unique ASCII string "QRY"	10h 11h 12h	51 52 59	Q R Y
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13h 14h	01 00	
15h	2	Extended query table primary algorithm	15h 16h	31 00	
17h	2	Alternate vendor command set and control interface ID code; 0000h means no second vendor-specified algorithm exists	17h 18h	00 00	
19h	2	Secondary algorithm extended query table address; 0000h means none exists	19h 1Ah	00 00	

System Interface Information

Table 10 provides useful information about optimizing system interface software.

Table 10: System Interface Information

OFFSET	LENGTH	DESCRIPTION	ADDRESS	HEX CODE	VALUE
1Bh	1	V_{CC} logic supply minimum program/erase voltage Bits 0–3 BCD 100mV Bits 4–7 BCD volts	1Bh	27	2.7V
1Ch	1	V_{CC} logic supply maximum program/erase voltage Bits 0–3 BCD 100mV Bits 4–7 BCD volts	1Ch	36	3.6V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage Bits 0–3 BCD 100mV Bits 4–7 Hex volts	1Dh	00	0.0V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage Bits 0–3 BCD 100mV Bits 4–7 Hex volts	1Eh	00	0.0V
1Fh	1	"n" such that typical single word program timeout = 2^nµs	1Fh	07	128µs
20h	1	"n" such that typical max. buffer write timeout = 2^nms	20h	07	128µs
21h	1	"n" such that typical block erase timeout = 2^nµs	21h	0A	1s
22h	1	"n" such that typical full chip erase timeout = 2^nms	22h	00	N/A
23h	1	"n" such that word program timeout = 2^n times typical	23h	04	2ms
24h	1	"n" such that typical max. buffer write timeout = 2^n times typical	24h	04	2ms
25h	1	"n" such that maximum block erase timeout = 2^n times typical	25h	04	16s
26h	1	"n" such that maximum chip erase timeout = 2^n times typical	26h	00	N/A

Device Geometry Definition

Tables 11 and 12 provide important details about the device geometry.

Table 11: Device Geometry Definitions

OFFSET	LENGTH	DESCRIPTION	CODE (see table 12 below)		
27h	1	"n" such that device size= 2^n in number of bytes	27h		
28h	2	Flash device interface: x8 async, x16 async, x8/x16 async; 28:00 29:00, 28:01 29:00, 28:02 29:00	28h 29h	02 00	x8/x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2n	2Ah 2Bh	05 00	32
2Ch	1	Number of erase block regions within device: 1. x = 0 means no erase blocking; the device erases in "bulk" 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) x (individual block size)	2Ch	01	1
2Dh	4	Erase Block Region 1 Information Bits 0–15 = y; y + 1 = number of identical-size erase blocks Bits 16–31 = z; region erase block(s) size are z x 256 bytes	2Dh 2Eh 2Fh 30h		

Table 12: Device Geometry Definition Codes

ADDRESS	32Mb	64Mb	128Mb
27h	16	17	18
28h	02	02	02
29h	00	00	00
2Ah	05	05	05
2Bh	00	00	00
2Ch	01	01	01
2Dh	1F	3F	7F
2Eh	00	00	00
2Fh	00	00	00
30h	02	02	02

Primary Vendor-Specific Extended-Query Table

Table 13 includes information about optional Flash features and commands and other similar information.

Table 13: Primary Vendor-Specific Extended-Query

OFFSET[1] P = 31h	DESCRIPTION (OPTIONAL FLASH FEATURES AND COMMANDS)	ADDRESS	HEX CODE	VALUE
(P+0)h (P+1)h (P+2)h	Primary extended query table Unique ASCII string, PRI	31h 32h 33h	50 52 49	P R I
(P+3)h	Major version number, ASCII	34h	31	1
(P+4)h	Minor version number, ASCII	35h	31	1
(P+5)h (P+6)h (P+7)h (P+8)h	Optional feature and command support (1 = yes, 0 = no) bits 9–31are reserved; undefined bits are "0." If bit 31 is "1," then another 31-bit field of optional features follows at the end of the bit 30 field. Bit 0 Chip erase supported = no = 0 Bit 1 Suspend erase supported = yes = 1 Bit 2 Suspend program supported = yes = 1 Bit 3 Legacy lock/unlock supported = no = 0 Bit 4 Queued erase supported = no = 0 Bit 5 Instant Individual block locking supported = no = 0 Bit 6 Protection bits supported = yes = 1 Bit 7 Page mode read supported = yes = 1	36h 37h 38h 39h	C6h 00 00 00	
(P+9)h	Supported functions after suspend: read array, status, query Other supported operations: Bits 1–7 Reserved; undefined bits are "0" Bit 0 Program supported after erase suspend = yes = 1	3Ah	01	
(P+A)h (P+B)h	Block status register mask Bits 2–15 Reserved; undefined bits are "0" Bit 0 Block lock bit status register active = yes = 1 Bit 1 Block lock down bit status active = no = 0	3Bh 3Ch	01 00	
(P+C)h	V_{CC} logic supply highest-performance program/erase voltage Bits 0–3 BCD value in 100mV Bits 4–7 BCD value in volts	3Dh	33	3.3V
(P+D)h	V_{PP} optimum program/erase supply voltage Bits 0–3 BCD value in 100mV Bits 4–7 Hex value in volts	3Eh	00	0.0V

NOTE:

1. The variable "P" is a pointer which is defined at CFI offset 15h.

Table 14: Protection Register Information

OFFSET[1] P = 31h	DESCRIPTION (Optional Flash Features and Commands)	ADDRESS	HEX	VALUE CODE
(P+E)h	Number of protection register fields in JEDEC ID space. "00h" indicates that 256 protection bytes are available.	3Fh	01	01
(P+F)h (P+10)h (P+11)h (P+12)h	Protection Field 1: Protection Description This field describes user-available, one-time programmable (OTP) protection register bytes. Some are pre-programmed with device-unique serial numbers; others are user-programmable. Bits 0–15 point to the protection register lock byte, the section's first byte. The following bytes are factory-pre-programmed and user-programmable. Bits 0–7 Lock/bytes JEDEC-plane physical low address Bits 8–15 Lock/bytes JEDEC-plane physical high address Bits 16–23 "n" such that 2n = factory pre-programmed bytes Bits 24–31 "n" such that 2n = user-programmable bytes	40h	00	00h

NOTE:
1. The variable "P" is a pointer which is defined at CFI offset 15h.

Table 15: Burst READ Information

OFFSET[1] P = 31h	DESCRIPTION (Optional Flash Features and Commands)	ADDRESS	HEX	VALUE CODE
(P+13)h	Page Mode Read Capability Bits 0–7 = "n" such that 2n Hex value represents the number of read page bytes. See offset 28h for device word width to determine page mode data output width. 00h indicates no read page buffer.	44h	03	8 byte
(P+14)h	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	45h	00	
(P+15)h	Reserved for future use.	46h		

NOTE:
1. The variable "P" is a pointer which is defined at CFI offset 15h.

READ IDENTIFIER CODES Command

Writing the READ IDENTIFIER CODES command initiates the IDENTIFIER CODE operation. Following the writing of the command, READ cycles from addresses shown in Figure 7 on page 12 retrieve the manufacturer, device, and block lock configuration codes (see Table 16 on page 23 for identifier code values). Page mode READs are not supported in this read mode. To terminate the operation, write another valid command. The READ IDENTIFIER CODES command functions independently of the VPEN voltage. This command is valid only when the ISM is off or the device is suspended. See Table 16 on page 23 for read identifier codes.

READ STATUS REGISTER Command

The status register may be read one of two ways: either issue a discrete READ STATUS REGISTER command or when the ISM is running, a READ of the device will provide valid status register data. Once the device is in this mode, all subsequent READ operations output data from the status register until another valid command is written. Page mode READs are not supported in this read mode.

The status register contents are latched on the falling edge of OE# or the first edge of CEx that enables the device (see Table 2 on page 11). To update the status register latch, OE# must toggle to VIH or the device must be disabled before further READs. The READ STATUS REGISTER command functions independently of the VPEN voltage. During a program, block erase, set block lock bits, or clear block lock bits command sequence, only SR7 is valid until the ISM completes or suspends the operation. Device I/O pins DQ0–DQ6 and DQ8–DQ15 are placed in High-Z. When the operation completes or suspends (check status register bit 7), all contents of the status register are valid during a READ.

Table 16: Identifier Codes

CODE	ADDRESS[1]	DATA
Manufacturer's Identification Code[2] • Intel ManID • Micron ManID	X00000h	 (00) 89 (00) 2C
Device Code • 32Mb • 64Mb • 128Mb	X00001h	 (00) 16 (00) 17 (00) 18
Block Lock Configuration • Block is Unlocked • Block is Locked • Reserved for Future Use	XX0002h[3]	 DQ0 = 0 DQ0 = 1 DQ1–DQ7

NOTE:

1. A0 is not used in either x8 or x16 modes when obtaining the identifier codes. The lowest-order address line is A1. Data is always presented on the low byte in x16 mode (upper byte contains 00h).
2. Different ManID devices are ordered via separate part numbers. See Figure 4 on page 8 for details.
3. X selects the specific block's lock configuration code. See Figure 6 on page 11 for the device identifier code memory map.

Table 17: Status Register Definitions

ISMS	ESS	ECLBS	PSLBS	VPENS	PSS	DPS	R
7	6	5	4	3	2	1	0

HIGH-Z WHEN BUSY?	STATUS REGISTER BITS	NOTES
No	SR7 = WRITE STATE MACHINE STATUS (ISMS) 1 = Ready 0 = Busy	Check STS or SR7 to determine block erase, program, or lock bit configuration completion. SR6–SR0 are not driven while SR7 = 0.
Yes	SR6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
Yes	SR5 = ERASE AND CLEAR LOCK BITS STATUS (ECLBS) 1 = Error in Block Erasure or Clear Block Bits 0 = Successful Block Erase or Clear Lock Bits	If both SR5 and SR4 are "1s" after a block erase, program, writer buffer command, or lock bit configuration attempt, an improper command sequence was entered.
Yes	SR4 = PROGRAM AND SET LOCK BIT STATUS (PSLBS) 1 = Error in Programming or Setting Block Lock Bits 0 = Successful Program or Set Block Lock Bits	
Yes	SR3 = PROGRAMMING VOLTAGE STATUS (VPENS) 1 = Low Programming Voltage Detected, Operation Aborted 0 = Programming Voltage OK	SR3 does not provide a continuous voltage level indication. The ISM interrogates and indicates the programming voltage level only after block erase, program, set block lock bits, or clear block lock bits command sequences.
Yes	SR2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	
Yes	SR1 DEVICE PROTECTSTATUS (DPS) 1 = Block Lock Bit Detected, Operation Aborted 0 = Unlock	SR1 does not provide a continuous indication of block lock bit values. The ISM interrogates the block lock bits only after block erase, program, or lock bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Read the block lock configuration codes using the READ IDENTIFIER CODES command to determine block lock bits status. SR0 is reserved for future use and should be masked when polling the status register.
Yes	SR0 = RESERVED FOR FUTURE ENHANCEMENTS	

CLEAR STATUS REGISTER Command

The ISM sets the status register bits SR5, SR4, SR3, and SR1 to "1s." These bits, which indicate various failure conditions, can only be reset by the CLEAR STATUS REGISTER command. Allowing system software to reset these bits can perform several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence). To determine if an error occurred during the sequence, the status register may be polled. To clear the status register, the CLEAR STATUS REGISTER command (50h) is written. The CLEAR STATUS REGISTER command functions independently of the applied VPEN voltage and is only valid when the ISM is off or the device is suspended.

BLOCK ERASE Command

The BLOCK ERASE command is a two-cycle command that erases one block. First, a block erase setup is written, followed by a block erase confirm. This command sequence requires an appropriate address within the block to be erased. The ISM handles all block preconditioning, erase, and verify. Time tWB after the two-cycle block erase sequence is written, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the output of the STS pin or status register bit SR7. Toggle OE# or CEx to update the status register. Upon block erase completion, status register bit SR5 should be checked to detect any block erase error. When an error is detected, the status register should be cleared before system software attempts corrective actions. The CEL remains in read status register mode until a new command is issued. This two-step setup command sequence ensures that block contents are not accidentally erased. An invalid block erase command sequence results in status register bits SR4 and SR5 being set to "1." Also, reliable block erasure can only occur when VCC is valid and VPEN = VPENH. Note that SR3 and SR5 are set to "1" if block erase is attempted while VPEN ≤ VPENLK. Successful block erase requires that the corresponding block lock bit be cleared. Similarly, SR1 and SR5 are set to "1" if block erase is attempted when the corresponding block lock bit is set.

BLOCK ERASE SUSPEND Command

The BLOCK ERASE SUSPEND command allows block erase interruption in order to read or program data in another block of memory. Writing the BLOCK ERASE SUSPEND command immediately after starting the block erase process requests that the ISM suspend the block erase sequence at an appropriate point in the algorithm. When reading after the BLOCK ERASE SUSPEND command is written, the device outputs status register data. Polling status register bit SR7, followed by SR6, shows when the BLOCK ERASE operation has been suspended. In the default mode, STS also transitions to VOH. ^{t}LES defines the block erase suspend latency. At this point, a READ ARRAY command can be written to read data from blocks other than that which is suspended. During erase suspend to program data in other blocks, a program command sequence can also be issued. During a PROGRAM operation with block erase suspended, status register bit SR7 returns to "0" and STS output (in default mode) transitions to VOL. However, SR6 remains "1" to indicate block erase suspend status. Using the PROGRAM SUSPEND command, a program operation can also be suspended. Resuming a SUSPENDED programming operation by issuing the Program Resume command enables the suspended programming operation to continue. To resume the suspended erase, the user must wait for the programming operation to complete before issuing the Block ERASE RESUME command. While block erase is suspended, the only other valid commands are READ QUERY, READ STATUS REGISTER, CLEAR STATUS REGISTER, CONFIGURE, and BLOCK ERASE RESUME. After a BLOCK ERASE RESUME command to the Flash memory is completed, the ISM continues the block erase process. Status register bits SR6 and SR7 automatically clear and STS (in default mode) returns to VOL. After the ERASE RESUME command is completed, the device automatically outputs status register data when read. VPEN must remain at VPENH (the same VPEN level used for block erase) during block erase suspension. Block erase cannot resume during block erase suspend until PROGRAM operations are complete.