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Parallel NOR Flash Automotive Memory

MT28FW02GBBA1HPC-0AAT, MT28FW02GBBA1LPC-0AAT

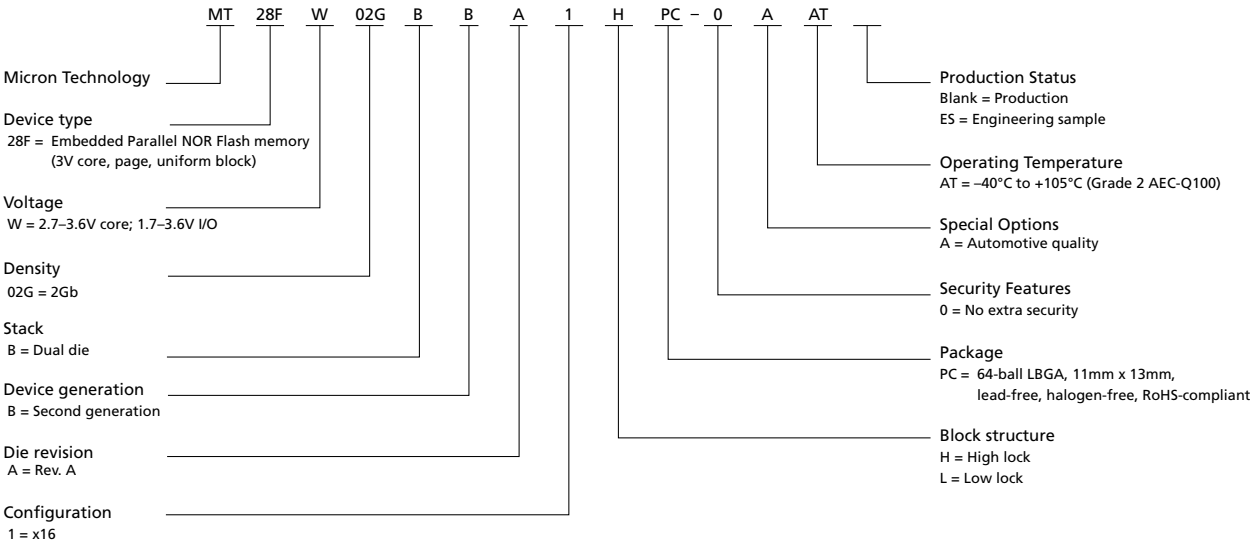
Features

- 2Gb stacked device (Two 1Gb die)
- Single-level cell (SLC) process technology
- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65–V_{CC} (I/O buffers)
- Asynchronous random/page read
  - Page size: 16 words
  - Page access: 20ns (V_{CC} = V_{CCQ} = 2.7–3.6V)
  - Random access: 105ns (V_{CC} = V_{CCQ} = 2.7–3.6V)
  - Random access: 110ns (V_{CCQ} = 1.65–V_{CC})
- Buffer program (512-word program buffer)
  - 2.0 MB/s (TYP) when using full buffer program
  - 2.5 MB/s (TYP) when using accelerated buffer program (V_{HH})
- Word program: 25µs per word (TYP)
- Block erase (128KB): 0.2s (TYP)
- Memory organization
  - Uniform blocks: 128KB or 64KW each
  - x16 data bus
- Program/erase suspend and resume capability
  - Read from another block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- Unlock bypass, block erase, die erase, and write to buffer capability
- BLANK CHECK operation to verify an erased block
- CYCLIC REDUNDANCY CHECK (CRC) operation to verify a program pattern
- V_{PP}/WP# protection
  - Protects first or last block regardless of block protection settings
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
- Extended memory block
  - 512-word block for permanent, secure identification
  - Programmed or locked at the factory or by the customer
- JESD47-compliant
  - 100,000 (minimum) ERASE cycles per block
  - Data retention: 20 years (TYP)
- Package
  - 64-ball LBGA, 11mm x 13mm (PC)
- RoHS-compliant, halogen-free packaging
- Automotive operating temperature
  - Ambient: –40°C to 105°C

Part Numbering Information

For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Chart



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General Description

The device is an asynchronous, uniform block, parallel NOR Flash memory device. It is a 2Gb stacked device that contains two 1Gb dies. It is selected by the A[max]. While A[max] = 0, the lower 1Gb die is selected, and while A[max] = 1, the upper 1Gb die is selected. READ, ERASE, and PROGRAM operations are performed using a single low-voltage supply. Upon power-up, the device defaults to read array mode.

The main memory array is divided into uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

CE#, OE#, and WE# control the bus operation of the device and enable a simple connection to most microprocessors, often without additional logic.

The device supports asynchronous random read and page read from all blocks of the array. It also features an internal program buffer that improves throughput by programming 512 words via one command sequence. A 512-word extended memory block overlaps addresses with array block 0. Users can program this additional space and then protect it to permanently secure the contents. The device also features different levels of hardware and software protection to secure blocks from unwanted modification.

Automatic Power Savings Feature

The automatic power savings feature provides low power operation during reads.

After data is read from the memory array and the address lines are quiescent, the automatic power savings feature reduces device current to a low value of I_{CCAPS}.

During automatic power savings mode, average current is measured over 5ms time interval 5µs after the following events happen:

- No internal read, program or erase activity occurring
- RST# is deasserted and CE# is asserted
- All other signals are quiescent and at V_{SS} or V_{CCQ}

Figure 2: Logic Diagram

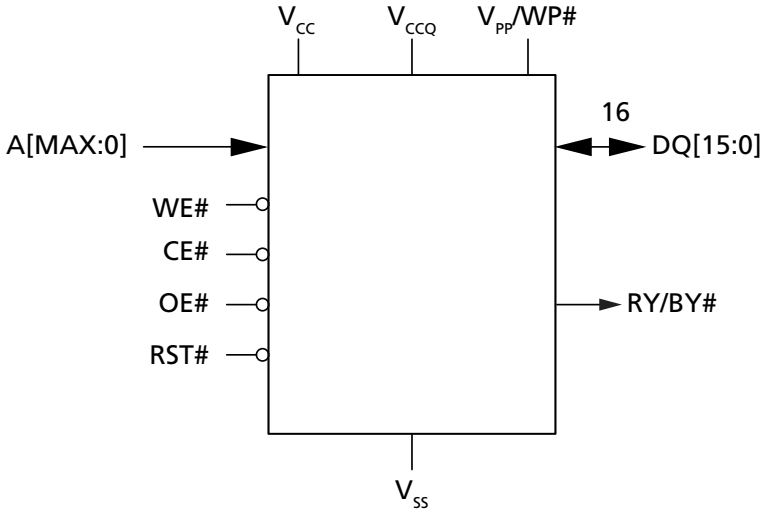
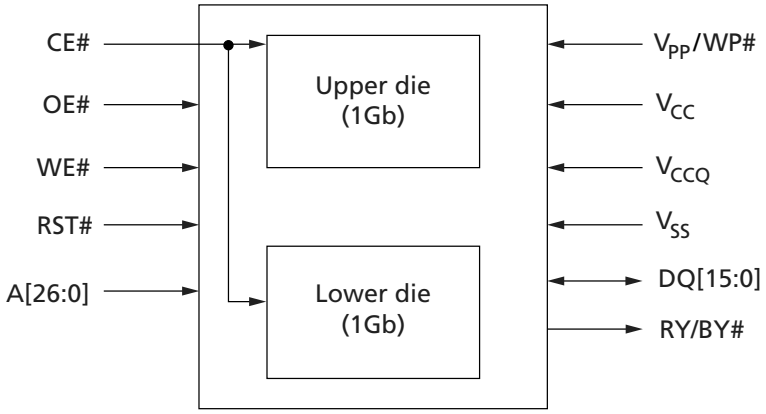


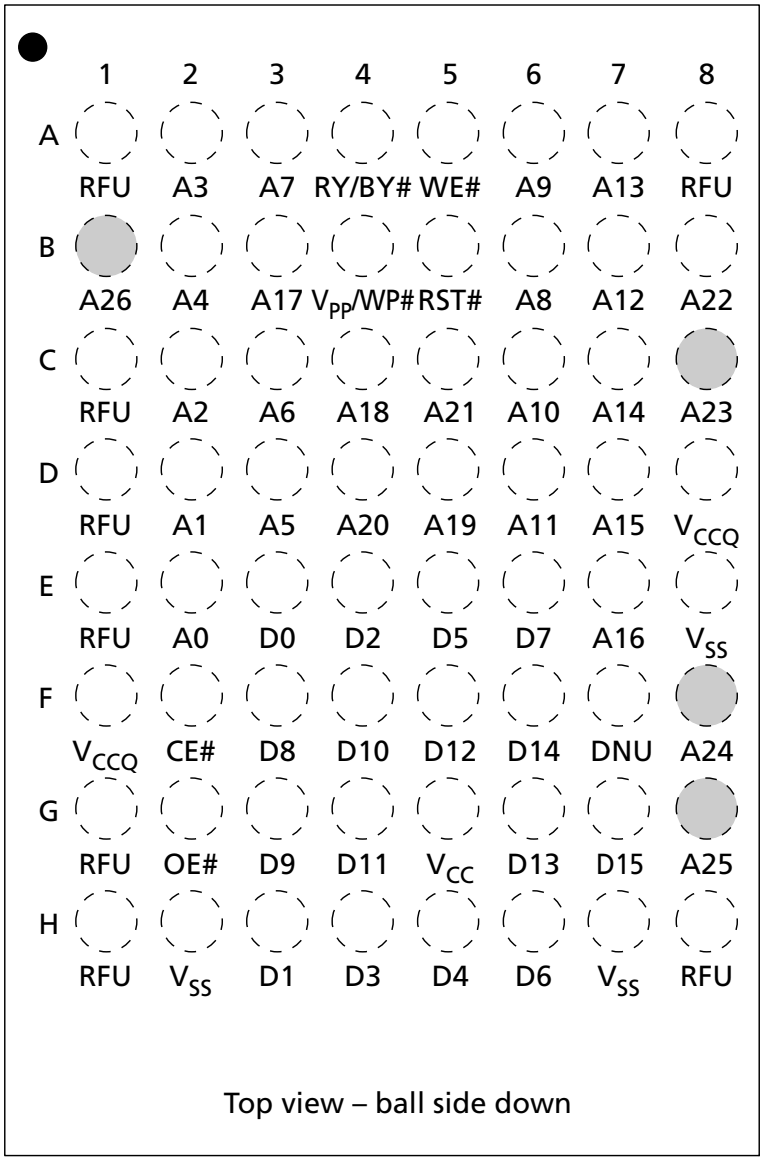
Figure 3: Dual Die Configuration – 2Gb



Note: 1. A[26] = V_{IH} selects the upper die; A[26] = V_{IL} selects the lower die.

Signal Assignments

Figure 4: 64-Ball Fortified BGA



Notes:
1. A23 is valid for 256Mb and above; otherwise, it is RFU.
2. A24 is valid for 512Mb and above; otherwise, it is RFU.
3. A25 is valid for 1Gb and above; otherwise, it is RFU.
4. A26 is valid for 2Gb only; otherwise it is RFU.

Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller. A[max] is used as a virtual CE pin. When A[max] = 0, the lower 1Gb die is selected, When A[max] = 1, the upper 1Gb is selected.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby and data outputs are High-Z.
OE#	Input	**Output enable:** Active LOW input. OE# LOW enables the data output buffers during READ cycles. When OE# is HIGH, data outputs are High-Z.
WE#	Input	**Write enable:** Controls WRITE operations to the device. Address is latched on the falling edge of WE# and data is latched on the rising edge.
V_{PP}/WP#	Input	**V_{PP}/Write Protect:** Provides WRITE PROTECT function and V_{HH} function. These functions protect the lowest or highest block and enable the device to enter unlock bypass mode, respectively. (Refer to Hardware Protection and Bypass Operations for details.)
RST#	Input	**Reset:** Applies a hardware reset to the device control logic and places it in standby, which is achieved by holding RST# LOW for at least ^{t}PLPH. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}PHWL, whichever occurs last).
DQ[15:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine.
RY/BY#	Output	**Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one (or more) of the devices is (are) busy. A 10K Ohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The device is disabled when $V_{CC} \le V_{LKO}$. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1µF and 0.01µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations (see DC Characteristics).
V_{CCQ}	Supply	**I/O supply voltage:** Provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}. A 0.1µF and 0.01µF capacitor should be connected between V_{CCQ} and V_{SS} to decouple the current surges from the power supply.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to the system ground.

Table 1: Signal Descriptions (Continued)

Name	Type	Description
RFU	—	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. These should be treated in the same way as a DNU signal.
DNU	—	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No connect:** No internal connection; can be driven or floated.

Memory Organization

Memory Configuration

The main memory array is divided into 128KB or 64KW uniform blocks.

Memory Map

Table 2: Blocks[2047:0]

Block	Address Range	
	Start	End
2047	7FF 0000h	7FF FFFFh
⋮	⋮	⋮
1023	3FF 0000h	3FF FFFFh
⋮	⋮	⋮
511	1FF 0000h	1FF FFFFh
⋮	⋮	⋮
255	0FF 0000h	0FF FFFFh
⋮	⋮	⋮
127	07F 0000h	07F FFFFh
⋮	⋮	⋮
63	03F 0000h	03F FFFFh
⋮	⋮	⋮
0	000 0000h	000 FFFFh

Note: 1. Block 0-1023 is the lower die, block 1024-2047 is the upper die.

Bus Operations

Table 3: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	A[MAX:0]	DQ[15:0]
READ	L	L	H	H	X	Address	Data output
WRITE	L	H	L	H	H[3]	Command address	Data input[4]
STANDBY	H	X	X	H	X	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z
RESET	X	X	X	L	X	X	High-Z

Notes:
1. Typical glitches of less than 3ns on CE#, OE#, and WE# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# is LOW, then the highest or the lowest block remains protected, depending on line item.
4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, extended memory block, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 16 words and is addressed by address inputs A[3:0]. The extended memory blocks and CFI area support page read mode.

A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. If CE# goes HIGH and returns LOW for a subsequent access, a random read access is performed and ^{t}ACC or ^{t}CE is required. (See AC Characteristics for details about when the output becomes valid.)

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation (See AC Characteristics for timing requirement details).

Standby

Driving CE# HIGH in read mode causes the device to enter standby and data I/Os to be High-Z (See DC Characteristics).

During PROGRAM or ERASE operations, the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes. The device cannot be placed into standby mode during a PROGRAM/ERASE operation.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and the outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to the standby level, independently from CE#, OE#, or WE# inputs.

When RST# is HIGH, a time of ^{t}PHEL is required before a READ operation can access the device, and a delay of ^{t}PHWL is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored, the device defaults to read array mode, and the data polling register is reset.

If RST# is driven LOW during a PROGRAM/ERASE operation or any other operation that requires writing to the device, the operation will abort within ^{t}PLRH, and memory contents at the aborted block or address are no longer valid.

Registers

The device features two methods for monitoring internal status during modify operations: data polling status and read status register. Users must not mix the two methods. Only one method at a time must be used to monitor internal operations.

Data Polling Register

The device has two 1Gb dies, the selected die automatically enters data polling status mode upon command issuance. The data polling status information uses the following to indicate information: DQ1, DQ2, DQ3, DQ5, DQ6, and DQ7; DQ[15:8] are reserved and will output 00h. The deselected die is in standby mode.

Table 4: Data Polling Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program, erase, or blank check controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE/BLANK CHECK operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or DIE ERASE operation fails to write the correct data to the memory, or when a BLANK CHECK or CRC operation fails.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	During DIE ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM, BLANK CHECK, or CRC operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode (see WRITE TO BUFFER PROGRAM command).	

Notes:
1. The data polling register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE operation in progress, DQ7 outputs 0; upon ERASE operation's successful completion, DQ7 outputs 1. During a BUFFER PROGRAM operation, the data polling bit is valid only for the last word being programmed in the write buffer.

3. After successful completion of a PROGRAM, ERASE, or BLANK CHECK operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.
5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.
6. When DQ5 is set to 1, a READ/RESET (F0h) command must be issued before any subsequent command.

Table 5: Operations and Corresponding Bit Settings

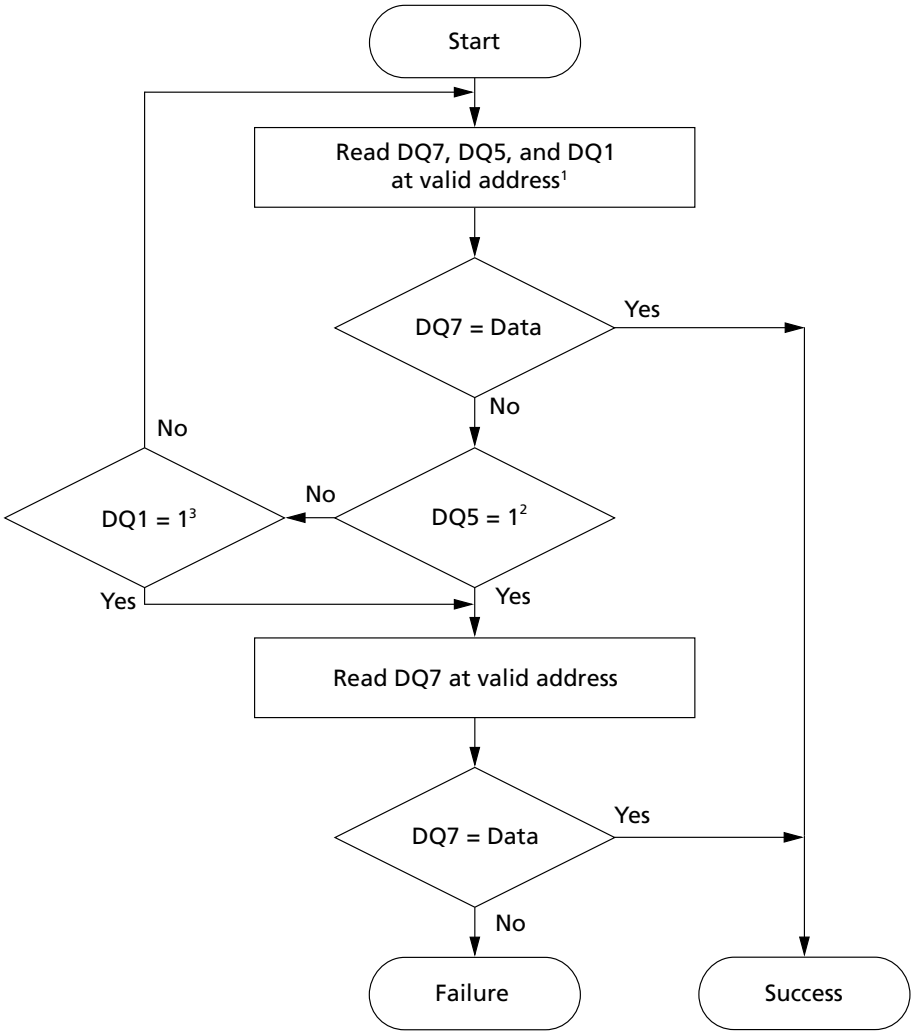
Note 1 and 2 apply to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	–	0	0	3
CRC range of blocks	Any address	1	Toggle	0	–	–	0	0	
CRC chip	Any address	DQ7#	Toggle	0	–	–	0	0	4
DIE ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLANK CHECK	Blank-checking block	0	Toggle	0	1	Toggle	–	0	
	Non-blank-checking block	0	Toggle	0	1	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
PROGRAM SUSPEND	Programming block	Invalid operation						High-Z	
	Nonprogramming block	Outputs memory array data as if in read mode						High-Z	
ERASE SUSPEND	Erasing block	1	No Toggle	0	–	Toggle	–	High-Z	
	Non-erasing block	Outputs memory array data as if in read mode						High-Z	
PROGRAM during ERASE SUSPEND	Erasing block	DQ7#	Toggle	0	–	Toggle	–	0	3
	Non-erasing block	DQ7#	Toggle	0	–	No Toggle	–	0	3
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	High-Z	
PROGRAM Error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	3
ERASE Error	Any address	0	Toggle	1	1	Toggle	–	High-Z	
BLANK CHECK Error	Any address	0	Toggle	1	1	Toggle	–	High-Z	
CRC range of blocks error	Any address	1	Toggle	1	–	–	–	High-Z	
CRC chip error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	4

Notes:
1. Unspecified data bits should be ignored.
2. The table is only for selected die. The non-select die will output the array content.

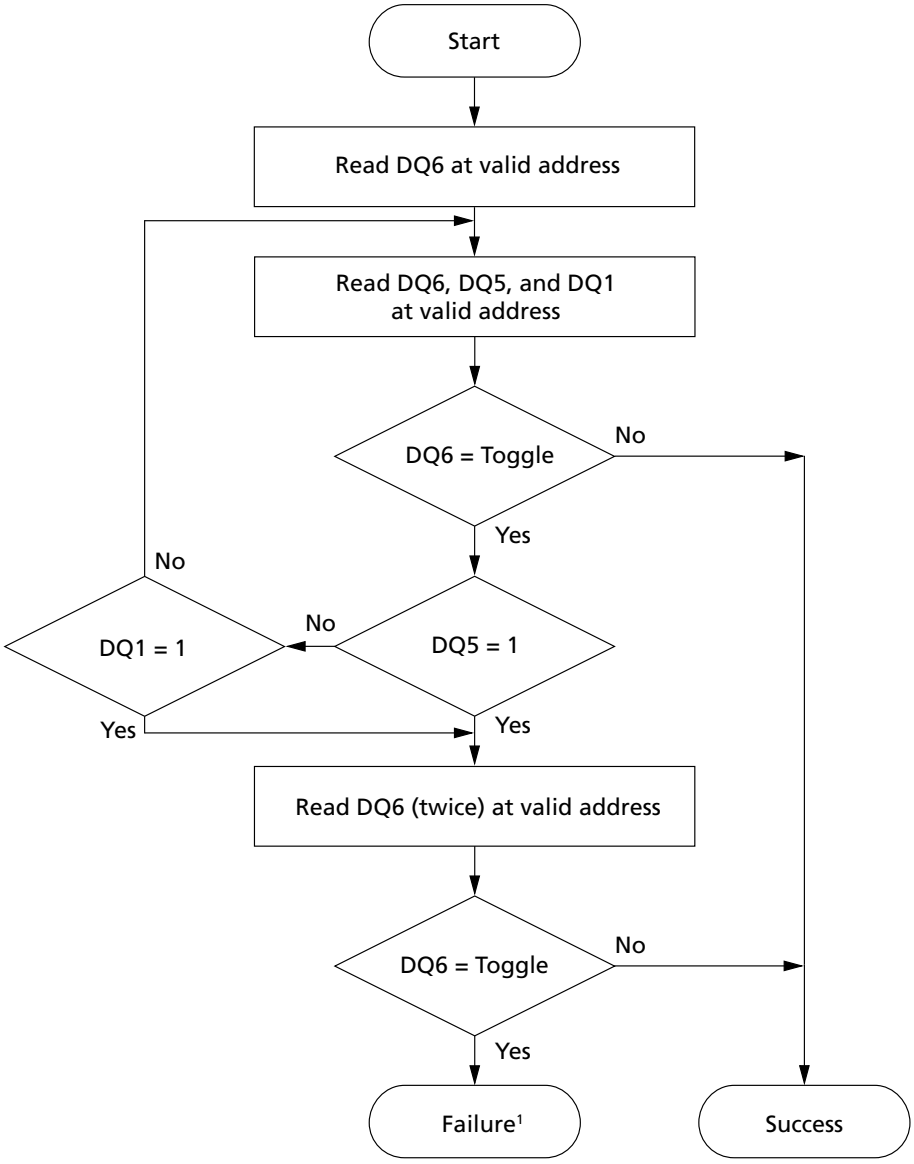
3. DQ7# for buffer program is related to the last address location loaded.
4. DQ7# is the reverse DQ7 of the last word or byte loaded before CRC chip confirm command cycle.

Figure 5: Data Polling Flowchart



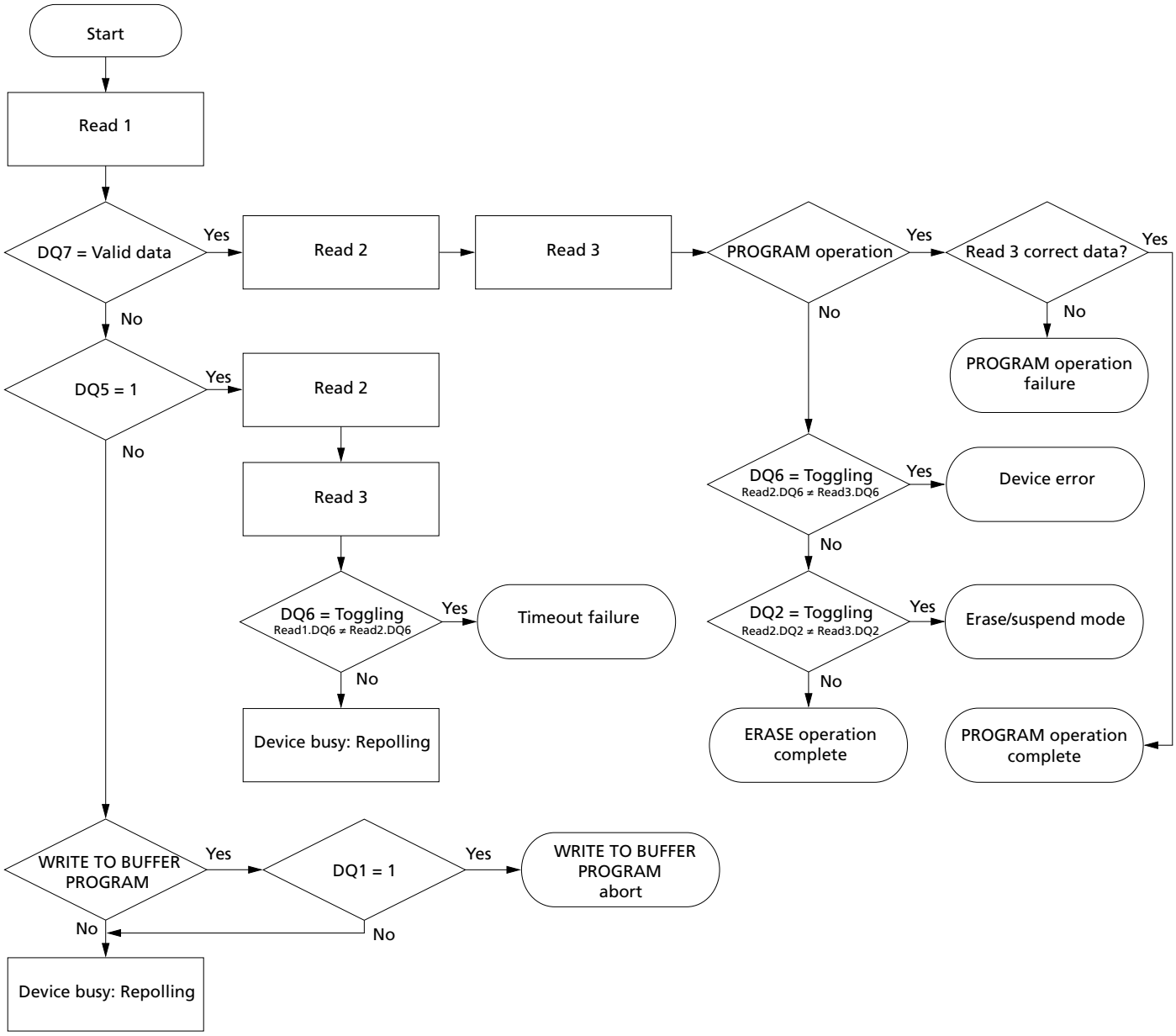
Notes:
1. Valid address is the last address being programmed or an address within the block being erased.
2. Failure results: DQ5 = 1 indicates an operation error. A READ/RESET (F0h) command must be issued before any subsequent command.
3. Failure results: DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation. A full three-cycle RESET (AAh/55h/F0h) command sequence must be used to reset the aborted device.

Figure 6: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 7: Data Polling/Toggle Bit Flowchart



Read Status Register

The device has two status registers: Each die has one status register. The operation initiated in one die must be terminated before attempting to start a new operation in another die. During PROGRAM or ERASE operations in one die, the related status register should be monitored by asserting A[max].

The device's status register displays PROGRAM, ERASE, and BLANK CHECK operations status. A device's status can be read after writing the READ STATUS REGISTER command (70h). When the READ STATUS REGISTER command is issued, the current status is captured by the register and the device is in read status register mode. The first read access in the status register mode exits the mode and returns to the output state when the READ STATUS REGISTER command was issued. No other command should be sent before reading the status register to exit the status register mode.

The status register bits are output on DQ[7:0], while DQ[15:8] outputs are 00h.

Table 6: Status Register Definitions

Bit	Name	Settings	Description
SR[15:8]	–	Reserved	Reserved for future use. Will always be set to 0.
SR7	Device program/ erase/blank check status	0 = Busy 1 = Ready	Indicates erase, program, or blank check completion in the device. SR[6:1] are invalid; SR7 = 0.
SR6	Erase suspend status	0 = Erase in progress/ complete 1 = Erase suspended	Indicates whether the device is erase suspended. After issuing an ERASE SUSPEND command, SR7 and SR6 are set to 1. SR6 remains set until the device receives an ERASE RESUME command.
SR5	Erase/blank check status	0 = Erase/blank check successful 1 = Erase/blank check error	Set to 1 if an attempted erase or blank check failed.
SR4	Program status	0 = Program success 1 = Program error	Indicates whether the program failed or the buffer program has aborted.
SR3	Writer buffer abort status	0 = Program not aborted 1 = Program aborted during buffer program	Indicates whether the buffer program has aborted.
SR2	Program suspend status	0 = Program in progress/complete 1 = Program suspended	Indicates whether the device is program suspended. After receiving a PROGRAM SUSPEND command, SR7 and SR2 are set to 1, and remain set at 1 until a RESUME command is received.
SR1	Device protect status	0 = Unlocked 1 = Aborted erase/ program attempt on a locked block	Indicates whether program or erase was attempted on a locked block. If an ERASE or PROGRAM operation is attempted on a locked block, SR1 is set to 1 and the operation aborts.
SR0	–	Reserved	Reserved for future use. Will always be set to 0.

Clear Status Register

The status register content can be cleared by CLEAR STATUS REGISTER command (71h). The CLEAR STATUS REGISTER command clears the status register bits SR[6:1]. SR7 remains at 0, which indicates the device is busy.

However, for buffer program abort only, the CLEAR STATUS REGISTER command would change also SR7 to 1, which reverts the device to main array read mode. The status register can also be cleared by using RESET Command (F0h).

Lock Register

The device has two lock registers: Each die has one lock register. Micron recommends programming both of the lock registers with the same contents in order to have the same protection scheme for both the upper and lower die.

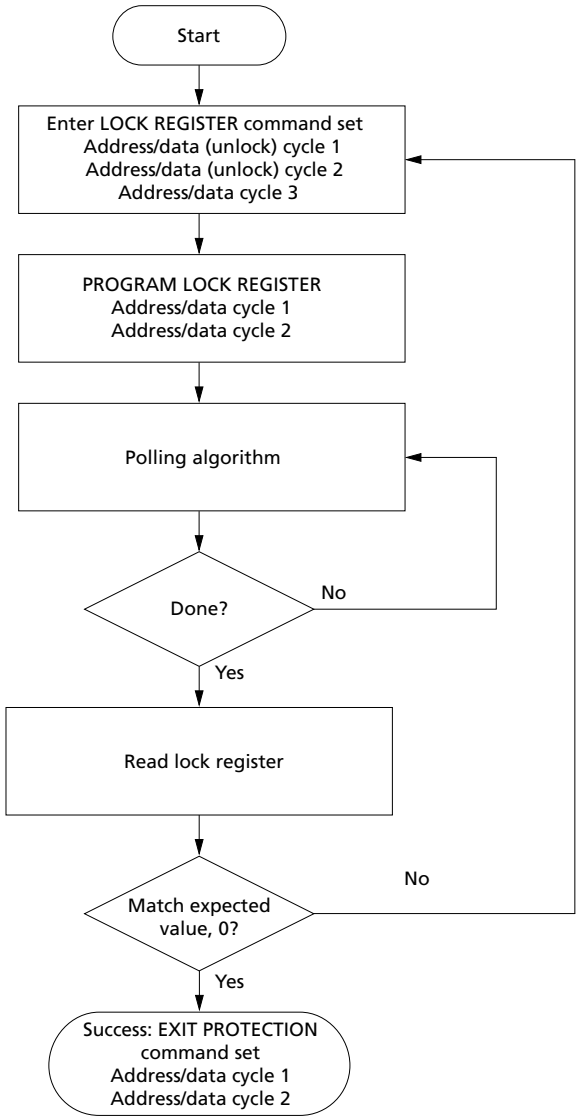
Table 7: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ[15:9]	–	Default value = 1	DQ[15:9] are reserved and are set to a default value of 1.	
DQ8	–	Default value = 0	DQ8 is reserved and is set to a default value of 0.	
DQ[7:3]	–	Default value =1	DQ[7:3] are reserved and are set to a default value of 1.	
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (default)	Places the device permanently in password protection mode.	2
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (default)	Places the device in nonvolatile protection mode, with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	2
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command.	

Notes:
1. The lock register is a 16-bit, one-time programmable register. DQ[15:3] are reserved.
2. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

Figure 8: Lock Register Program Flowchart



Notes:
1. Each lock register bit can be programmed only once.
2. See the Block Protection Command Definitions table for address-data cycle details.
3. DQ5 and DQ1 are ignored in this algorithm flow.

Standard Command Definitions – Address-Data Cycles

Table 8: Standard Command Definitions – Address-Data Cycles

Note 1 applies to entire table

Command and Code/Subcode	Address and Data Cycles												Notes
	1st		2nd		3rd		4th		5th		6th		
	A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations													
READ/RESET (F0h)	555	AA	2AA	55	X	F0							2
READ CFI (98h)	555	98											
EXIT READ CFI (F0h)	X	F0											
AUTO SELECT (90h)	555	AA	2AA	55	555	90	Note 3	Note 3					4, 5
EXIT AUTO SELECT (F0h)	X	F0											
READ STATUS (70h)	555	70											
CLEAR STATUS (71h)	555	71											
BYPASS Operations													
UNLOCK BYPASS (20h)	555	AA	2AA	55	555	20							
UNLOCK BYPASS RESET (90h/00h)	X	90	X	00									
PROGRAM Operations													
PROGRAM (A0h)	555	AA	2AA	55	555	A0	PA	PD					
UNLOCK BYPASS PROGRAM (A0h)	X	A0	PA	PD									6
WRITE TO BUFFER PROGRAM (25h)	555	AA	2AA	55	BAd	25	BAd	N	PA	PD			7, 8, 9
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	BAd	25	BAd	N	PA	PD							6
WRITE TO BUFFER PROGRAM CONFIRM (29h)	BAd	29											7
BUFFERED PROGRAM ABORT and RESET (F0h)	555	AA	2AA	55	555	F0							
PROGRAM SUSPEND (B0h)	X	B0											
PROGRAM RESUME (30h)	X	30											
PROGRAM SUSPEND (51h)	X	51											
PROGRAM RESUME (50h)	X	50											
ERASE Operations													
DIE ERASE (80/10h)	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10	
UNLOCK BYPASS DIE ERASE (80/10h)	X	80	X	10									6

Table 8: Standard Command Definitions – Address-Data Cycles (Continued)

Note 1 applies to entire table

Command and Code/Subcode	Address and Data Cycles												Notes
	1st		2nd		3rd		4th		5th		6th		
	A	D	A	D	A	D	A	D	A	D	A	D	
BLOCK ERASE (80/30h)	555	AA	2AA	55	555	80	555	AA	2AA	55	BAd	30	
UNLOCK BYPASS BLOCK ERASE (80/30h)	X	80	BAd	30									6
ERASE SUSPEND (B0h)	X	B0											
ERASE RESUME (30h)	X	30											
BLANK CHECK Operations													
BLANK CHECK	555	33											

Notes:
1. A = Address; D = Data; X = "Don't Care"; BAd = Any address in the block; N = Number of words to be programmed; PA = Program address; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode. All the commands are effective for the selected die only.
2. A full three-cycle RESET command sequence must be used to reset the device in the event of a buffered program abort error (DQ1 = 1).
3. These cells represent READ cycles (versus WRITE cycles for the others).
4. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
5. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Extended Memory Block Protection table.
6. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
7. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM 3rd and 4th cycles.
8. WRITE TO BUFFER PROGRAM operation: maximum cycles = 517. UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 515. WRITE TO BUFFER PROGRAM operation: N + 1 = words to be programmed; maximum buffer size = 512 words.
9. A[MAX:9] address pins should remain unchanged while A[8:0] pins are used to select a word within the N+1 word page.