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Micron StrataFlash Embedded Memory

MT28GU256AAA1EGC-0SIT, MT28GU256AAA2EGC-0SIT
MT28GU512AAA1EGC-0SIT, MT28GU512AAA2EGC-0SIT,
MT28GU01GAAA1EGC-0SIT, MT28GU01GAAA2EGC-0SIT

Features

- High-performance read, program, and erase
  - 96ns initial read access
  - 108 MHz with zero wait-state synchronous burst reads: 7ns clock-to-data output
  - 133 MHz with zero wait-state synchronous burst reads: 5.5ns clock-to-data output
  - 8-, 16-, and continuous-word synchronous-burst reads
  - Programmable WAIT configuration
  - Customer-configurable output driver impedance
  - Buffered Programming: 2.0 µs/Word (TYP), 512Mb, 65nm
  - Block erase: 0.9s per block (TYP)
  - 20µs (TYP) program/erase suspend
- Architecture
  - 16-bit wide data bus
  - Multilevel cell technology
  - Symmetrically-blocked array architecture
  - 256KB erase blocks
  - 1Gb device: Eight 128Mb partitions
  - 512Mb device: Eight 64Mb partitions
  - 256Mb device: Eight 32Mb partitions
  - READ-While-PROGRAM and READ-While-ERASE commands
  - Status register for partition/device status
  - Blank check feature
- Temperature Range
  - Expanded temperature: –40°C to +85°C
- JESD47H-compliant
  - Minimum 100,000 ERASE cycles per block
  - Data retention: 20 years (TYP)
- Power
  - Core voltage: 1.7– 2.0V
  - I/O voltage: 1.7–2.0V
  - Standby current: 60µA (TYP) for 512Mb, 65nm
  - Automatic power savings mode
  - 16-word synchronous-burst read current: 23mA (TYP) @ 108 MHz; 24mA (TYP) @ 133 MHz
- Software
  - Micron® Flash data integrator (FDI) optimized
  - Basic command set (BCS) and extended command set (ECS) compatible
  - Common Flash interface (CFI) capable
- Security
  - One-time programmable (OTP) space
    64 unique factory device identifier bits
    2112 user-programmable OTP bits
  - Absolute write protection: V_{PP} = GND
  - Power-transition erase/program lockout
  - Individual zero latency block locking
  - Individual block lock-down
- Density and packaging
  - 256Mb, 512Mb, and 1Gb
  - Address-data multiplexed and non-multiplexed interfaces
  - 64-Ball Easy BGA

Part Numbering Information

Available with extended memory block prelocked by Micron. Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Figure 1: Current Part Number Decoder

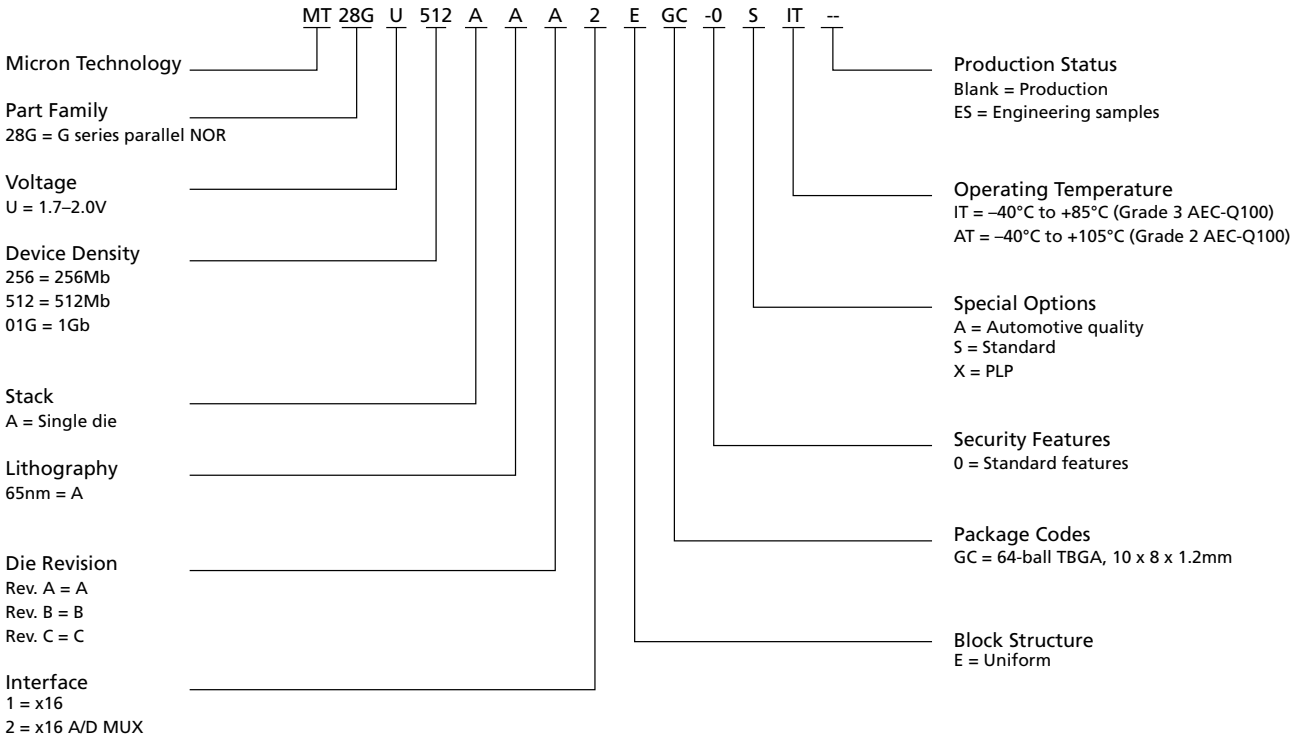

Figure 2: Legacy Part Number Decoder

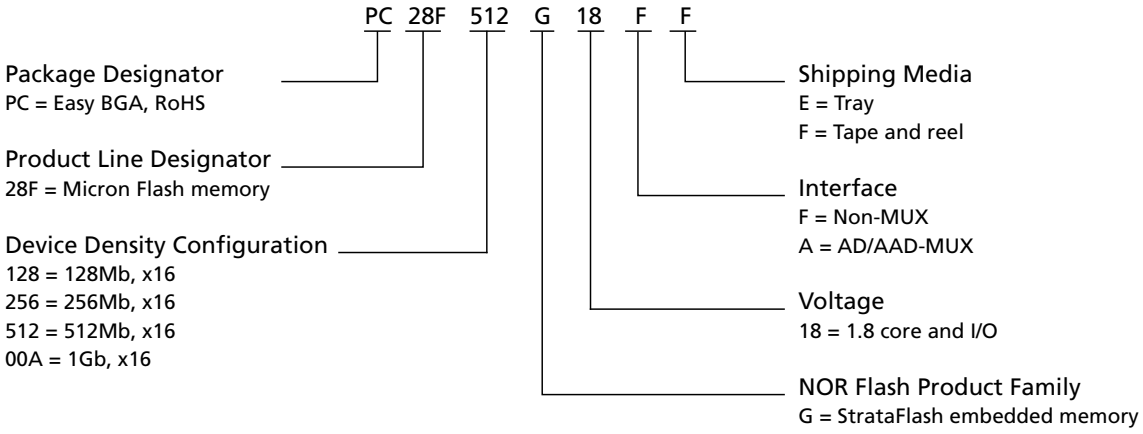

Table 1: Part Number Information

Note 1 and 2 apply to entire table

Micron Part Number	Legacy Part Number	Density	Interface	Shipping Media
MT28GU256AAA1EGC-0SIT	PC28F256G18FE	256Mb	Non-MUX	Tray
	PC28F256G18FF	256Mb	Non-MUX	Tape and Reel
MT28GU256AAA2EGC-0SIT	PC28F256G18AE	256Mb	AD/AAD-MUX	Tray
	PC28F256G18AF	256Mb	AD/AAD-MUX	Tape and Reel
MT28GU512AAA1EGC-0SIT	PC28F512G18FE	512Mb	Non-MUX	Tray
	PC28F512G18FF	512Mb	Non-MUX	Tape and Reel
MT28GU512AAA2EGC-0SIT	PC28F512G18AE	512Mb	AD/AAD-MUX	Tray
	PC28F512G18AF	512Mb	AD/AAD-MUX	Tape and Reel
MT28GU01GAAA1EGC-0SIT	PC28F00AG18FE	1Gb	Non-MUX	Tray
	PC28F00AG18FF	1Gb	Non-MUX	Tape and Reel
MT28GU01GAAA2EGC-0SIT	PC28F00AG18AE	1Gb	AD/AAD-MUX	Tray
	PC28F00AG18AF	1Gb	AD/AAD-MUX	Tape and Reel

Notes:
1. New Micron part numbers must be used for all new samples/designs. Legacy part numbers are being discontinued.
2. Shipping media must be specified at time of order entry for new Micron part numbers.

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General Description

Micron's 65nm device is the latest generation of StrataFlash® memory featuring flexible, multiple-partition, dual-operation architecture. The device provides high-performance, asynchronous read mode and synchronous-burst read mode using 1.8V low-voltage, multilevel cell (MLC) technology.

The multiple-partition architecture enables background programming or erasing to occur in one partition while code execution or data reads take place in another partition. This dual-operation architecture also allows two processors to interleave code operations while PROGRAM and ERASE operations take place in the background. The multiple partitions allow flexibility for system designers to choose the size of the code and data segments.

The device is manufactured using 65nm process technologies and is available in industry-standard chip scale packaging.

Functional Overview

This device provides high read and write performance at low voltage on a 16-bit data bus. The multi-partition architecture provides read-while-write and read-while-erase capability, with individually erasable memory blocks sized for optimum code and data storage.

The device supports synchronous burst reads up to 133 MHz using CLK latching.

Upon initial power-up or return from reset, the device defaults to asynchronous read mode. Configuring the read configuration register enables synchronous burst mode reads. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. In continuous-burst mode, a data read can traverse partition boundaries. A WAIT signal simplifies synchronizing the CPU to the memory.

Designed for low-voltage applications, the device supports READ operations with V_{CC} at 1.8V, and ERASE and PROGRAM operations with V_{PP} at 1.8V or 9.0V. V_{CC} and V_{PP} can be tied together for a simple, ultra low-power design. In addition to voltage flexibility, a dedicated V_{PP} connection provides complete data protection when V_{PP} is less than V_{PPLK}.

A status register provides status and error conditions of ERASE and PROGRAM operations.

One-time programmable (OTP) area enables unique identification that can be used to increase security. Additionally, the individual block lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.

The device offers power-savings features, including automatic power savings mode and standby mode. For power savings, the device automatically enters APS following a READ cycle. Standby is initiated when the system deselects the device by de-asserting CE#.

Configuration and Memory Map

The device features a symmetrical block architecture.

The main array of the 256Mb device is divided into eight 32Mb partitions. Each partition is divided into sixteen 256KB blocks (8 x 16 = 128 blocks).

The main array of the 512Mb device is divided into eight 64Mb partitions. Each partition is divided into thirty-two 256KB blocks (8 x 32 = 256 blocks).

The main array of the 1Gb device is divided into eight 128Mb partitions. Each partition is divided into sixty-four 256KB blocks (8 x 64 = 512 blocks).

Each block is divided into as many as 256 1KB programming regions. Each region is divided into as many as thirty-two 32-byte segments

Table 2: Main Array Memory Map – 256Mb

Partition	Size (Mb)	Block #	Address Range
7	32	127	FF0000-FFFFFF
		. . .	. . .
		112	FD0000-FDFFFF
6	32	111	0DE0000-0DFFFF
		. . .	. . .
		96	0C00000-0C1FFF
5	32	95	0BE0000-0BFFFF
		. . .	. . .
		80	0A00000-0A1FFF
4	32	79	09E0000-09FFFF
		. . .	. . .
		64	0800000-081FFF
3	32	63	07E0000-07FFFF
		. . .	. . .
		48	0600000-061FFF

Table 2: Main Array Memory Map – 256Mb (Continued)

Partition	Size (Mb)	Block #	Address Range
2	32	47	05E0000-05FFFFF
		. . .	. . .
		32	0400000-041FFFF
1	32	31	03E0000-03FFFFF
		. . .	. . .
		16	0200000-021FFFF
0	32	15	01E0000-01FFFFF
		. . .	. . .
		0	0000000-001FFFF

Table 3: Main Array Memory Map – 512Mb, 1Gb

512Mb				1Gb		
Partition	Size (Mb)	Block #	Address Range	Size (Mb)	Block #	Address Range
7	64	255	1FE0000-1FFFFFF	128	511	3FE0000-3FFFFFF
		. . .	. . .		. . .	. . .
		224	1C00000-1C1FFFF		448	3800000-381FFFF
6	64	223	1BE0000-1BFFFFF	128	447	37E0000-37FFFFF
		. . .	. . .		. . .	. . .
		192	1800000-181FFFF		384	3000000-301FFFF
5	64	191	17E0000-17FFFFF	128	383	2FE0000-2FFFFFF
		. . .	. . .		. . .	. . .
		160	1400000-141FFFF		320	2800000-281FFFF
4	64	159	13E0000-13FFFFF	128	319	27E0000-27FFFFF
		. . .	. . .		. . .	. . .
		128	1000000-101FFFF		256	2000000-201FFFF

Table 3: Main Array Memory Map – 512Mb, 1Gb (Continued)

512Mb				1Gb		
Partition	Size (Mb)	Block #	Address Range	Size (Mb)	Block #	Address Range
3	64	127	0FE0000-0FFFFFF	128	255	1FE0000-1FFFFFF
		. . .	. . .		. . .	. . .
		96	0300000-031FFFF		192	1800000-181FFFF
2	64	95	0BE0000-0BFFFFF	128	191	17E0000-17FFFFF
		. . .	. . .		. . .	. . .
		64	0800000-081FFFF		128	1000000-101FFFF
1	64	63	07E0000-07FFFFF	128	127	0FE0000-0FFFFFF
		. . .	. . .		. . .	. . .
		32	0400000-041FFFF		64	0800000-081FFFF
0	64	31	03E0000-03FFFFF	128	63	07E0000-07FFFFF
		. . .	. . .		. . .	. . .
		0	0000000-001FFFF		0	0000000-001FFFF

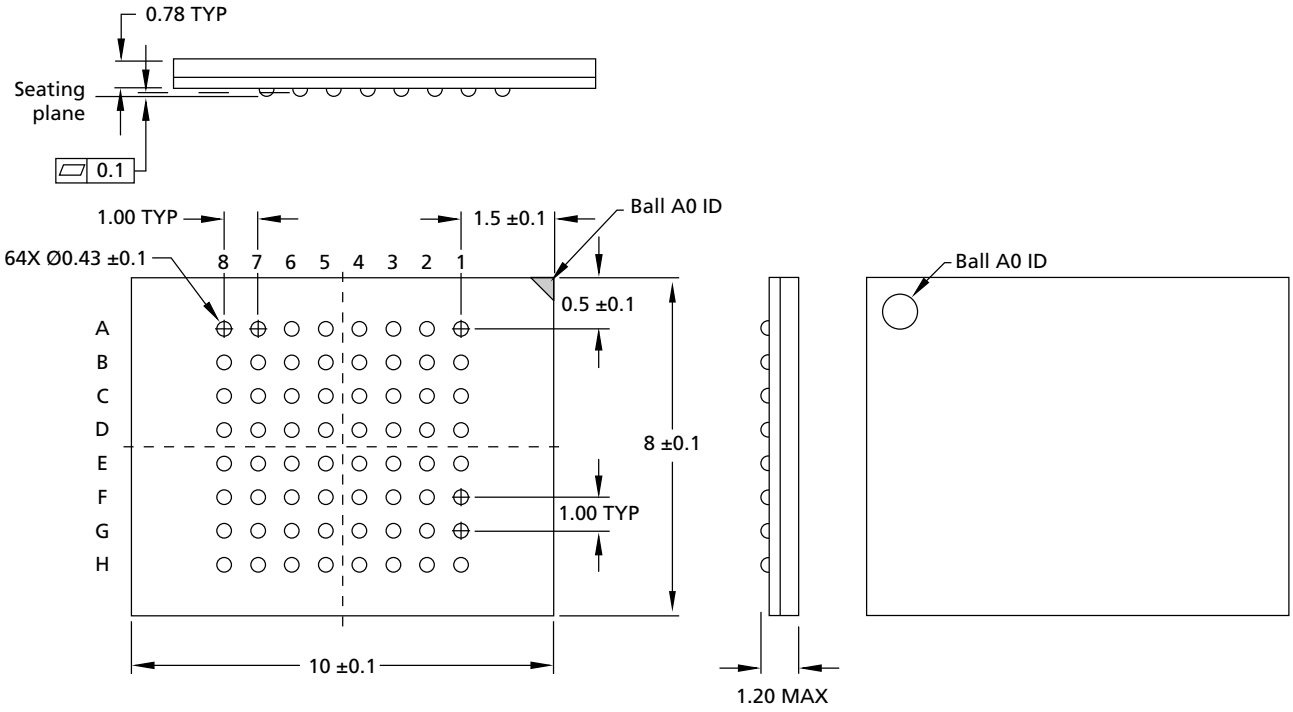
Device ID

Table 4: Device ID Codes

Density	Product	Device Identifier Code (Hex)
256Mb	Non-MUX A/D MUX	8901 8904
512Mb	Non-MUX A/D MUX	887E 8881
1024Mb	Non-MUX A/D MUX	88B0 88B1

Package Dimensions

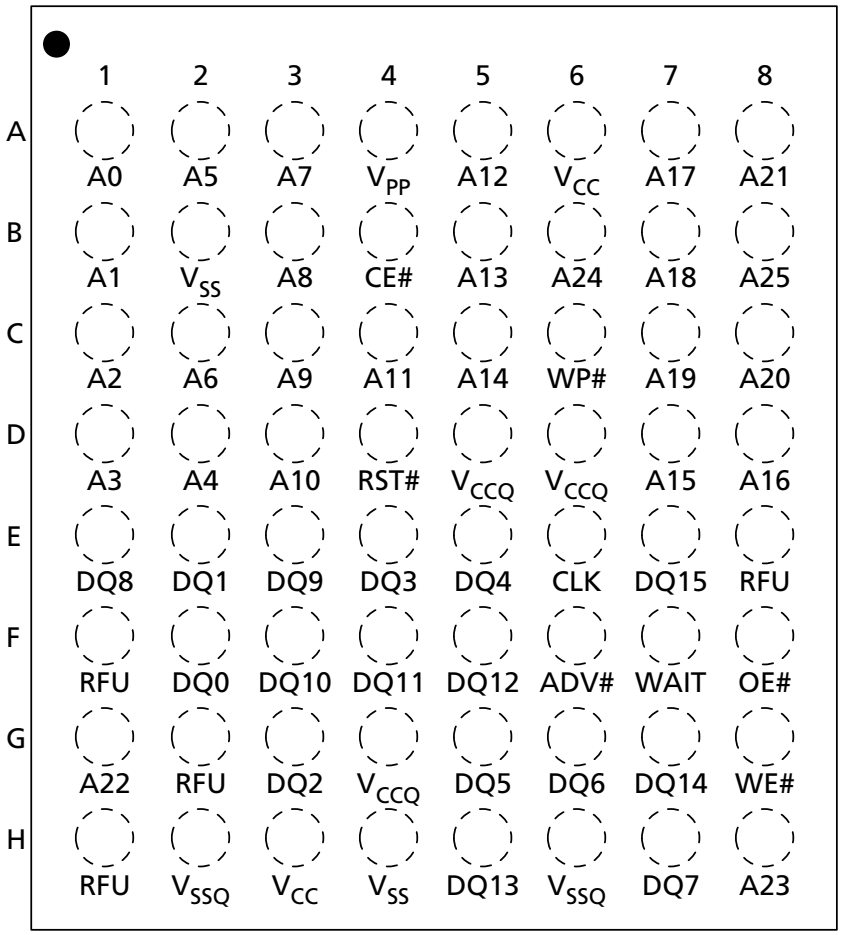
Figure 3: 64-Ball TBGA (10mm x 8mm x 1.2mm) – Package Code: GC



Note: 1. All dimensions are in millimeters.

Signal Assignments

Figure 4: 64-Ball Easy BGA (Top View, Balls Down)



Notes:
1. A0 is the least significant address bit.
2. H8 is A23 for 256Mb density and above; otherwise, it is a no connect (NC).
3. B6 is A24 for 512Mb densities and above; otherwise, it is a no connect (NC).
4. B8 is A25 for 1Gb density; otherwise, it is a no connect (NC).
5. For AA/D MUX configuration, the upper addresses A[MAX;16] must be connected to V_{SS}.

Signal Descriptions

Table 5: Signal Descriptions

Symbol	Type	Description
Non-MUX		
A[MAX:0]	Input	**Address inputs:** Address inputs for all READ/WRITE cycles.
DQ[15:0]	Input/Output	**Data:** Data or command inputs during WRITE cycles; data, status, or device information outputs during READ cycles.
A/D MUX		
A[MAX:16]	Input	**Address inputs:** Upper address inputs for all READ/WRITE cycles.
A/DQ[15:0]	Input/Output	**Address inputs or data:** Lower address inputs during the address phase for all READ/WRITE cycles; data or command inputs during WRITE cycles; data, status, or device information outputs during READ cycles.
Control Signals		
CE#	Input	**Chip enable:** LOW true input. When LOW, CE# selects the die; when HIGH, CE# deselects the die and places it in standby.
OE#	Input	**Output enable:** LOW true input. Must be LOW for READs and HIGH for WRITEs.
WE#	Input	**Write enable:** LOW true input. Must be LOW for WRITEs and HIGH for READs.
CLK	Input	**Clock:** Synchronizes burst READ operations with the host controller.
ADV#	Input	**Address valid:** LOW true input. When LOW, ADV# enables address inputs. For synchronous burst READs, address inputs are latched on the rising edge.
WP#	Input	**Write protect:** LOW true input. When LOW, WP# enables block lock down; when HIGH, WP# disables block lock down.
RST#	Input	**Reset:** LOW true input. When LOW, RST# inhibits all operations; must be HIGH for normal operations.
V_{PP}	Input	**Erase/program voltage:** Enables voltage for PROGRAM and ERASE operations. Array contents cannot be altered when V_{PP} is at or below V_{PPLK}.
WAIT	Output	**WAIT:** Configurable HIGH or LOW true output. When asserted, WAIT indicates DQ[15:0] is invalid; when de-asserted, WAIT indicates DQ[15:0] is valid.
V_{CC}	Power	**Core power:** Supply voltage for core circuits. All operations are inhibited when V_{CC} is at or below V_{LKO}.
V_{CCQ}	Power	**I/O power:** Supply voltage for all I/O drivers. All operations are inhibited when V_{CCQ} is at or below V_{LKOQ}.
V_{SS}	Power	**Logic ground:** Core logic ground return. Connect all V_{SS} balls to system ground; do not float any V_{SS} balls.
V_{SSQ}	Power	**I/O ground:** I/O driver ground return. Connect all V_{SSQ} balls to system ground; do not float any V_{SSQ} balls.
RFU	Reserved	**Reserved:** Reserved for future use and should not be connected.

Table 6: Address Mapping for Address/Data MUX Interface

Address Bit	A/D MUX Configuration (RCR Bit 4 = 0) and OE# = 1	AADM Mode (RCR Bit 4 = 1) and OE# = 1	AADM Mode (RCR Bit 4 = 1) and OE# = 0
A0	DQ0	A0	A16
A1	DQ1	A1	A17
A2	DQ2	A2	A18
A3	DQ3	A3	A19
A4	DQ4	A4	A20
A5	DQ5	A5	A21
A6	DQ6	A6	A22
A7	DQ7	A7	A23
A8	DQ8	A8	A24
A9	DQ9	A9	A25
A10	DQ10	A10	–
A11	DQ11	A11	–
A12	DQ12	A12	–
A13	DQ13	A13	–
A14	DQ14	A14	–
A15	DQ15	A15	–
A16	A16	–	–
A17	A17	–	–
A18	A18	–	–
A19	A19	–	–
A20	A20	–	–
A21	A21	–	–
A22	A22	–	–
A23	A23	–	–
A24	A24	–	–
A25	A25	–	–

Bus Interface

The bus interface uses CMOS-compatible address, data, and bus control signals for all bus WRITE and bus READ operations. The address signals are input only, the data signals are input/output (I/O), and the bus control signals are input only. The address inputs are used to specify the internal device location during bus READ and bus WRITE operations. The data I/Os carry commands, data, or status to and from the device. The control signals are used to select and deselect the device, indicate a bus READ or bus WRITE operation, synchronize operations, and reset the device.

Do not float any inputs. All inputs must be driven or terminated for proper device operation. Some features may use additional signals. See Signal Descriptions for descriptions of these signals.

The following table shows the logic levels that must be applied to the bus control signal inputs for the bus operations listed.

Table 7: Bus Control Signals

X = Don't Care; High = V_{IH}; Low = V_{IL}

Bus Operations	RST#	CE#	CLK	ADV#	OE#	WE#	Address	Data I/O
RESET	LOW	X	X	X	X	X	X	High-Z
STANDBY	HIGH	HIGH	X	X	X	X	X	High-Z
OUTPUT DISABLE	HIGH	X	X	X	HIGH	X	X	High-Z
Asynchronous READ	HIGH	LOW	X	LOW	LOW	HIGH	Valid	Output
Synchronous READ	HIGH	LOW	Running	Toggle	LOW	HIGH	Valid	Output
WRITE	HIGH	LOW	X	X	HIGH	LOW	Valid	Input

Reset

RST# LOW places the device in reset, where device operations are disabled; inputs are ignored, and outputs are placed in High-Z.

Any ongoing ERASE or PROGRAM operation will be aborted and data at that location will be indeterminate.

RST# HIGH enables normal device operations. A minimum delay is required before the device is able to perform a bus READ or bus WRITE operation. See AC specifications.

Standby

RST# HIGH and CE# HIGH place the device in standby, where all other inputs are ignored, outputs are placed in High-Z (independent of the level placed on OE#), and power consumption is substantially reduced.

Any ongoing ERASE or PROGRAM operation continues in the background and the device draws active current until the operation has finished.

Output Disable

When OE# is de-asserted with CE# asserted, the device outputs are disabled. Output pins are placed in High-Z. WAIT is de-asserted in A/D-MUX devices and driven to High-Z in non-MUX devices.

Asynchronous Read

For RCR15 = 1 (default), CE# LOW and OE# LOW place the device in asynchronous bus read mode:

- RST# and WE# must be held HIGH; CLK must be tied either HIGH or LOW.
- Address inputs must be held stable throughout the access, or latched with ADV#.
- ADV# must be held LOW or can be toggled to latch the address.
- Valid data is output on the data I/Os after ^{t}AVQV, ^{t}ELQV, ^{t}VLQV, or ^{t}GLQV, whichever is satisfied last.

Asynchronous READ operations are independent of the voltage level on V_{PP}.

For asynchronous page reads, subsequent data words are output ^{t}APA after the least significant address bit(s) are toggled: 16-word page buffer, A[3:0].

Synchronous Read

For RCR15 = 0, CE# LOW, OE# LOW, and ADV# LOW place the device in synchronous bus read mode:

- RST# and WE# must be held HIGH.
- CLK must be running.
- The first data word is output ^{t}CHQV after the latency count has been satisfied.
- For array reads, the next address data is output ^{t}CHQV after valid CLK edges until the burst length is satisfied.
- For nonarray reads, the same address data is output ^{t}CHQV after valid CLK edges until the burst length is satisfied.

The address for synchronous read operations is latched on the ADV# rising edge or the first rising CLK edge after ADV# LOW, whichever occurs first for devices that support up to 108 MHz. For devices that support up to 133 MHz, the address is latched on the last CLK edge when ADV# is LOW.

Burst Wrapping

Data stored within the memory array is arranged in rows or word lines. During synchronous burst reads, data words are sensed in groups from the array. The starting address of a synchronous burst read determines which word within the wordgroup is output first, and subsequent words are output in sequence until the burst length is satisfied.

The setting of the burst wrap bit (RCR3) determines whether synchronous burst reads will wrap within the wordgroup or continue on to the next wordgroup.

Figure 5: Main Array Word Lines

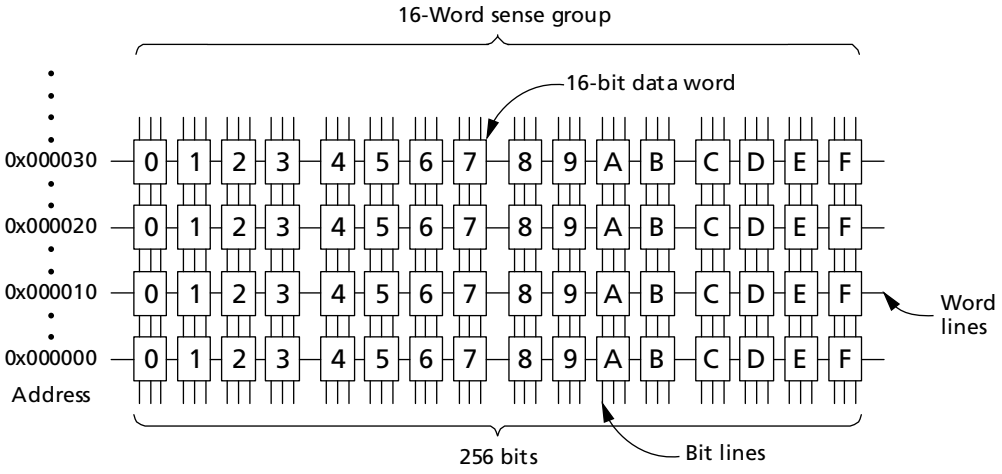
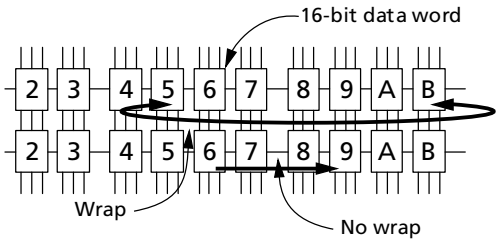


Figure 6: Wrap/No-Wrap Example

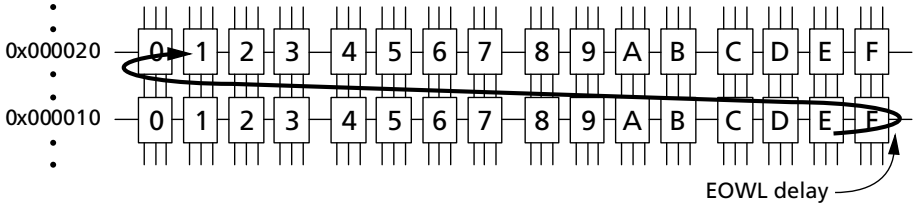


End-of-Wordline Delay

Output delays may occur when the burst sequence crosses the first end-of-wordline boundary onto the start of the next wordline.

No delays occur if the starting address is sense-group aligned or if the burst sequence never crosses a wordline boundary. However, if the starting address is not sense-group aligned, the worst-case end-of-wordline delay is one clock cycle less than the initial access latency count used. This delay occurs only once during the burst access. WAIT informs the system of this delay when it occurs.

Figure 7: End-of-Wordline Delay



Write

CE# LOW and WE# LOW place the device in bus write mode, where RST# and OE# must be HIGH, CLK and ADV# are ignored, input data and address are sampled on the rising edge of WE# or CE#, whichever occurs first.

During a WRITE operation in MUX devices, address is latched during the rising edge of ADV# OR CE# whichever occurs first and data is latched during the rising edge of WE# OR CE# whichever occurs first.

Bus WRITE cycles are asynchronous only.

The following conditions apply when a bus WRITE cycle occurs immediately before, or immediately after, a bus READ cycle:

- When transitioning from a bus READ cycle to a bus WRITE cycle, CE# or ADV# must toggle after OE# goes HIGH.
- When in synchronous read mode (RCR15 = 0; burst clock running), bus WRITE cycle timings ^{t}VHWL (ADV# HIGH to WE# LOW), ^{t}CHWL (CLK HIGH to WE# LOW), and ^{t}WHCH (WE# HIGH to CLK HIGH) must be met.
- When transitioning from a bus WRITE cycle to a bus READ cycle, CE# or ADV# must toggle after WE# goes HIGH.

Command Definitions

Commands are written to the device to control all operations. Some commands are two-cycle commands that use a SETUP and a CONFIRM command; other commands are single-cycle commands that use only a SETUP command followed by a data READ cycle or data WRITE cycle. Valid commands and their associated command codes are shown in the table below.

The device supports READ-While-WRITE and READ-While-ERASE operations with bus cycle granularity, not command granularity. That is, both bus WRITE cycles of a two-cycle command do not need to occur as back-to-back bus WRITE cycles to the device; READ cycles may occur between the two WRITE cycles of a two-cycle command.

However, a WRITE operation must not occur between the two bus WRITE cycles of a two-cycle command; this will cause a command sequence error (SR[7,5,4] = 1).

Due to the large buffer size of devices, the system interrupt latency may be impacted during the buffer fill phase of a buffered programming operation. Refer to the relevant technical note to implement a software solution.

Figure 8: Two-Cycle Command Sequence

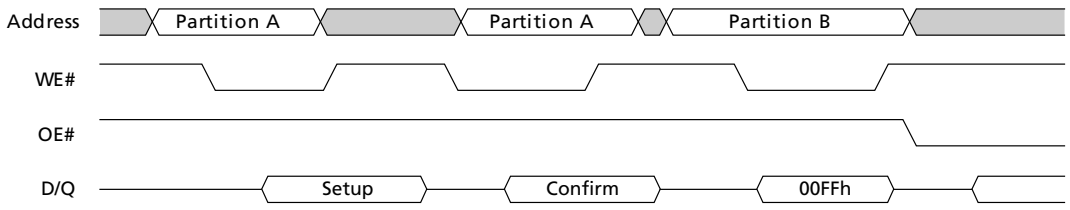


Figure 9: Single-Cycle Command Sequence

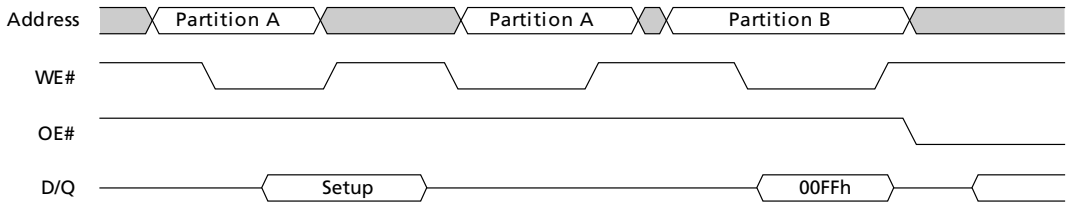


Figure 10: READ Cycle Between WRITE Cycles

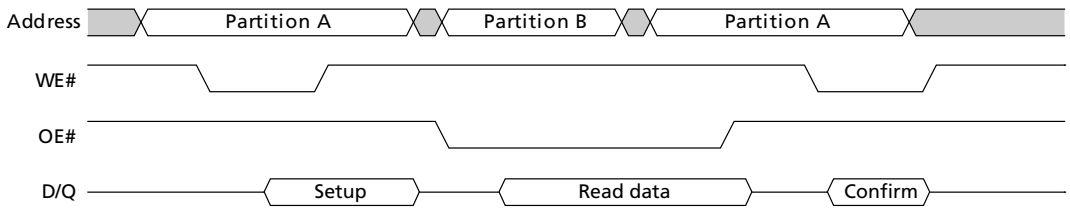


Figure 11: Illegal Command Sequence

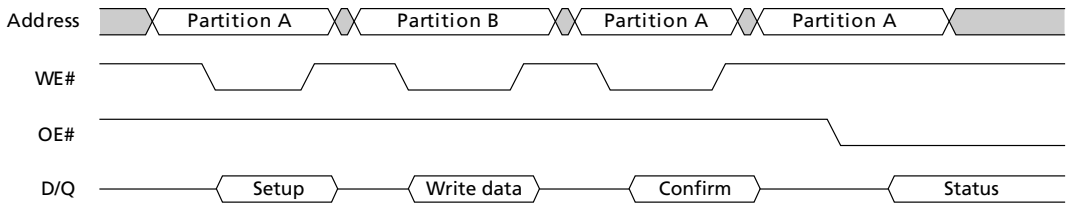


Table 8: Command Set

Command	Code (Setup/Confirm)	Description
Register Operations		
PROGRAM READ CONFIGURATION REGISTER	0060h/0003h	Programs the read configuration register. The desired read configuration register value is placed on the address bus, and written to the read configuration register when the CONFIRM command is issued.
PROGRAM EXTENDED CONFIGURATION REGISTER	0060h/0004h	Programs the extended configuration register. The desired extended configuration register value is placed on the address bus, and written to the read configuration register when the CONFIRM command is issued.
PROGRAM OTP AREA	00C0h	Programs OTP area and OTP lock registers. The desired register data is written to the addressed register on the next WRITE cycle.
CLEAR STATUS REGISTER	0050h	Clears all error bits in the status register.
Read Mode Operations		
READ ARRAY	00FFh	Places the addressed partition in read array mode. Subsequent reads outputs array data.
READ STATUS REGISTER	0070h	Places the addressed partition in read status mode. Subsequent reads outputs status register data.
READ ID	0090h	Places the addressed partition in read ID mode. Subsequent reads from specified address offsets output unique device information.
READ CFI	0098h	Places the addressed partition in read CFI mode. Subsequent reads from specified address offsets output CFI data.
Array Programming Operations		
SINGLE-WORD PROGRAM	0041h	Programs a single word into the array. Data is written to the array on the next WRITE cycle. The addressed partition automatically switches to read status register mode.
BUFFERED PROGRAM	00E9h/00D0h	Initiates and executes a BUFFERED PROGRAM operation. Additional bus READ/WRITE cycles are required between the and confirm commands to properly perform this operation. The addressed partition automatically switches to read status register mode.

Table 8: Command Set (Continued)

Command	Code (Setup/Confirm)	Description
BUFFERED ENHANCED FACTORY PROGRAM	0080h/00D0h	Initiates and executes a BUFFERED ENHANCED FACTORY PROGRAM operation. Additional bus READ/WRITE cycles are required after the CONFIRM command to properly perform this operation. The addressed partition automatically switches to read status register mode.
Block Erase Operations		
BLOCK ERASE	0020h/00D0h	Erases a single, addressed block. The ERASE operation commences when the CONFIRM command is issued. The addressed partition automatically switches to read status register mode.
Security Operations		
Lock Block	0060h/0001h	Sets the lock bit of the addressed block.
Unlock Block	0060h/00D0h	Clears the lock bit of the addressed block.
Lock-Down Block	0060h/002Fh	Sets the lock-down bit of the addressed block.
Other Operations		
SUSPEND	00B0h	Initiates a suspend of a PROGRAM or BLOCK ERASE operation already in progress when issued to any device address SR[6] = 1 indicates erase suspend SR[2] = 1 indicates program suspend
RESUME	00D0h	Resumes a suspended PROGRAM or BLOCK ERASE operation when issued to any device address. A program suspend nested within an erase suspend is resumed first.
BLANK CHECK	00BCh/00D0h	Performs a blank check of an addressed block. The addressed partition automatically switches to read status register mode.