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NAND Flash and Mobile LPDDR 168-Ball Package-on-Package (PoP) MCP Combination Memory (TI OMAP™)

MT29C4G48MAYBAAKQ-5 WT, MT29C4G48MAZBAAKQ-5 WT, MT29C4G96MAYBACJG-5 WT, MT29C4G96MAZBACJG-5 WT, MT29C8G96MAYBADJV-5 WT, MT29C8G96MAZBADJV-5 WT MT29C4G48MAZBAAKQ-5 IT, MT29C4G96MAZBACJG-5 IT MT29C8G96MAZBADJV-5 IT

Features

- Micron® NAND Flash and LPDDR components
- RoHS-compliant, "green" package
- Separate NAND Flash and LPDDR interfaces
- Space-saving multichip package/package-on-package combination
- Low-voltage operation (1.70–1.95V)
- Wireless temperature range: –25°C to +85°C
- Industrial temperature range: –40°C to +85°C

NAND Flash-Specific Features

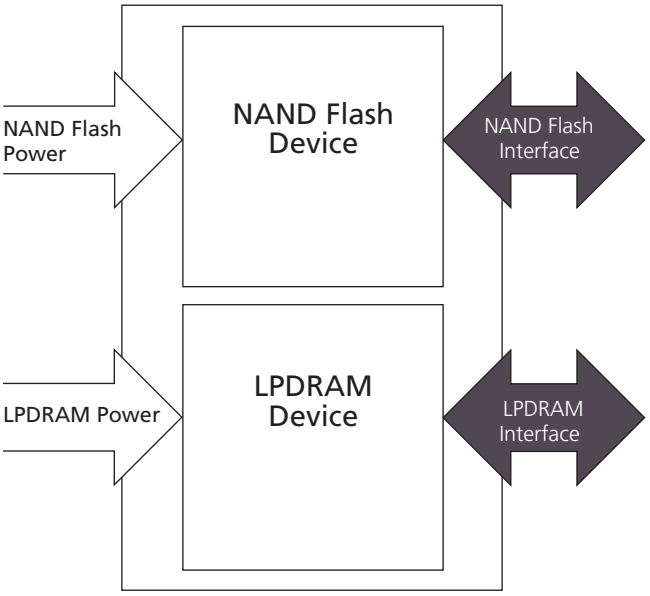
Organization
- Page size
  - x8: 2112 bytes (2048 + 64 bytes)
  - x16: 1056 words (1024 + 32 words)
- Block size: 64 pages (128K + 4K bytes)

Mobile LPDDR-Specific Features

- No external voltage reference required
- No minimum clock rate requirement
- 1.8V LVCMOS-compatible inputs
- Programmable burst lengths
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Selectable output drive strength
- STATUS REGISTER READ (SRR) supported[1]

Notes: 1. Contact factory for remapped SRR output.
2. For physical part markings, see on page .

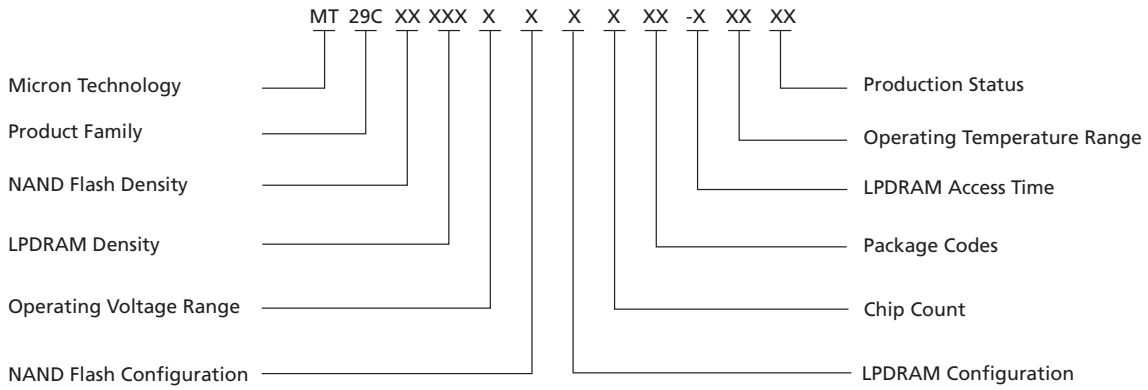
Figure 1: PoP Block Diagram



Part Numbering Information

Micron NAND Flash and LPDRAM devices are available in different configurations and densities. The MCP/PoP part numbering guide is available at www.micron.com/numbering.

Figure 2: Part Number Chart



Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

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MCP General Description

Micron package-on-package (PoP) MCP products combine NAND Flash and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The NAND Flash and Mobile LPDRAM devices are also members of the Micron discrete memory products portfolio.

The NAND Flash and Mobile LPDRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile LPDRAM buses. The NAND Flash and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, V_{SS} is tied together on the two devices).

The bus architecture of this device also supports separate NAND Flash and Mobile LPDRAM functionality without concern for device interaction.

Ball Assignments and Descriptions

Figure 3: 168-Ball VFBGA (NAND x8, x16; LPDDR x32) Ball Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	(DNU)	(DNU)	DQ17	V_{DDQ}	DQ19	DM2	V_{DDQ}	DQ21	DQ23	V_{DDQ}	CK	V_{DD}	DQ9	DQ11	V_{DDQ}	DQ13	DM1	V_{DDQ}	DQ15	DM3	DQ25	(DNU)	(DNU)	A
B	(DNU)	(DNU)	DQ16	V_{SSQ}	DQ18	DQS2	V_{SSQ}	DQ20	DQ22	V_{SSQ}	CK#	V_{SS}	DQ8	DQ10	V_{SSQ}	DQ12	DQS1	V_{SSQ}	DQ14	DQS3	DQ24	(DNU)	(DNU)	B
C	DM0	DQS0																				V_{SSQ}	V_{DDQ}	C
D	DQ7	DQ6																				DQ26	DQ27	D
E	V_{DDQ}	V_{SSQ}																				DQ28	DQ29	E
F	DQ5	DQ4																				V_{SSQ}	V_{DDQ}	F
G	DQ3	DQ2																				DQ30	DQ31	G
H	V_{DDQ}	V_{SSQ}																				V_{SS}	V_{DD}	H
J	DQ1	DQ0																				CKE0	CKE1	J
K	V_{DD}	V_{SS}																				V_{SS}	WE#	K
L	V_{CC}	V_{SS}																				CAS#	RAS#	L
M	I/O1	I/O0																				CS0#	CS1#	M
N	I/O3	I/O2																				A0	A1	N
P	V_{CC}	V_{SS}																				A2	A3	P
R	I/O5	I/O4																				A4	A5	R
T	I/O7	I/O6																				A6	A7	T
U	V_{CC}	V_{SS}																				A8	A9	U
V	WE#	RE#																				A10	A11	V
W	ALE	(NC)																				A12	A13	W
Y	CE1#	CE0#																				A14	V_{DD}	Y
AA	V_{CC}	V_{SS}																				V_{SS}	V_{DD}	AA
AB	(DNU)	(DNU)	I/O8	I/O10	V_{SS}	I/O12	I/O14	V_{SS}	LOCK	WP#	(NC)	R/B#	V_{SS}	V_{SS}	(NC)	(NC)	(NC)	(NC)	(NC)	V_{SS}	BA0	(DNU)	(DNU)	AB
AC	(DNU)	(DNU)	I/O9	I/O11	V_{CC}	I/O13	I/O15	V_{CC}	(NC)	(NC)	(NC)	CLE	V_{CC}	TQ	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	BA1	(DNU)	(DNU)	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Top View – Ball Down

NAND LPDDR Supply Ground

Table 1: x8, x16 NAND Ball Descriptions

Symbol	Type	Description
ALE	Input	Address latch enable: When ALE is HIGH, addresses can be transferred to the on-chip address register.
CE0#, CE1#	Input	Chip enable: Gates transfers between the host system and the NAND device. CE1# is used when a second CE# is required and is RFU[1] in all other configurations.
CLE	Input	Command latch enable: When CLE is HIGH, commands can be transferred to the on-chip command register.
LOCK	Input	When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable BLOCK LOCK, connect LOCK to V_{SS} during power-up, or leave it unconnected (internal pull-down).
RE#	Input	Read enable: Gates information from the NAND device to the host system.
WE#	Input	Write enable: Gates information from the host system to the NAND device.
WP#	Input	Write protect: Driving WP# LOW blocks ERASE and PROGRAM operations.
I/O[15:0]	Input/ output	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs. I/O[15:8] are RFU for x8 NAND devices.
R/B#	Output	Ready/busy: Open-drain, active-LOW output that indicates when an internal operation is in progress.
V_{CC}	Supply	V_{CC}: NAND power supply.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 2: x32 LPDDR Ball Descriptions

Symbol	Type	Description
A[14:0]	Input	Address inputs: Specifies the row or column address. Also used to load the mode registers. The maximum LPDDR address is determined by density and configuration. Consult the LPDDR product data sheet for the maximum address for a given density and configuration. Unused address balls become RFU.[1]
BA0, BA1	Input	Bank address inputs: Specifies one of the 4 banks.
CAS#	Input	Column select: Specifies which command to execute.
CK, CK#	Input	CK is the system clock. CK and CK# are differential clock inputs. All address and control signals are sampled and referenced on the crossing of the rising edge of CK with the falling edge of CK#.
CKE0, CKE1	Input	Clock enable. CKE0 is used for a single LPDDR product. CKE1 is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
CS0#, CS1#	Input	Chip select: CS0# is used for a single LPDDR product. CS1# is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
DM[3:0]	Input	Data mask: Determines which bytes are written during WRITE operations.
RAS#	Input	Row select: Specifies the command to execute.
WE#	Input	Write enable: Specifies the command to execute.
DQ[31:0]	Input/ output	Data bus: Data inputs/outputs.
DQS[3:0]	Input/ output	Data strobe: Coordinates READ/WRITE transfers of data; one DQS per DQ byte.
TQ	Output	Temperature sensor output: TQ HIGH when LPDDR T_J exceeds 85°C.
V_{DD}	Supply	V_{DD}: LPDDR power supply.
V_{DDQ}	Supply	V_{DDQ}: LPDDR I/O power supply.
V_{SSQ}	Supply	V_{SSQ}: LPDDR I/O ground.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 3: Non-Device-Specific Descriptions

Symbol	Type	Description
V_{SS}	Supply	V_{SS}: Shared ground.
Symbol	**Type**	**Description**
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.
RFU[1]	–	Reserved for future use.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Electrical Specifications

Table 4: Absolute Maximum Ratings

Parameters/Conditions	Symbol	Min	Max	Unit
V_{CC}, V_{DD}, V_{DDQ} supply voltage relative to V_{SS}	V_{CC}, V_{DD}, V_{DDQ}	–1.0	2.4	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.5	2.4 or (supply voltage[1] + 0.3V), whichever is less	V
Storage temperature range		–55	+150	°C

Note: 1. Supply voltage references V_{CC}, V_{DD}, or V_{DDQ}.

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5: Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}, V_{DD}	1.70	1.80	1.95	V
I/O supply voltage	V_{DDQ}	1.70	1.80	1.95	V
Operating temperature range	–	–25	–	+85	°C

Device Diagrams

Figure 4: 168-Ball (Single LPDDR) Functional Block Diagram

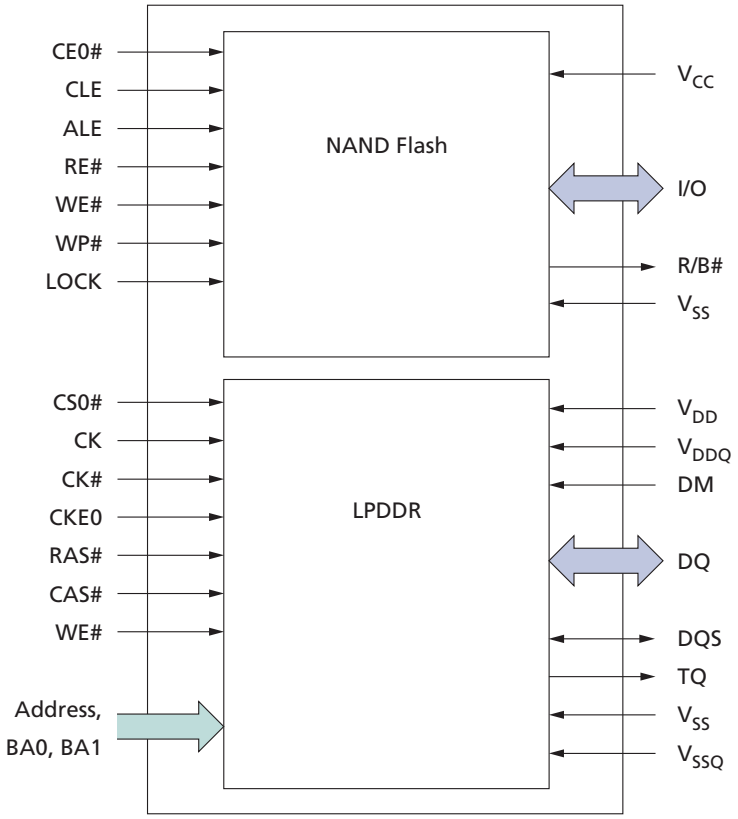
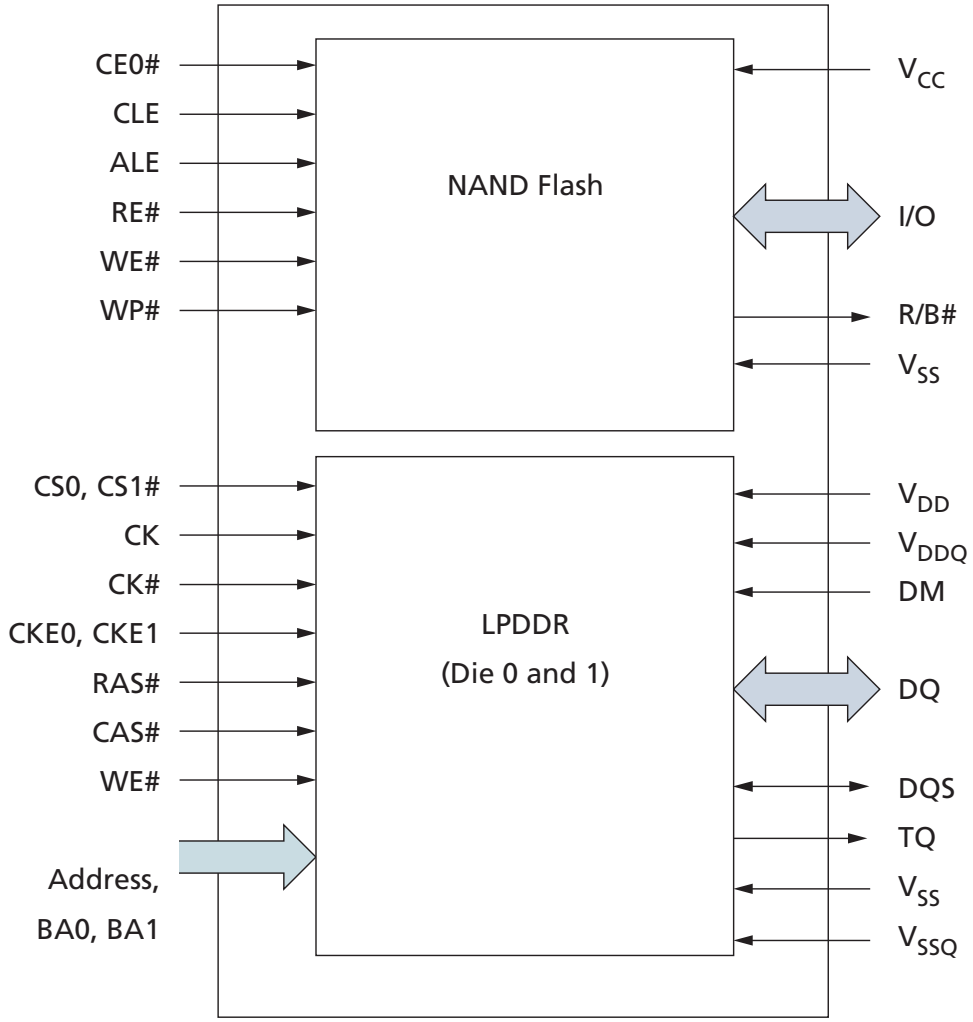
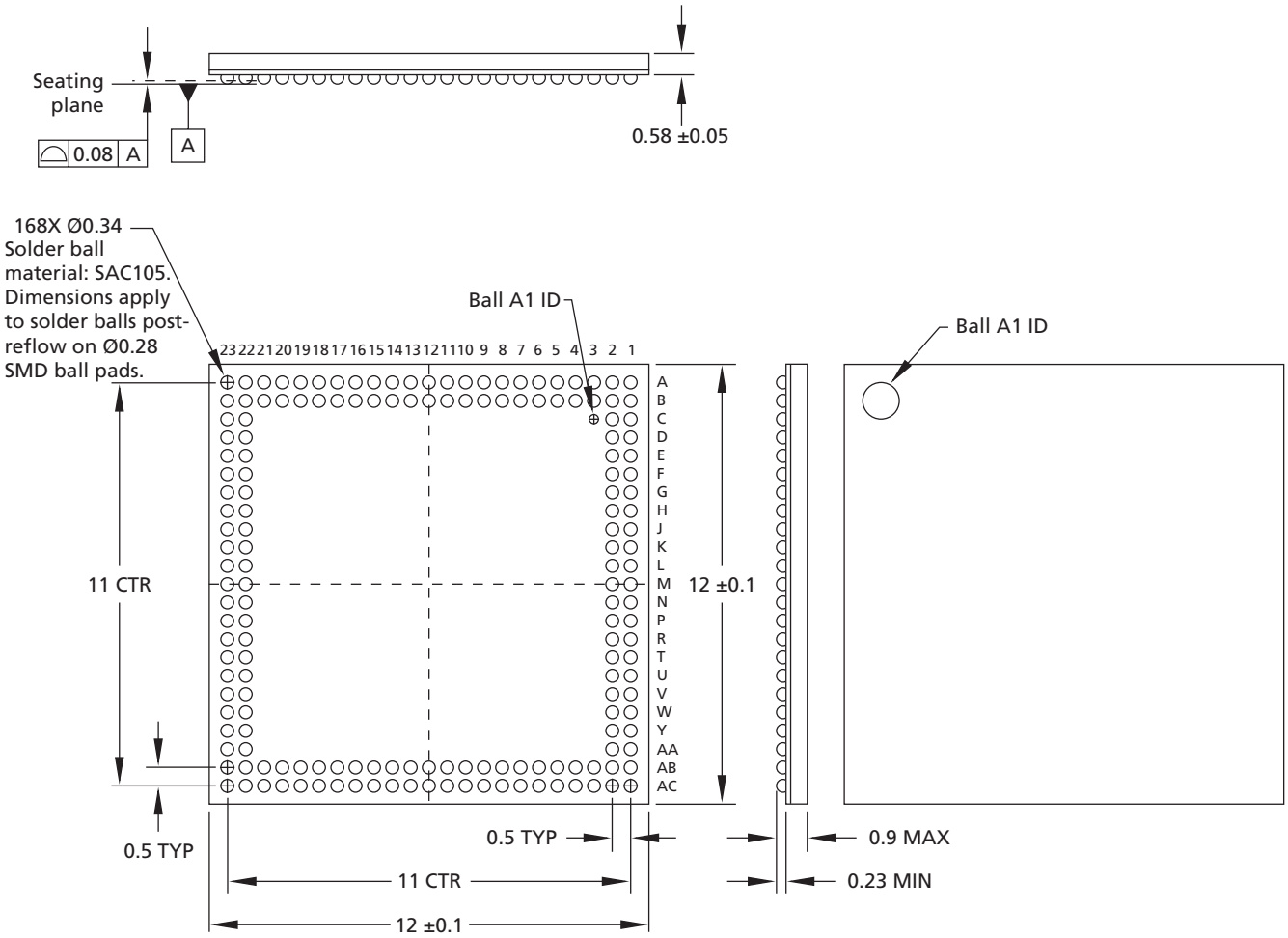


Figure 5: 168-Ball (Dual LPDDR) Functional Block Diagram



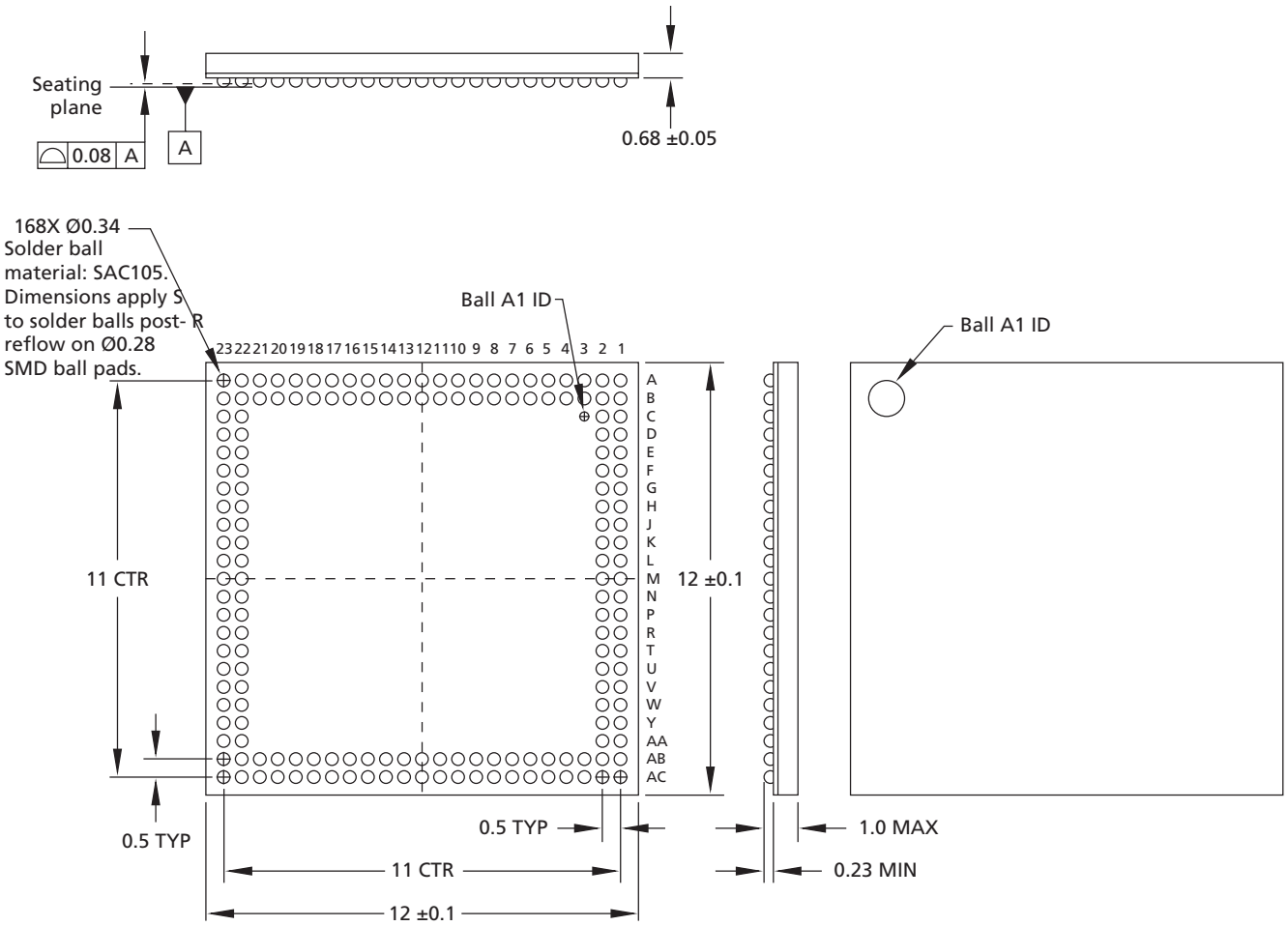
Package Dimensions

Figure 6: 168-Ball VFBGA (Package Code: JG)



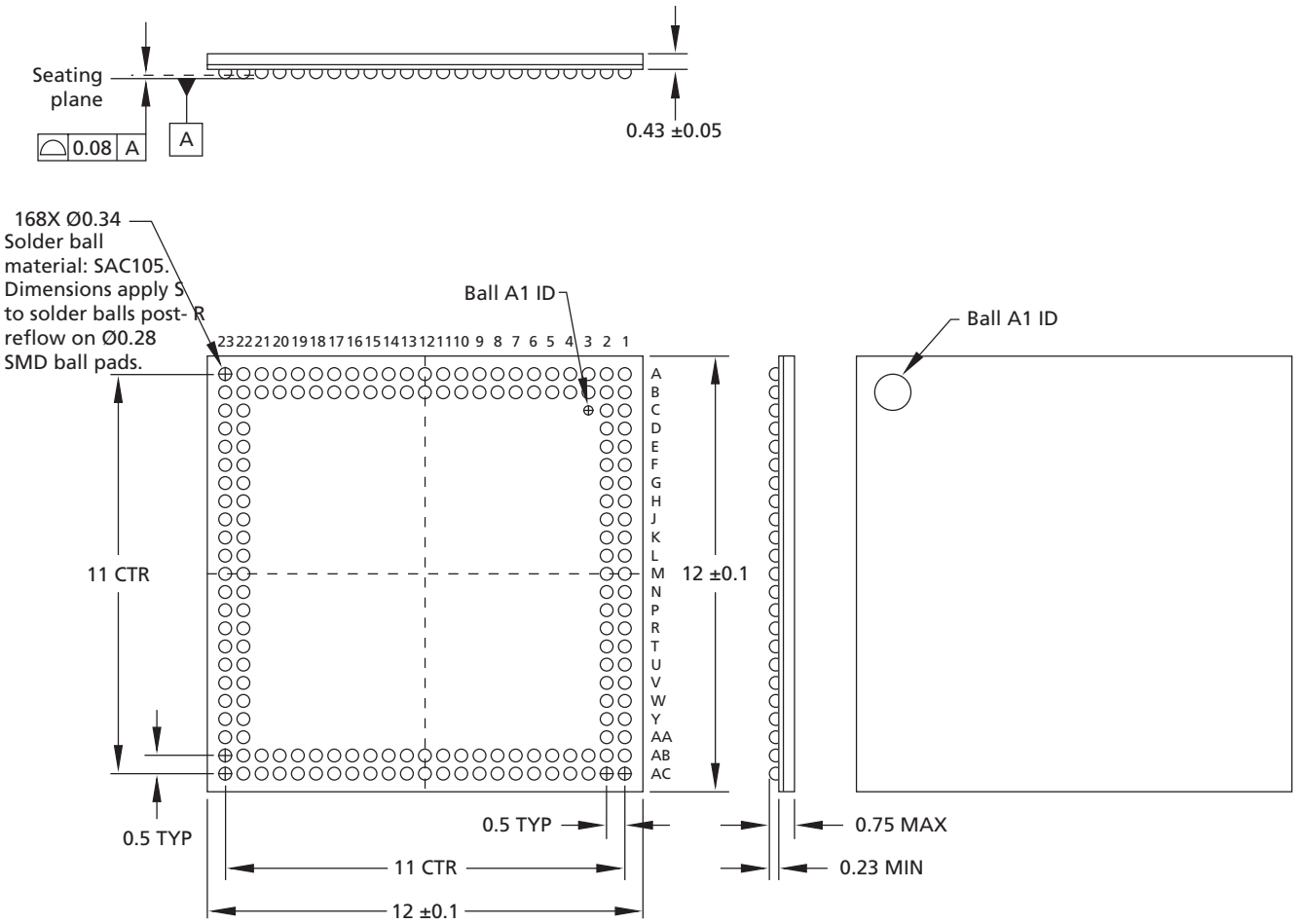
Note: 1. All dimensions are in millimeters.

Figure 7: 168-Ball VFBGA (Package Code: JV)



Note: 1. All dimensions are in millimeters.

Figure 8: 168-Ball WFBGA (Package Code: KQ)



Note: 1. All dimensions are in millimeters.

4Gb, 8Gb: x8, x16 NAND Flash Memory

Features

- Open NAND Flash Interface (ONFI) 1.0-compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 2112 bytes (2048 + 64 bytes)
  - Page size x16: 1056 words (1024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Plane size: 2 planes x 2048 blocks per plane
  - Device size: 4Gb: 4096 blocks; 8Gb: 8192 blocks
- Asynchronous I/O performance
  - ^{t}RC/^{t}WC: 20ns (3.3V), 25ns (1.8V)
- Array performance
  - Read page: 25µs[2]
  - Program page: 200µs (TYP: 1.8V, 3.3V)[2]
  - Erase block: 700µs (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced command set
  - Program page cache mode[3]
  - Read page cache mode[3]
  - One-time programmable (OTP) mode
  - Two-plane commands[3]
  - Interleaved die (LUN) operations
  - Read unique ID
  - Block lock (1.8V only)
  - Internal data move
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- Blocks 0–15 (block addresses 00h–0Fh) are valid when shipped from factory with ECC; for minimum required ECC, see Error Management
- Block 0 requires 1-bit ECC if PROGRAM/ERASE cycles are less than 1000
- RESET (FFh) required as first command after power-on
- Alternate method of device initialization (Nand_Init) after power-up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: 10 years
- Operating voltage range
  - V_{CC}: 2.7–3.6V
  - V_{CC}: 1.7–1.95V
- Operating temperature
  - Commercial: 0°C to +70°C
  - Industrial (IT): –40°C to +85°C

Notes: 1. The ONFI 1.0 specification is available at www.onfi.org.

2. See Electrical Specifications – Program/Erase Characteristics (page 122) for ^{t}R_ECC and ^{t}PROG_ECC specifications.
3. These commands supported only with ECC disabled.

General Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization.

This device has an internal 4-bit ECC that can be enabled using the GET/SET features. See Internal ECC and Spare Area Mapping for ECC for more information.

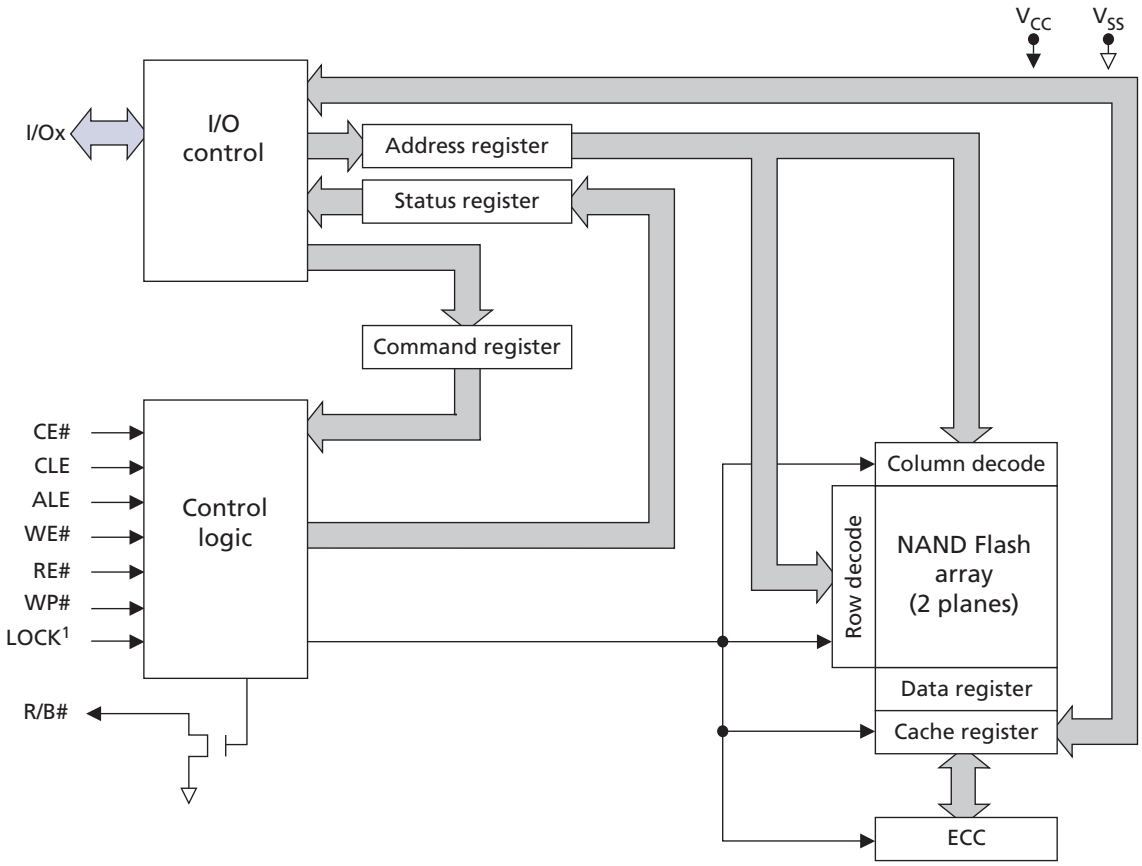
Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte (x8) or word by word (x16), through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput. The status register reports the status of die operations.

Figure 9: NAND Flash Die (LUN) Functional Block Diagram



Note: 1. The LOCK pin is used on the 1.8V device.

Device and Array Organization

Figure 10: Array Organization – MT29F4G08 (x8)

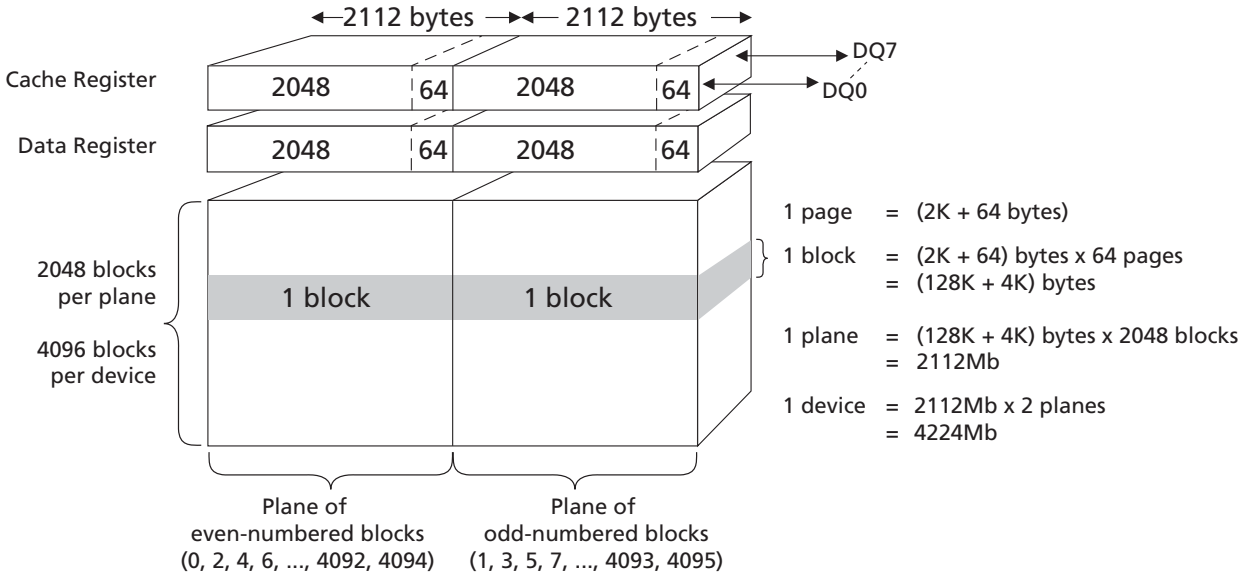


Table 6: Array Addressing – MT29F4G08 (x8)

Cycle	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes:
1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 is 1, then CA[10:6] must be 0.
3. BA6 controls plane selection.