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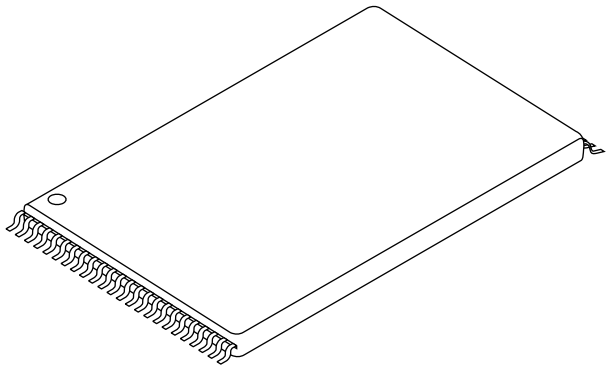
NAND Flash Memory

MT29F4G08AAA, MT29F8G08BAA, MT29F8G08DAA, MT29F16G08FAA

Features

- Single-level cell (SLC) technology
- Organization
  - Page size x8: 2,112 bytes (2,048 + 64 bytes)
  - Block size: 64 pages (128K + 4K bytes)
  - Plane size: 2,048 blocks
  - Device size: 4Gb: 4,096 blocks; 8Gb: 8,192 blocks; 16Gb: 16,384 blocks
- READ performance
  - Random READ: 25µs (MAX)
  - Sequential READ: 25ns (MIN)
- WRITE performance
  - PROGRAM PAGE: 220µs (TYP)
  - BLOCK ERASE: 1.5ms (TYP)
- Data retention: 10 years
- Endurance: 100,000 PROGRAM/ERASE cycles
- First block (block address 00h) guaranteed to be valid up to 1,000 PROGRAM/ERASE cycles[1]
- Industry-standard basic NAND Flash command set
- Advanced command set:
  - PROGRAM PAGE CACHE MODE
  - PAGE READ CACHE MODE
  - One-time programmable (OTP) commands
  - Two-plane commands
  - Interleaved die operations
  - READ UNIQUE ID (contact factory)
  - READ ID2 (contact factory)
- Operation status byte provides a software method of detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: write protect entire device
- RESET required after power-up
- INTERNAL DATA MOVE operations supported within the plane from which data is read

Figure 1: 48-Pin TSOP Type 1



Options

- Density[2]
  - 4Gb (single die)
  - 8Gb (dual-die stack 1 CE#)
  - 8Gb (dual-die stack 2 CE#)
  - 16Gb (quad-die stack)
- Device width: x8
- Configuration

# of die	# of CE#	# of R/B#	I/O
1	1	1	Common
2	1	1	Common
2	2	2	Common
4	2	2	Common

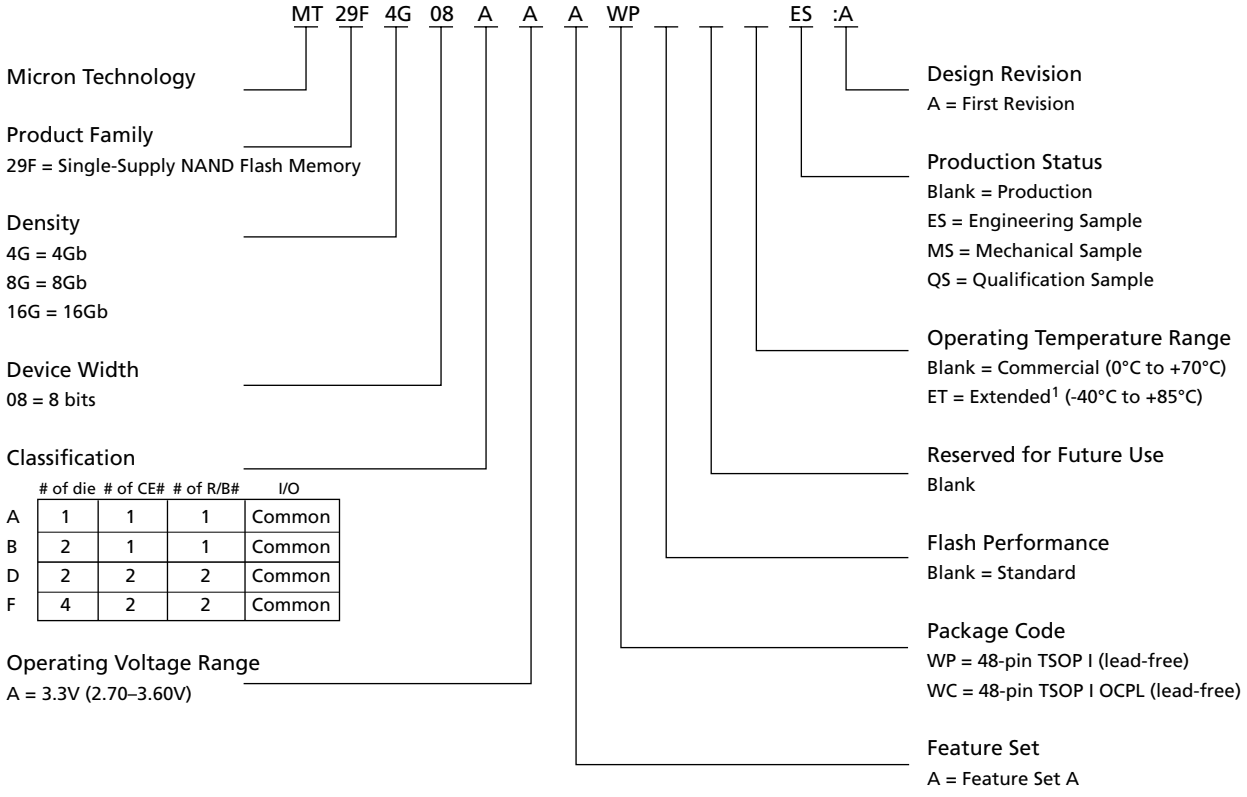
- V_{CC}: 2.7–3.6V
- Package
  - 48 TSOP type I (lead-free plating)
  - 48 TSOP type I OCPL[3] (lead-free plating)
- Operating temperature
  - Commercial (0°C to +70°C)
  - Extended (–40°C to +85°C)[4]

Notes: 1. For further details, see “Error Management” on page 58.
2. For part numbering and markings, see Figure 2 on page 2.
3. OCPL = off-center parting line.
4. For ET devices, contact factory.

Part Numbering Information

Micron® NAND Flash devices are available in several different configurations and densities (see Figure 2).

Figure 2: Part Number Chart



Notes: 1. For ET devices, contact factory.

Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part number is offered and valid by using the Micron Parametric Part Search Web site at www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

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General Description

NAND Flash technology provides a cost-effective solution for applications requiring high-density, solid-state storage. The MT29F4G08AAA is a 4Gb NAND Flash memory device. The MT29F8G08BAA is a two-die stack that operates as a single 8Gb device. The MT29F8G08DAA is a two-die stack that operates as two independent 4Gb devices. The MT29F16G08FAA is a four-die stack that operates as two independent 8Gb devices, providing a total storage capacity of 16Gb in a single, space-saving package. Micron NAND Flash devices include standard NAND Flash features as well as new features designed to enhance system-level performance.

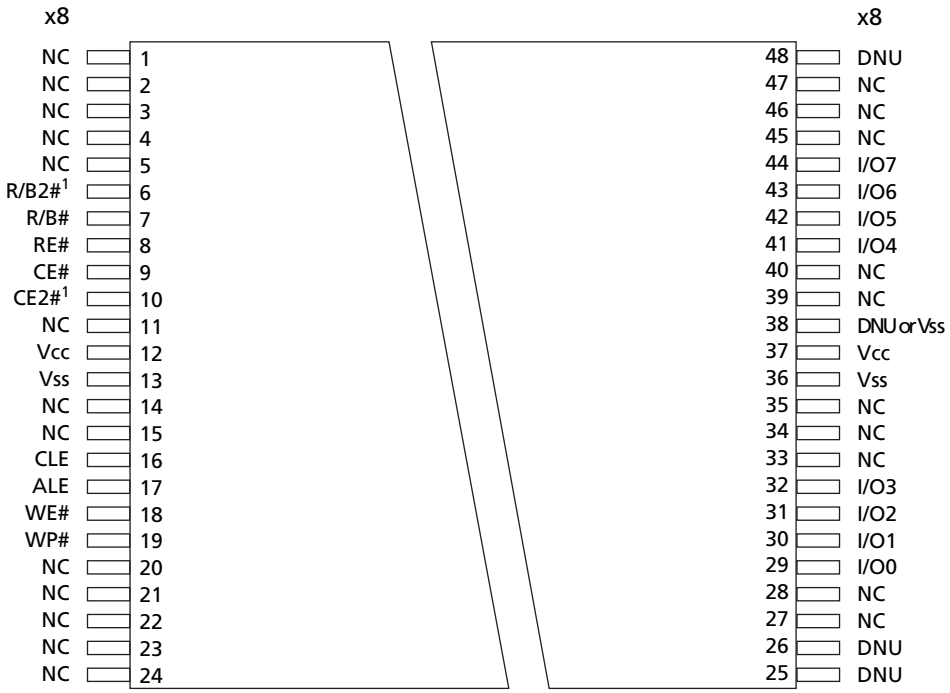
Micron NAND Flash devices use a highly multiplexed 8-bit bus (I/O[7:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND Flash command bus interface protocol. Additional pins control hardware write protection (WP#) and monitor device status (R/B#).

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

The MT29F4G, MT29F8G, and MT29F16G devices contain two planes per die. Each plane consists of 2,048 blocks. Each block is subdivided into 64 programmable pages. Each page consists of 2,112 bytes. The pages are further divided into a 2,048-byte data storage region with a separate 64-byte area. The 64-byte area is typically used for error management functions.

The contents of each page can be programmed in 220µs (TYP), and an entire block can be erased in 1.5ms (TYP). On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. PROGRAM/ERASE endurance is specified at 100,000 cycles with appropriate error correction code (ECC) and error management.

Figure 3: 48-Pin TSOP Type 1 Pin Assignment (Top View)



Notes: 1. CE2# and R/B2# are available on 8Gb 2-CE# devices and 16Gb devices only. These pins are NC for other configurations.

Table 1: Signal Descriptions

Symbol	Type	Description
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#, CE2#	Input	Chip enable: Gates transfers between the host system and the NAND Flash device. After the device starts a PROGRAM or ERASE operation, CE# can be de-asserted. For the 8Gb configuration, CE# controls the first 4Gb of memory; CE2# controls the second 4Gb of memory. For the 16Gb configuration, CE# controls the first 8Gb of memory; CE2# controls the second 8Gb. See "Bus Operation" on page 15 for additional operational details.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
RE#	Input	Read enable: Gates transfers from the NAND Flash device to the host system.
WE#	Input	Write enable: Gates transfers from the host system to the NAND Flash device.
WP#	Input	Write protect: Protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.
I/O[7:0] (x8)	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#, R/B2#	Output	Ready/busy: An open-drain, active-LOW output, that uses an external pull-up resistor. R/B# is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during READ operations to indicate when data is being transferred from the array into the serial data register. When these operations have completed, R/B# returns to the High-Z state. In the 8Gb configuration, R/B# is for the 4Gb of memory enabled by CE#; R/B2# is for the 4Gb of memory enabled by CE2#. In the 16Gb configuration, R/B# is for the 8Gb of memory enabled by CE#; R/B2# is for the 8Gb of memory enabled by CE2#.
V_{CC}	Supply	V_{CC}: Power supply.
V_{SS}	Supply	V_{SS}: Ground connection.
NC	–	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	–	Do not use: DNUs must be left unconnected.

Architecture

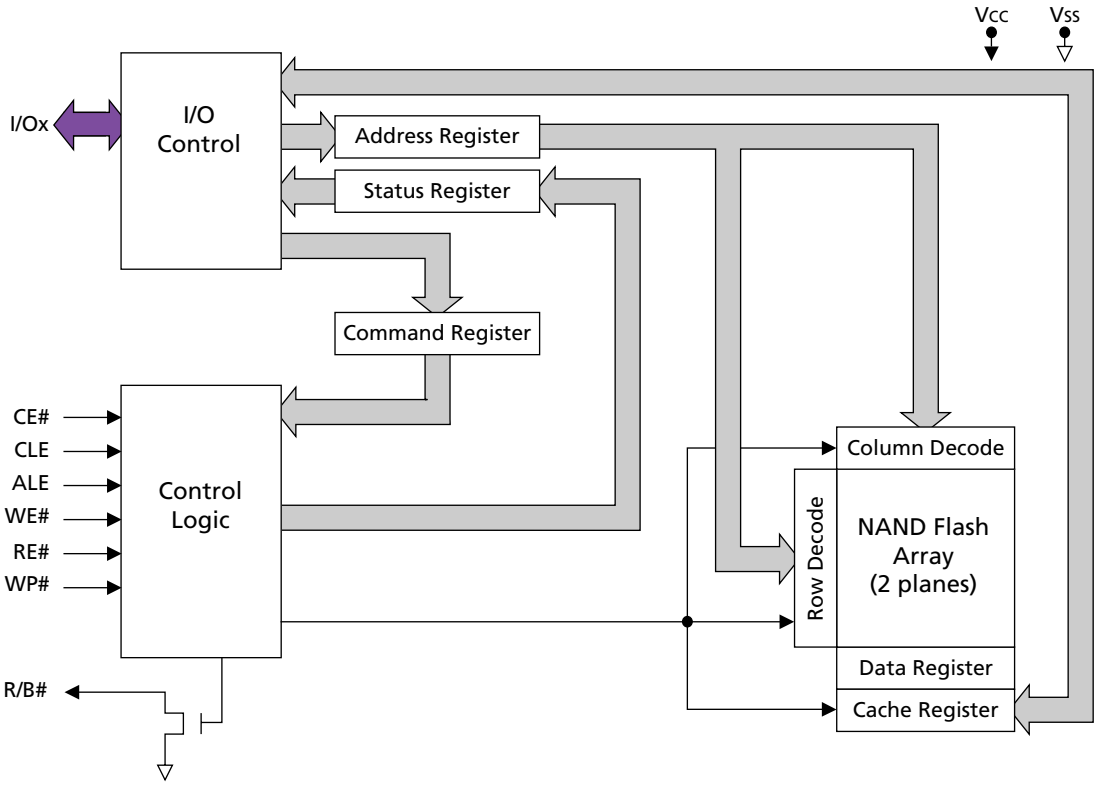
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. This provides a memory device with a low pin count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder or a column decoder to select a row address or a column address, respectively.

The data are transferred to or from the NAND Flash memory array, byte by byte (x8), through a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data, whereas the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations and is erased in block-based operations. During normal page operations, the data and cache registers are tied together and act as a single register. During cache operations the data and cache registers operate independently to increase data throughput.

These devices also have a status register that reports the status of device operation.

Figure 4: NAND Flash Functional Block Diagram



Addressing

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a 5-cycle sequence as shown in Tables 3 and 4, on pages 13 and 14. See Figure 5 for additional memory mapping and addressing details.

Memory Mapping

Figure 5: Memory Map

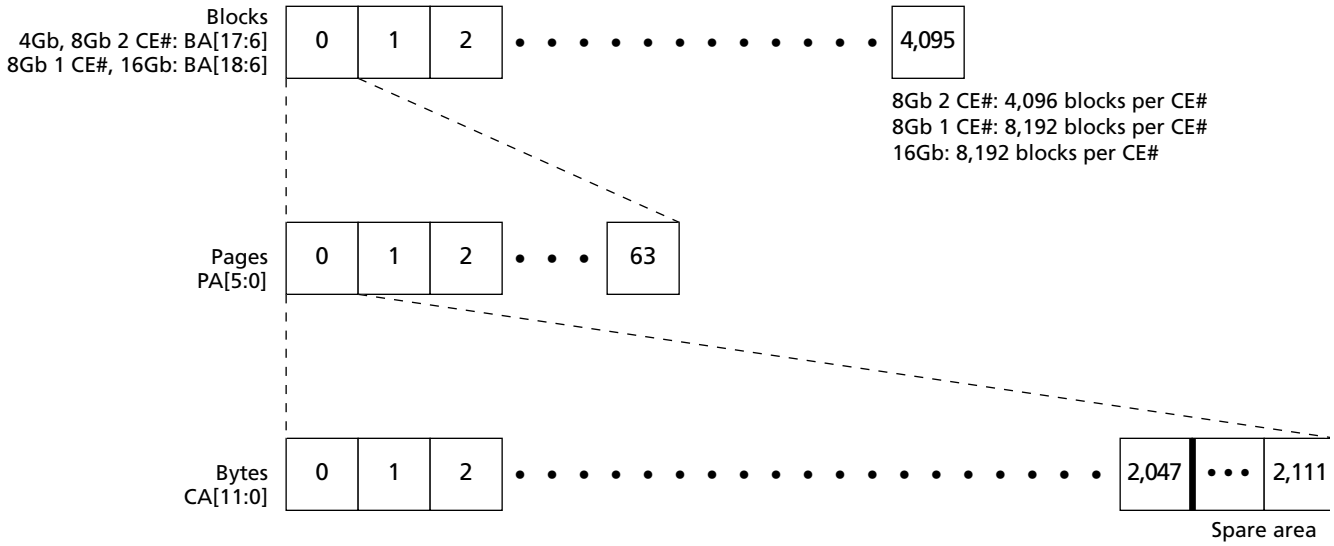


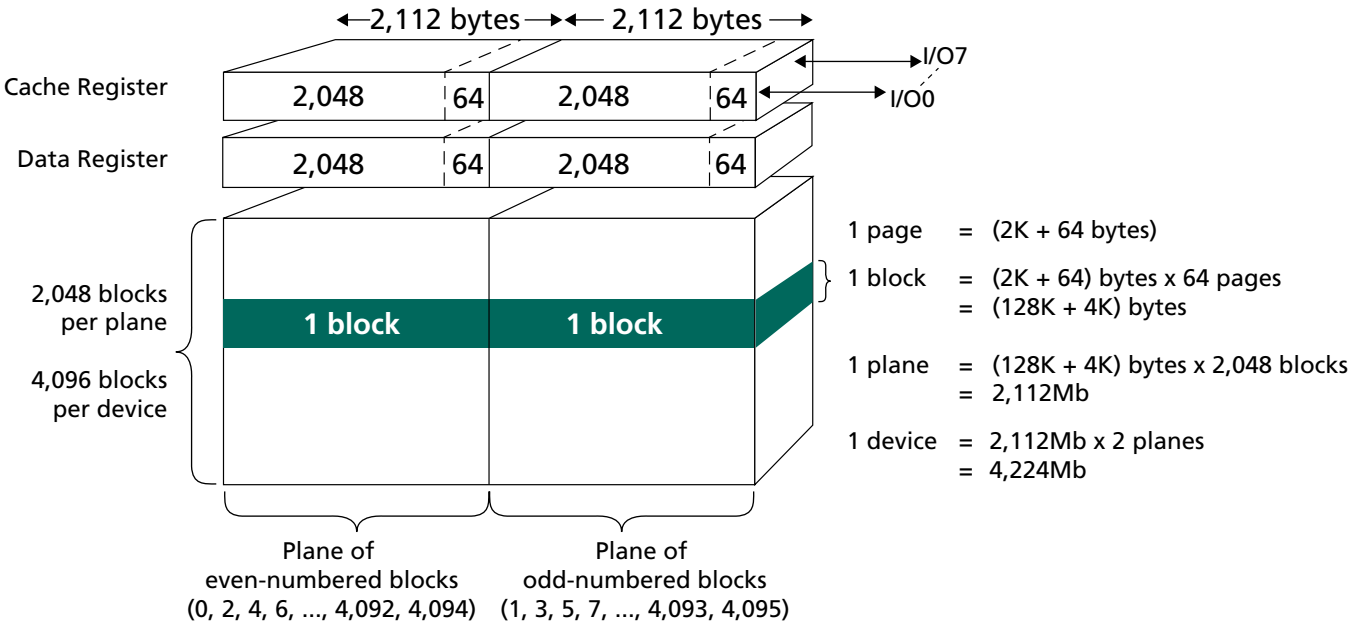
Table 2: Operational Example

Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x000000083F	0x0000000840–0x0000000FFF
0	1	0x0000010000	0x000001083F	0x0000010840–0x0000010FFF
0	2	0x0000020000	0x000002083F	0x0000020840–0x0000020FFF
…	…	…	…	
4,095	62	0x03FFFE0000	0x03FFFE083F	0x03FFFE0840–0x03FFFE0FFF
4,095	63	0x03FFFF0000	0x03FFFF083F	0x03FFFF0840–0x03FFFF0FFF

Notes:
1. As shown in Table 3 on page 13, the high nibble of ADDRESS cycle 2 has no assigned address bits; however, these 4 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.
2. The 12-bit column address is capable of addressing from 0 to 4,095 bytes on a x8 device; however, only bytes 0 through 2,111 are valid. Bytes 2,112 through 4,095 of each page are "out of bounds," do not exist in the device, and cannot be addressed.

Array Organization

Figure 6: Array Organization for MT29F4G08AAA and MT29F8G08DAA (x8)



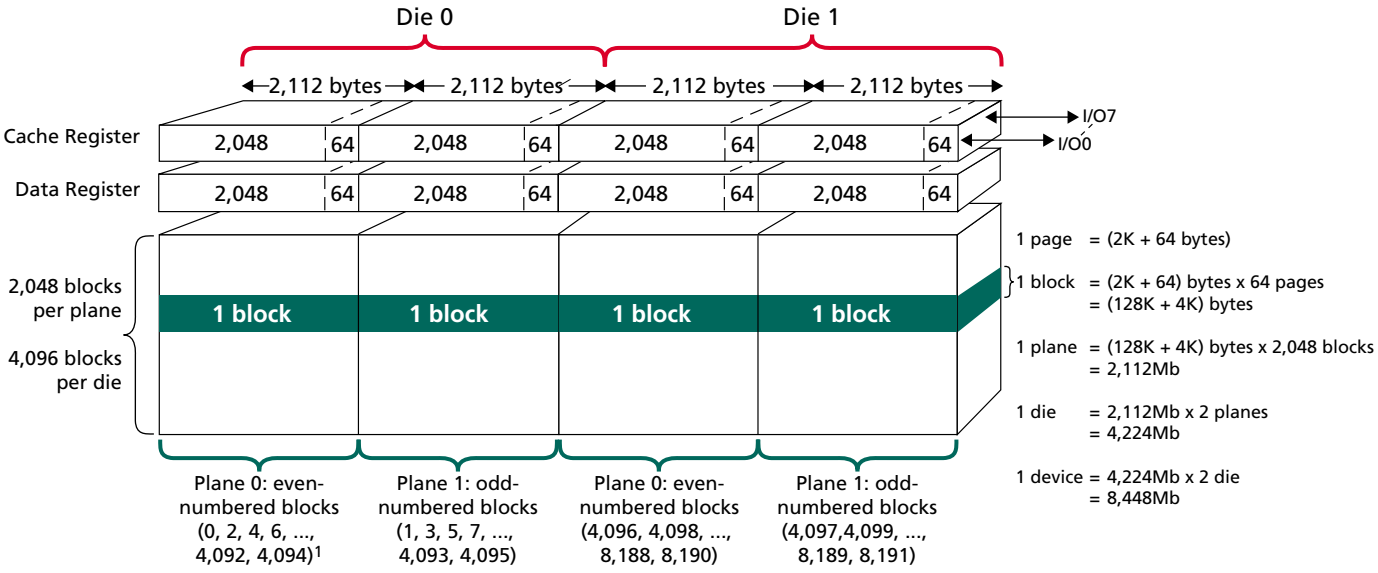
Notes: 1. For the 8Gb MT29F8G08DAA, the 4Gb array organization shown applies to each chip enable (CE# and CE2#).

Table 3: Array Addressing: MT29F4G08AAA and MT29F8G08DAA

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes: 1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 is "1," then CA[10:6] must be "0."

Figure 7: Array Organization for MT29F8G08BAA and MT29F16G08FAA (x8)



Notes:
1. Die 0, Plane 0: BA18 = 0; BA6 = 0.
   Die 0, Plane 1: BA18 = 0; BA6 = 1.
   Die 1, Plane 0: BA18 = 1; BA6 = 0.
   Die 1, Plane 1: BA18 = 1; BA6 = 1.
2. For the 16Gb MT29F16G08FAA, the 8Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 4: Array Addressing: MT28F8G08BAA and MT29F16G08FAA

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	BA18[3]	BA17	BA16

Notes:
1. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 is 1, then CA[10:6] must be "0."
3. Die address boundary: 0 = 0–4Gb; 1 = 4Gb–8Gb.

Bus Operation

The bus on MT29Fxxx devices is multiplexed. Data I/O, addresses, and commands all share the same pins, I/O[7:0].

The command sequence normally consists of a COMMAND LATCH cycle, ADDRESS INPUT cycles, and 1 or more DATA cycles—either READ or WRITE.

Control Signals

CE#, WE#, RE#, CLE, ALE, and WP# control NAND Flash device READ and WRITE operations. On the 8Gb MT29F8G08DAA, CE# and CE2# each control independent 4Gb arrays. On the 16Gb MT29F16G08FAA, CE# and CE2# each control independent 8Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the NAND Flash memory will accept command, address, and data information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 61 on page 69 and Figure 69 on page 75 for examples of CE# "Don't Care" operations.

The CE# "Don't Care" operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- The device is not busy

As exceptions, the device accepts the READ STATUS, TWO-PLANE/MULTIPLE-DIE READ STATUS, and RESET commands when busy. Commands are transferred to the command register on the rising edge of WE# (see Figure 53 on page 65). Commands are input on I/O[7:0].

Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are LOW, and
- ALE is HIGH

Addresses are input on I/O[7:0]. Bits not part of the address space must be LOW.

The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Table 6 on page 19).

Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy

Data is input on I/O[7:0]. See Figure 55 on page 66 for additional data input details.

READs

After a READ command is issued, data is transferred from the memory array to the data register on the rising edge of WE#. R/B# goes LOW for ^{t}R and transitions HIGH after the transfer is complete. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 60 on page 68 for detailed timing information.

The READ STATUS (70h) command, TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command, or the R/B# signal can be used to determine when the device is ready.

If a controller is using a timing of 30ns or longer for ^{t}RC, use Figure 56 on page 66 for proper timing. If ^{t}RC is less than 30ns, use Figure 57 on page 67 for extended data output (EDO) timing.

Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 8 on page 17).

On the 8Gb MT29F8G08DAA, R/B# provides a status indication for the 4Gb section enabled by CE#, and R/B2# does the same for the 4Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 4Gb section.

On the 16Gb MT29F16G08FAA, R/B# provides a status indication for the 8Gb section enabled by CE#, and R/B2# does the same for the 8Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 8Gb section.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10 to 90 percent points on the R/B# waveform, rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance.

Refer to Figures 10 and 11 on page 18, which depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and VCC.

$$Rp(MIN,\ 3.3\text{V part}) = \frac{VCC(MAX) - VOL(MAX)}{IOL + \Sigma IL} = \frac{3.2V}{8mA + \Sigma IL}$$

Where ΣIL is the sum of the input currents of all devices tied to the R/B# pin.

Figure 8: READY/BUSY# Open Drain

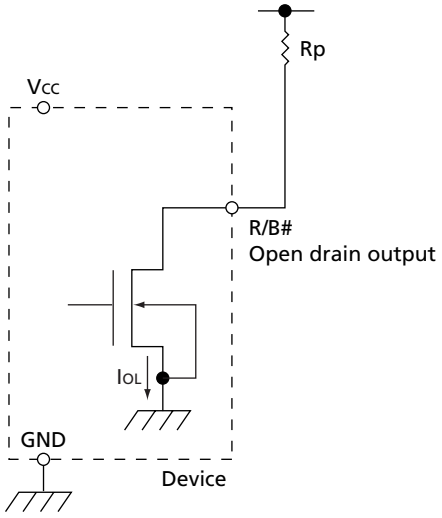
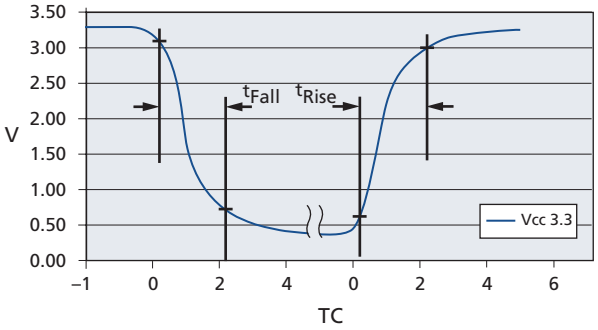


Figure 9: ^{t}Fall and ^{t}Rise



Notes:
1. ^{t}Fall and ^{t}Rise calculated at 10 percent and 90 percent points.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 10ns at 3.3V.
4. See TC values in Figure 11 on page 18 for approximate Rp value and TC.

Figure 10: IOL vs. Rp

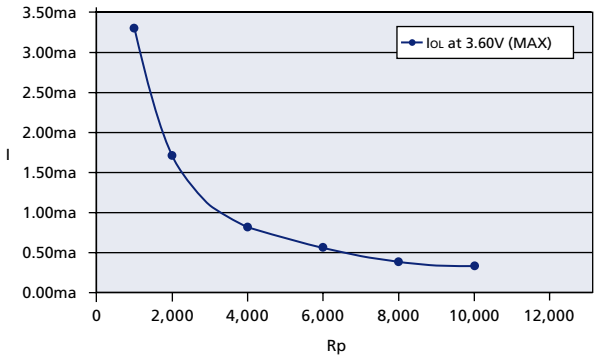


Figure 11: TC vs. Rp

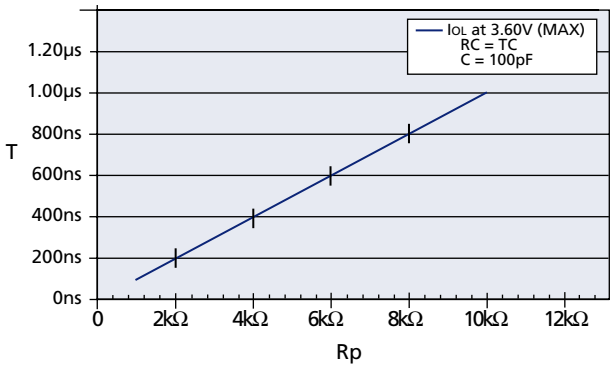


Table 5: Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L		H	X	Read mode	Command input
L	H	L		H	X		Address input
H	L	L		H	H	Write mode	Command input
L	H	L		H	H		Address input
L	L	L		H	H	Data input	
L	L	L	H		X	Sequential read and data output	
X	X	X	H	H	X	During read (busy)	
X	X	X	X	X	H	During program (busy)	
X	X	X	X	X	H	During erase (busy)	
X	X	X	X	X	L	Write protect	
X	X	H	X	X	0V/Vcc[1]	Standby	

Notes: 1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = VIH or VIL.

Command Definitions

Table 6: Command Set

Command	Command Cycle 1	Number of Address Cycles	Data Cycles Required[1]	Command Cycle 2	Valid During Busy	Notes
PAGE READ	00h	5	No	30h	No	
PAGE READ CACHE MODE	31h	–	No	–	No	2
PAGE READ CACHE MODE LAST	3Fh	–	No	–	No	2
READ for INTERNAL DATA MOVE	00h	5	No	35h	No	3
RANDOM DATA READ	05h	2	No	E0h	No	4
READ ID	90h	1	No	–	No	
READ STATUS	70h	–	No	–	Yes	
PROGRAM PAGE	80h	5	Yes	10h	No	5
PROGRAM PAGE CACHE MODE	80h	5	Yes	15h	No	5
PROGRAM for INTERNAL DATA MOVE	85h	5	Optional	10h	No	3
RANDOM DATA INPUT	85h	2	Yes	–	No	6
BLOCK ERASE	60h	3	No	D0h	No	5
RESET	FFh	–	No	–	Yes	
OTP DATA PROGRAM	A0h	5	Yes	10h	No	
OTP DATA PROTECT	A5h	5	No	10h	No	
OTP DATA READ	AFh	5	No	30h	No	

Notes:
1. Indicates required data cycles between command cycle 1 and command cycle 2.
2. Do not cross block address boundaries when using PAGE READ CACHE MODE operations.
3. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE. See Tables 3 and 4 on pages 13 and 14 for plane address boundary definitions.
4. The RANDOM DATA READ command is limited to use within a single page.
5. These commands are valid during busy when performing an interleaved die operation. See "Interleaved Die Operations" on page 47 for additional details.
6. The RANDOM DATA INPUT command is limited to use within a single page.

Table 7: Two-Plane Command Set

Command	Command Cycle 1	Number of Address Cycles	Command Cycle 2	Number of Address Cycles	Command Cycle 3	Valid During Busy	Notes
TWO-PLANE PAGE READ	00h	5	00h	5	30h	No	
TWO-PLANE READ for INTERNAL DATA MOVE	00h	5	00h	5	35h	No	1
TWO-PLANE RANDOM DATA READ	06h	5	E0h	–	–	No	2
TWO-PLANE/MULTIPLE-DIE READ STATUS	78h	3	–	–	–	Yes	3
TWO-PLANE PROGRAM PAGE	80h	5	11h-80h	5	10h	No	4
TWO-PLANE PROGRAM PAGE CACHE MODE	80h	5	11h-80h	5	15h	No	4
TWO-PLANE PROGRAM for INTERNAL DATA MOVE	85h	5	11h-80h	5	10h	No	1
TWO-PLANE BLOCK ERASE	60h	3	60h	3	D0h	No	4

Notes:
1. Do not cross plane address boundaries when using TWO-PLANE READ for INTERNAL DATA MOVE and TWO-PLANE PROGRAM for INTERNAL DATA MOVE. See Tables 3 and 4 on pages 13 and 14 for plane address boundary definitions.
2. The TWO-PLANE RANDOM DATA READ command is limited to use with the TWO-PLANE PAGE READ command.
3. The TWO-PLANE/MULTIPLE-DIE READ STATUS command can be used to check status with two-plane and multiple-die operations, excluding the TWO-PLANE PAGE READ (00h-00h-30h) command.
4. These commands are valid during busy when performing interleaved die operations. See "Interleaved Die Operations" on page 47 for additional details.

READ Operations

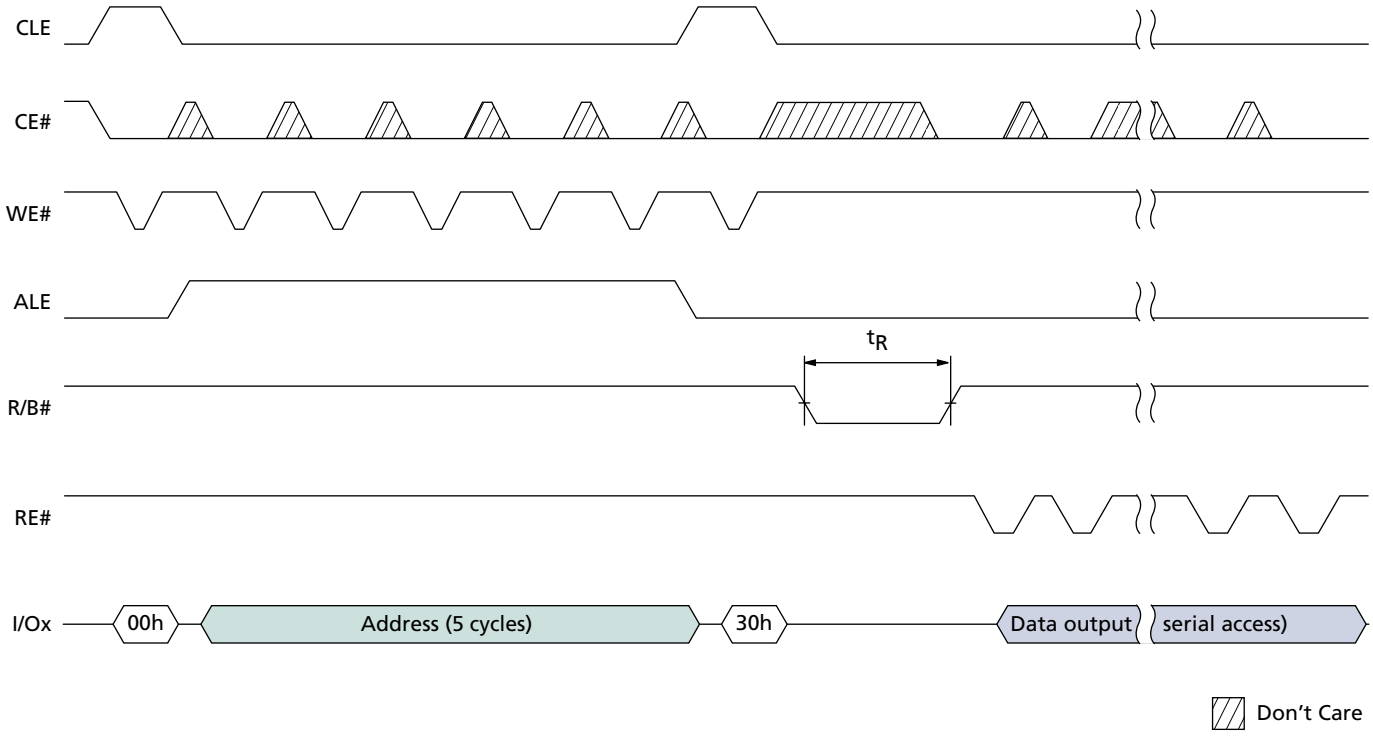
PAGE READ 00h-30h

At power-on, the device defaults to READ mode. To enter READ mode while in operation, write the 00h command to the command register, then write 5 ADDRESS cycles, and conclude with the 30h command.

To determine the progress of the data transfer from the NAND Flash array to the data register (^{t}R), monitor the R/B# signal or, alternatively, issue a READ STATUS (70h) command. If the READ STATUS command is used to monitor the data transfer, the user must reissue the READ (00h) command to receive data output from the data register. See Figure 65 on page 72 and Figure 66 on page 73 for examples. After the READ command has been reissued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address and going to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate (see Figure 12).

Figure 12: PAGE READ Operation



RANDOM DATA READ 05h-E0h

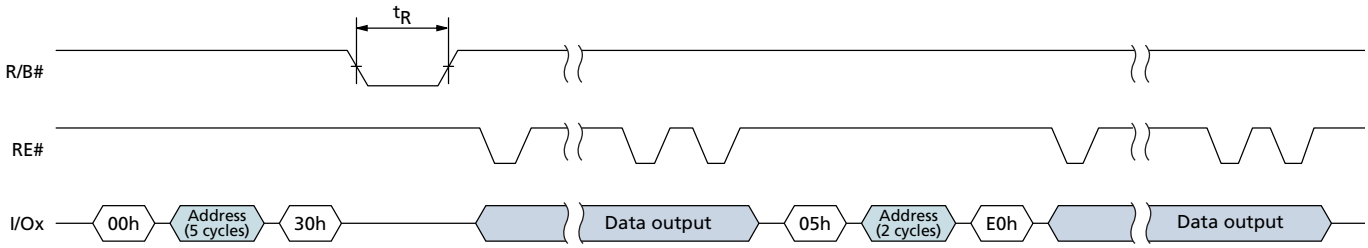
The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h) sequence.

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (2 cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially (see Figure 13).

Figure 13: RANDOM DATA READ Operation



PAGE READ CACHE MODE START 31h; PAGE READ CACHE MODE START LAST 3Fh

Micron NAND Flash devices have a cache register that can be used to increase the READ operation speed when accessing sequential pages within a block.

First, issue a normal PAGE READ (00h–30h) command sequence. See Figure 14 on page 23 for operation details. The R/B# signal goes LOW for ^{t}R during the time it takes to transfer the first page of data from the memory to the data register. After R/B# returns to HIGH, the PAGE READ CACHE MODE START (31h) command is latched into the command register. R/B# goes LOW for ^{t}DCBSYR1 while data is being transferred from the data register to the cache register. After the data register contents are transferred to the cache register, another PAGE READ is automatically started as part of the 31h command. Data is transferred from the next sequential page of the memory array to the data register during the same time data is being read serially (pulsing RE#) from the cache register. If the total time to output data exceeds ^{t}R, then the PAGE READ is hidden.

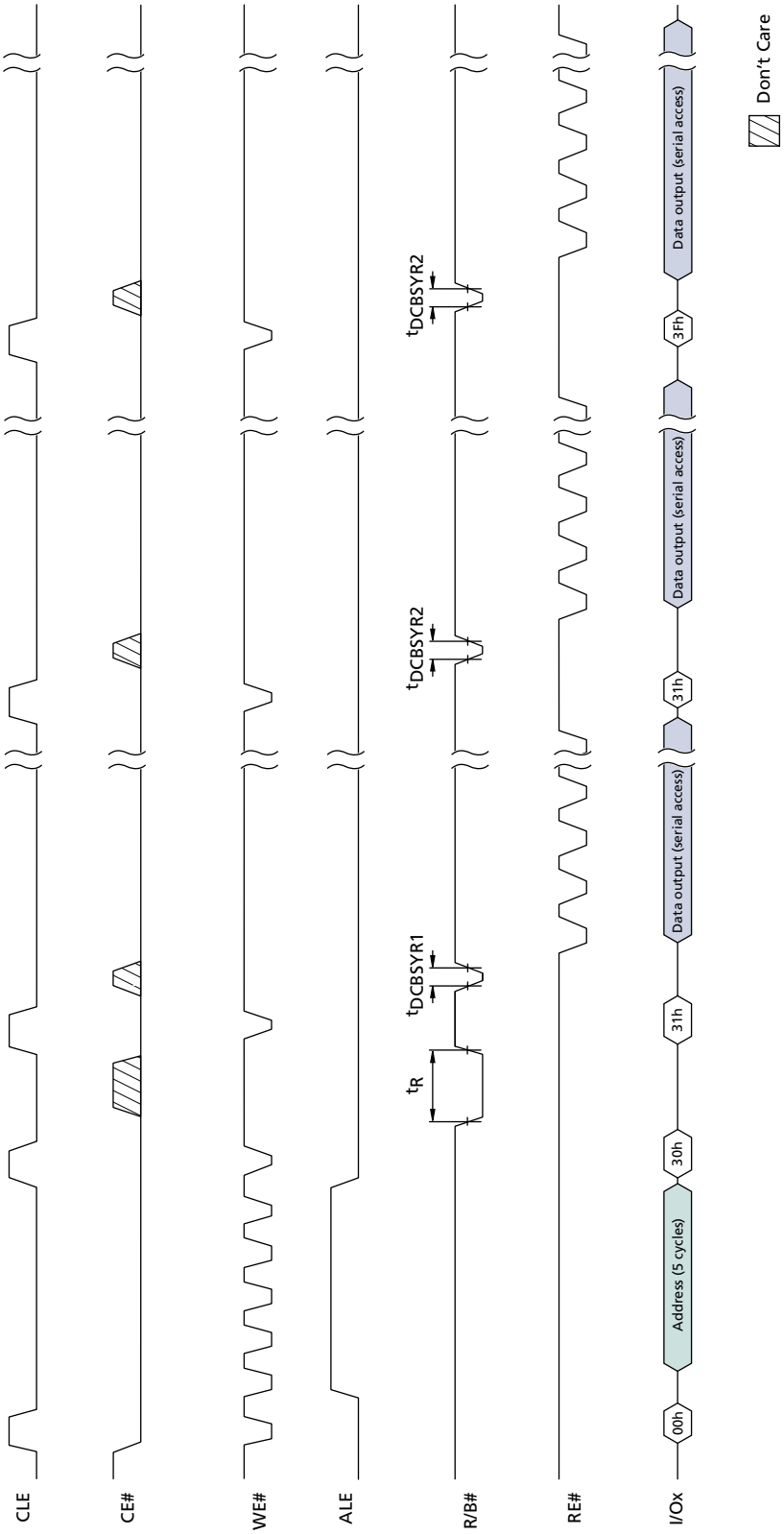
The second and subsequent pages of data are transferred to the cache register by issuing additional 31h commands. R/B# will stay LOW up to ^{t}DCBSYR2. This time can vary, depending on whether the previous memory-to-data-register transfer was completed prior to issuing the next 31h command. See Table 18 on page 63 for timing parameters. If the data transfer from memory to the data register is not completed before the 31h command is issued, R/B# stays LOW until the transfer is complete.

It is not necessary to output a whole page of data before issuing another 31h command. R/B# will stay LOW until the previous PAGE READ is complete and the data has been transferred to the cache register.

To read out the last page of data, the PAGE READ CACHE MODE START LAST (3Fh) command is issued. This command transfers data from the data register to the cache register without issuing another PAGE READ (see Figure 14 on page 23).

Crossing block address boundaries when using the PAGE READ CACHE MODE operation is prohibited.

Figure 14: PAGE READ CACHE MODE Operation

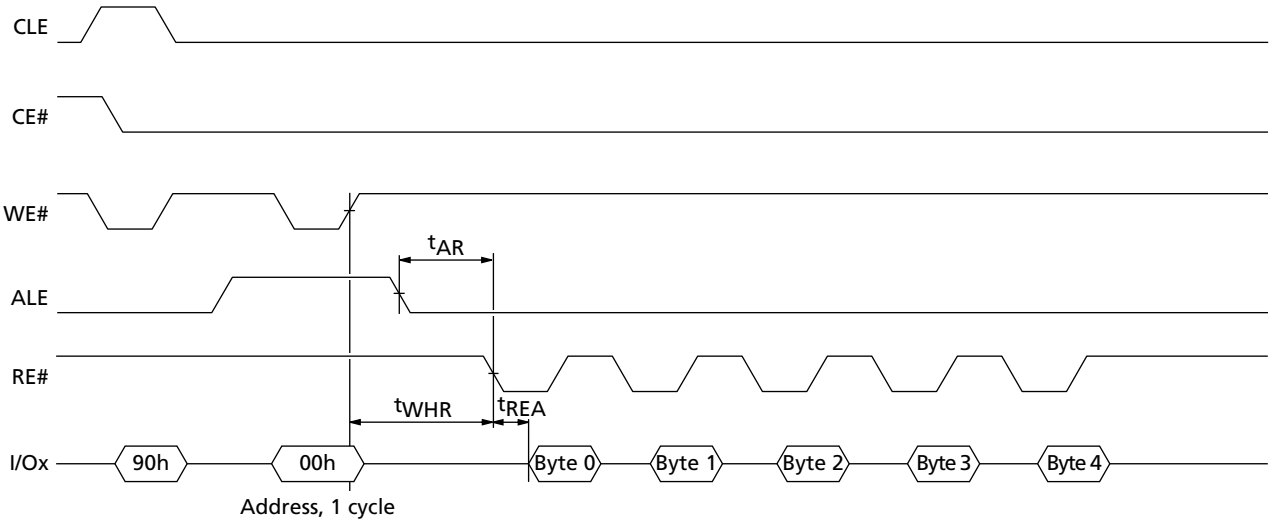


READ ID 90h

The READ ID command is used to read the 5 bytes of identifier code programmed into the NAND Flash devices. The READ ID command reads a 5-byte table that includes manufacturer ID, device configuration, and part-specific information (see Table 8 on page 25).

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until the next command cycle is issued (see Figure 15).

Figure 15: READ ID Operation



Notes: 1. See Table 8 on page 25 for byte definitions.

Table 8: Device ID and Configuration Codes

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	Manufacturer ID										
	Micron	0	0	1	0	1	1	0	0	2Ch	
Byte 1	Device ID										
MT29F4G08AAA	4Gb, x8, 3V	1	1	0	1	1	1	0	0	DCh	
MT29F8G08BAA	8Gb, x8, 3V	1	1	0	1	0	0	1	1	D3h	
MT29F8G08DAA	8Gb, x8, 3V	1	1	0	1	1	1	0	0	DCh	2
MT29F16G08FAA	16Gb, x8, 3V	1	1	0	1	0	0	1	1	D3h	3
Byte 2											
Number of die per CE	1							0	0	00b	
	2							0	1	01b	
Cell type	SLC					0	0			00b	
Number of simultaneously programmed pages	2			0	1					01b	
Interleaved operations between multiple die on the same CE#	Not supported		0							0b	
	Supported		1							1b	
Cache programming	Supported	1								1b	
Byte value	MT29F4G08AAA	1	0	0	1	0	0	0	0	90h	
	MT29F8G08BAA	1	1	0	1	0	0	0	1	D1h	3
	MT29F8G08DAA	1	0	0	1	0	0	0	0	90h	2
	MT29F16G08FAA	1	1	0	1	0	0	0	1	D1h	3
Byte 3											
Page size	2KB							0	1	01b	
Spare area size (bytes)	64B						1			1b	
Block size (w/o spare)	128KB			0	1					01b	
Organization	x8		0							0b	
Serial access (MIN)	25ns	1				0				1xxx0b	
Byte value	MT29FxG08xAA	1	0	0	1	0	1	0	1	95h	
Byte 4											
Reserved								0	0	00b	
Planes per CE#	2					0	1			01b	
	4					1	0			10b	
Plane size	2Gb		1	0	1					101b	
Reserved		0								0b	
Byte value	MT29F4G08AAA	0	1	0	1	0	1	0	0	54h	
	MT29F8G08BAA	0	1	0	1	1	0	0	0	58h	
	MT29F8G08DAA	0	1	0	1	0	1	0	0	54h	2
	MT29F16G08FAA	0	1	0	1	1	0	0	0	58h	3

Notes:
1. b = binary; h = hex.
2. The MT29F8G08DAA device ID code reflects the configuration of each 4Gb section.
3. The MT29F16G08FAA device ID code reflects the configuration of each 8Gb section.