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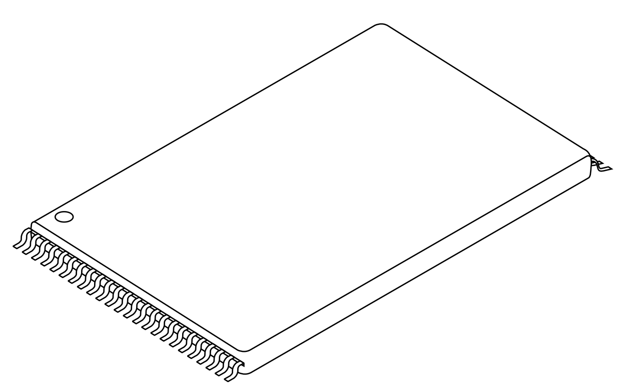
NAND Flash Memory

MT29F2G08AABWP/MT29F2G16AABWP
MT29F4G08BABWP/MT29F4G16BABWP
MT29F8G08FABWP

Features

- Organization:
  - Page size:
    x8: 2,112 bytes (2,048 + 64 bytes)
    x16: 1,056 words (1,024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size: 2Gb: 2,048 blocks; 4Gb: 4,096 blocks; 8Gb: 8,192 blocks
- Read performance:
  - Random read: 25µs
  - Sequential read: 30ns (3V x8 only)
- Write performance:
  - Page program: 300µs (TYP)
  - Block erase: 2ms (TYP)
- Endurance: 100,000 PROGRAM/ERASE cycles
- Data retention: 10 years
- First block (block address 00h) guaranteed to be valid without ECC (up to 1,000 PROGRAM/ERASE cycles)
- VCC: 2.7V–3.6V
- Automated PROGRAM and ERASE
- Basic NAND command set:
  - PAGE READ, RANDOM DATA READ, READ ID, READ STATUS, PROGRAM PAGE, RANDOM DATA INPUT, PROGRAM PAGE CACHE MODE, INTERNAL DATA MOVE, INTERNAL DATA MOVE with RANDOM DATA INPUT, BLOCK ERASE, RESET
- New commands:
  - PAGE READ CACHE MODE
  - READ UNIQUE ID (contact factory)
  - READ ID2 (contact factory)
- Operation status byte provides a software method of detecting:
  - PROGRAM/ERASE operation completion
  - PROGRAM/ERASE pass/fail condition
  - Write-protect status
- Ready/busy# (R/B#) pin provides a hardware method of detecting PROGRAM or ERASE cycle completion
- PRE pin: prefetch on power up
- WP# pin: hardware write protect

Figure 1: 48-Pin TSOP Type 1



Options				Marking
• Density:				
2Gb (single die)				MT29F2GxxAAB
4Gb (dual-die stack)				MT29F4GxxBAB
8Gb (quad-die stack)				MT29F8GxxFAB
• Device width:				
x8				MT29Fxx08x
x16				MT29Fxx16x
• Configuration:	# of die	# of CE#	# of R/B#	
	1	1	1	A
	2	1	1	B
	4	2	2	F
• VCC: 2.7V–3.6V				A
• Second generation die				B
• Package:				
48 TSOP type I (lead-free)				WP
48 TSOP type I (NEW version, 8Gb device only, lead-free)				WA
48 TSOP type I (contact factory)				WG
• Operating temperature:				
Commercial (0°C to 70°C)				None
Extended temperature (-40°C to +85°C)				ET

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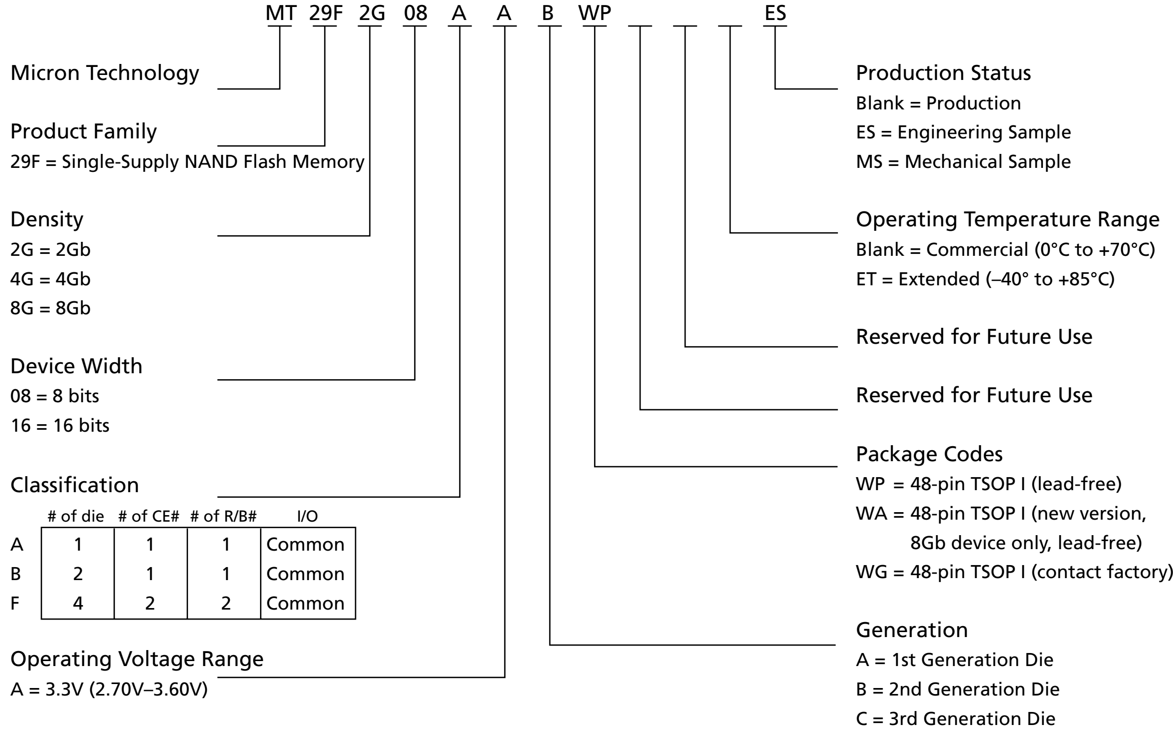
Part Numbering Information

Micron® NAND Flash devices are available in several different configurations and densities. (See Figure 2.)

Figure 2: Part Number Chart



Valid Part Number Combinations

After building the part number from the part numbering chart above, verify that the part number is valid using the Micron Parametric Part Search Web site at http://www.micron.com/partsearch to verify that the part number is offered and valid. If the device required is not on this list, contact the factory.

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Table of Contents

Features 1
Part Numbering Information 2
Valid Part Number Combinations 2
General Description 7
Architecture 10
Addressing 10
Bus Operation 16
Control Signals 16
Commands 16
Address Input 16
Data Input 17
READs 17
Ready/Busy# 17
Minimum Rp 18
Power-On AUTO-READ 21
Command Definitions 22
READ Operations 23
PAGE READ 00h-30h 23
RANDOM DATA READ 05h-E0h 24
PAGE READ CACHE MODE START 31h; PAGE READ CACHE MODE START LAST 3Fh 24
READ ID 90h 26
READ STATUS 70h 27
PROGRAM Operations 29
PROGRAM PAGE 80h-10h 29
SERIAL DATA INPUT 80h 29
RANDOM DATA INPUT 85h 29
PROGRAM PAGE CACHE MODE 80h-15h 30
Internal Data Move 31
READ FOR INTERNAL DATA MOVE 00h-35h 31
INTERNAL DATA MOVE 85h-10h 31
BLOCK ERASE Operation 33
BLOCK ERASE 60h-D0h 33
RESET Operation 34
RESET FFh 34
WRITE PROTECT Operation 35
Error Management 37
Electrical Characteristics 38
VCC Power Cycling 38
Timing Diagrams 42
Package Dimensions 56

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List of Figures

Figure 1: 48-Pin TSOP Type 1 1
Figure 2: Part Number Chart 2
Figure 3: NAND Flash Functional Block Diagram 8
Figure 4: Pin Assignment (Top View) 48-Pin TSOP Type 1 8
Figure 5: Memory Map x8 11
Figure 6: Memory Map x16 11
Figure 7: Array Organization for MT29F2G08AxB (x8) 12
Figure 8: Array Organization for MT29F2G16AxB (x16) 13
Figure 9: Array Organization for MT29F4G08BxB and MT29F8G08FxB (x8) 14
Figure 10: Array Organization for MT29F4G16BxB (x16) 15
Figure 11: Time Constants 17
Figure 12: READY/BUSY# Open Drain 18
Figure 13: tR and tF 18
Figure 14: Iol vs. Rp 19
Figure 15: TC vs. Rp 19
Figure 16: First Page Power-On AUTO-READ (3V VCC only) 21
Figure 17: AC Waveforms During Power Transitions 21
Figure 18: PAGE READ Operation 23
Figure 19: RANDOM DATA READ Operation 24
Figure 20: PAGE READ CACHE MODE 25
Figure 21: READ ID Operation 26
Figure 22: Status Register Operation 28
Figure 23: PROGRAM and READ STATUS Operation 29
Figure 24: RANDOM DATA INPUT 29
Figure 25: PROGRAM PAGE CACHE MODE Example 30
Figure 26: INTERNAL DATA MOVE 32
Figure 27: INTERNAL DATA MOVE with RANDOM DATA INPUT 32
Figure 28: BLOCK ERASE Operation 33
Figure 29: RESET Operation 34
Figure 30: ERASE Enable 35
Figure 31: ERASE Disable 35
Figure 32: PROGRAM Enable 35
Figure 33: PROGRAM Disable 36
Figure 34: COMMAND LATCH Cycle 42
Figure 35: ADDRESS LATCH Cycle 42
Figure 36: INPUT DATA LATCH 43
Figure 37: SERIAL ACCESS Cycle After READ 43
Figure 38: STATUS READ Cycle 44
Figure 39: PAGE READ 44
Figure 40: READ Operation with CE# “Don’t Care” 45
Figure 41: RANDOM DATA READ 45
Figure 42: PAGE READ CACHE MODE Timing Diagram, Part 1 of 2 46
Figure 43: PAGE READ CACHE MODE Timing Diagram, Part 2 of 2 47
Figure 44: PAGE READ CACHE MODE Timing without R/B#, Part 1 of 2 48
Figure 45: PAGE READ CACHE MODE Timing without R/B#, Part 2 of 2 49
Figure 46: READ ID Operation 50
Figure 47: Program Operation with CE# “Don’t Care” 50
Figure 48: PROGRAM PAGE Operation 51
Figure 49: PROGRAM PAGE Operation with RANDOM DATA INPUT 52
Figure 50: INTERNAL DATA MOVE 52
Figure 51: PROGRAM PAGE CACHE MODE 53

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Figure 52: PROGRAM PAGE CACHE MODE Ending on 15h 54
Figure 53: BLOCK ERASE Operation 55
Figure 54: RESET Operation 55
Figure 55: 48-Pin TSOP Type I 56

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List of Tables

Table 1: Pin Descriptions 9
Table 2: Array Addressing: MT29F2G08AxB 12
Table 3: Array Addressing: MT29F2G16AxB 13
Table 4: Array Addressing: MT29F4G08BxB and MT29F8G08FxB. 14
Table 5: Array Addressing: MT29F4G16BxB 15
Table 6: Mode Selection 20
Table 7: Command Set 22
Table 8: Device ID and Configuration Codes 27
Table 9: Status Register Bit Definition 28
Table 10: Status Register Contents After RESET Operation 34
Table 11: Absolute Maximum Ratings by Device 38
Table 12: Recommended Operating Conditions 38
Table 13: DC and Operating Characteristics 39
Table 14: Valid Blocks 39
Table 15: Capacitance 39
Table 16: Test Conditions 40
Table 17: AC Characteristics: Command, Data, and Address Input 40
Table 18: AC Characteristics: Normal Operation. 41
Table 19: PROGRAM/ERASE Characteristics 41

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General Description

NAND technology provides a cost-effective solution for applications requiring high-density solid-state storage. The MT29F2G08AxB and MT29F2G16AxB are 2Gb NAND Flash memory devices. The MT29F4G08BxB and MT29F4G16BxB are two-die stacks that operate as a single 4Gb device. The MT29F8G08FAB is a four-die stack that operates as two independent 4Gb devices (MT29F4G08BxB), providing a total storage capacity of 8Gb in a single, space-saving package. Micron NAND Flash devices include standard NAND features as well as new features designed to enhance system-level performance.

Micron NAND Flash devices use a highly multiplexed 8- or 16-bit bus (I/O[7:0] or I/O[15:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND command bus interface protocol. Three additional pins control hardware write protection (WP#), monitor device status (R/B#), and initiate the auto-read feature (PRE—3V device only). Note that the PRE function is not supported on extended-temperature devices.

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

MT29F2G and MT29F4G devices contain 2,048 and 4,096 erasable blocks respectively. Each block is subdivided into 64 programmable pages. Each page consists of 2,112 bytes (x8) or 1,056 words (x16). The pages are further divided into a 2,048-byte data storage region with a separate 64-byte area on the x8 device; and on the x16 device, separate 1,024-word and 32-word areas. The 64-byte and 32-word areas are typically used for error management functions.

The contents of each 2,112-byte page can be programmed in 300µs, and an entire 132K-byte/66K word block can be erased in 2ms. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. ERASE/PROGRAM endurance is specified at 100,000 cycles when using appropriate error correcting code (ECC) and error management.

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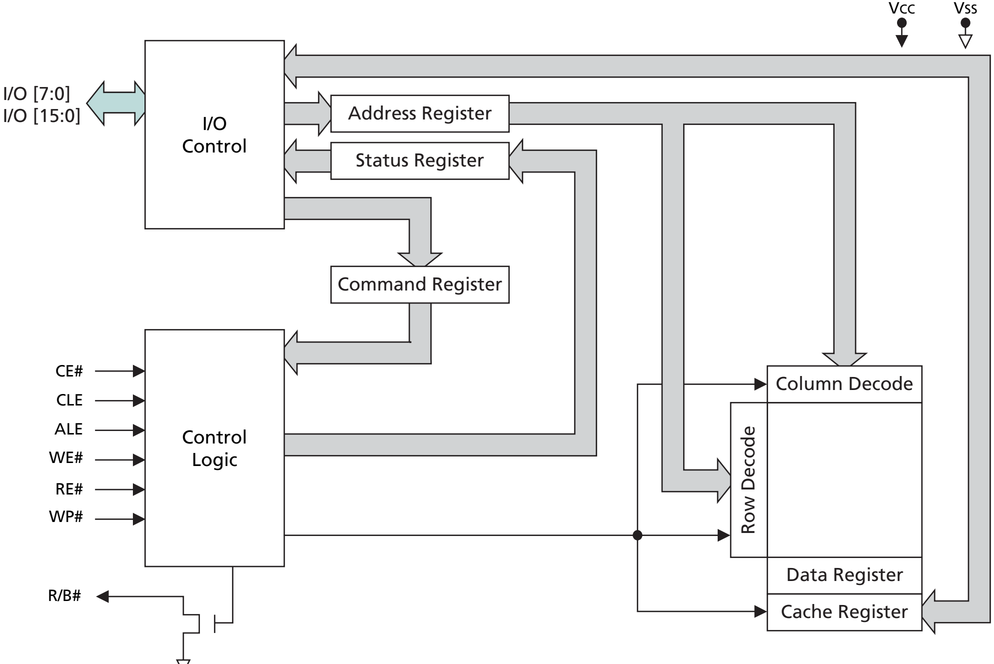
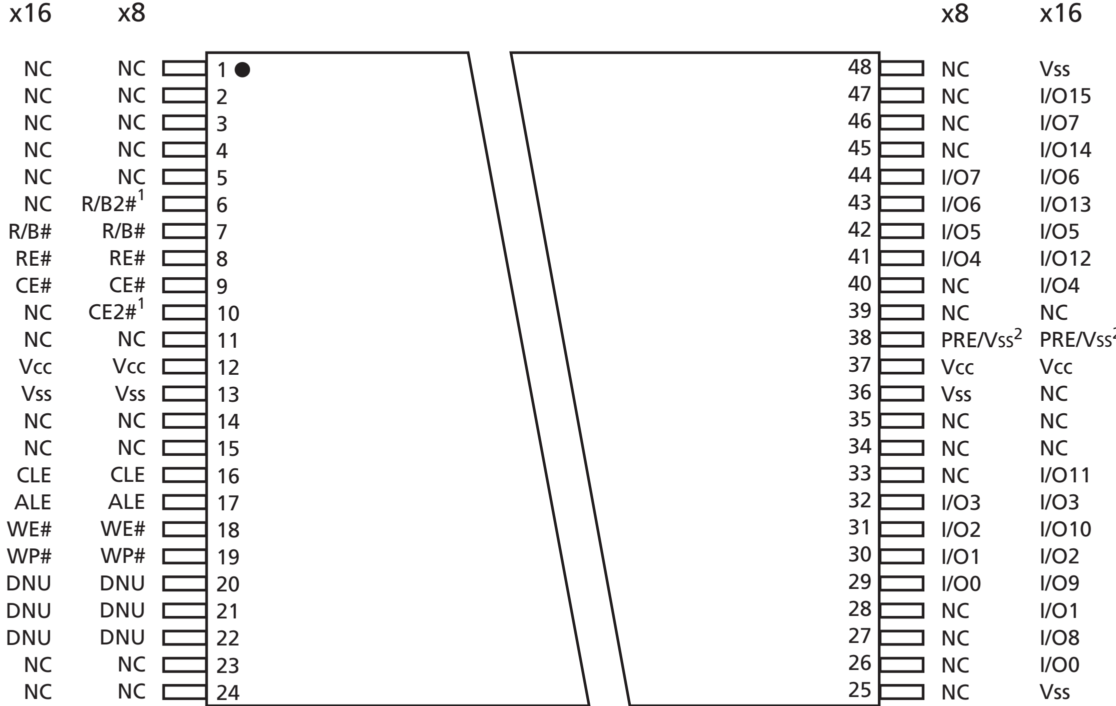
Figure 3: NAND Flash Functional Block Diagram



Note: The PRE function is not supported on extended-temperature devices.

Figure 4: Pin Assignment (Top View) 48-Pin TSOP Type 1



Notes: 1. CE2# and R/B2# on 8Gb device only. These pins are NC for other configurations.
2. The PRE function is not supported on extended-temperature devices.

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Table 1: Pin Descriptions

Symbol	Type	Description
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register upon a LOW-to-HIGH transition on WE#. When address information is not being loaded, the ALE pin should be driven LOW.
CE#, CE2#	Input	Chip enable: Gates transfers between the host system and the NAND device. Once the device starts a PROGRAM or ERASE operation, the chip enable pin can be de-asserted. For the 8Gb configuration, CE# controls the first 4Gb of memory; CE2# controls the second 4Gb. See the Bus Operation section, starting on "Bus Operation" on page 16 for additional operational details.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, the CLE pin should be driven LOW.
PRE[1] (3V device only)	Input	Power-on read enable: Enables the auto-read function when at Vcc. See "Bus Operation" on page 16, for additional details.
RE#	Input	Read enable: Gates transfers from the NAND device to the host system.
WE#	Input	Write enable: Gates transfers from the host system to the NAND device.
WP#	Input	Write protect: Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when the WP# pin is LOW.
I/O[7:0] MT29FxG08 I/O[15:0] MT29FxG16	I/O	Data inputs/outputs: The bidirectional I/O pins transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/O pins are inputs.
R/B#, R/B2#	Output	Ready/busy: An *open-drain,* active-LOW output, that uses an external pull-up resistor. The pin is used to indicate when the chip is processing a PROGRAM or ERASE operation. The pin is also used during a READ operation to indicate when data is being transferred from the array into the serial data register. Once these operations have completed, the R/B# returns to the High-Z state. In the 8Gb configuration, R/B# is for the 4Gb of memory enabled by CE#; R/B2# is for the 4Gb of memory enabled by CE2#.
Vcc	Supply	Vcc: The Vcc pin is the power supply pin.
Vss	Supply	Vss: The Vss pin is the ground connection.
DNU	–	Do not use: Must be left floating.
NC	–	No connect: NC pins are not internally connected. These pins can be driven or left unconnected.

Notes: 1. The PRE function is not supported on extended-temperature devices.

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Architecture

These devices use NAND electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins. This provides a memory device with a low pin count.

The internal memory array is accessed on a page basis. When doing reads, a page of data is copied from the memory array into the data register. Once copied to the data register, data is output sequentially, byte-by-byte on x8 devices, or word-by-word on x16 devices.

The memory array is programmed on a page basis. After the starting address is loaded into the internal address register, data is sequentially written to the internal data register up to the end of a page. After all of the page data has been loaded into the data register, array programming is started.

In order to increase programming bandwidth, this device incorporates a cache register. In the cache programming mode, data is first copied into the cache register and then into the data register. Once the data is copied into the data register, programming begins.

After the data register has been loaded and programming started, the cache register becomes available for loading additional data. Loading the next page of data into the cache register takes place while page programming is in process.

The INTERNAL DATA MOVE command also uses the internal cache register. Normally, moving data from one area of external memory to another uses a large number of external memory cycles. By using the internal cache register and data register, array data can be copied from one page and then programmed into another without using external memory cycles.

Addressing

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a five-cycle sequence as shown in Figures 7 and 8, on pages 12 and 13 respectively. Table 2 on page 12 presents address functions internal to the x8 device; Table 3 on page 13 covers the same functions for the x16 device. See Figures 5 and 6 on page 11 for additional memory mapping and addressing details.

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Figure 5: Memory Map x8

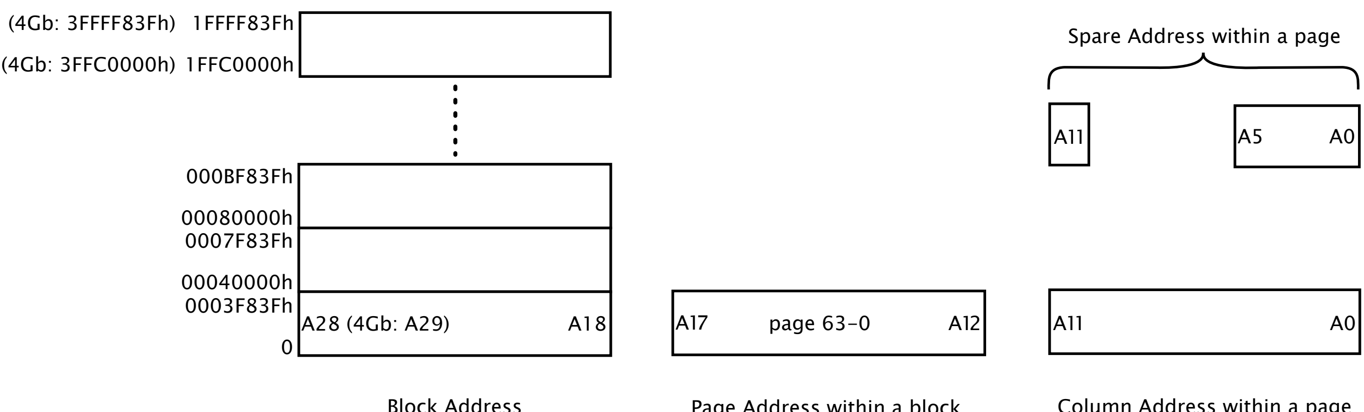
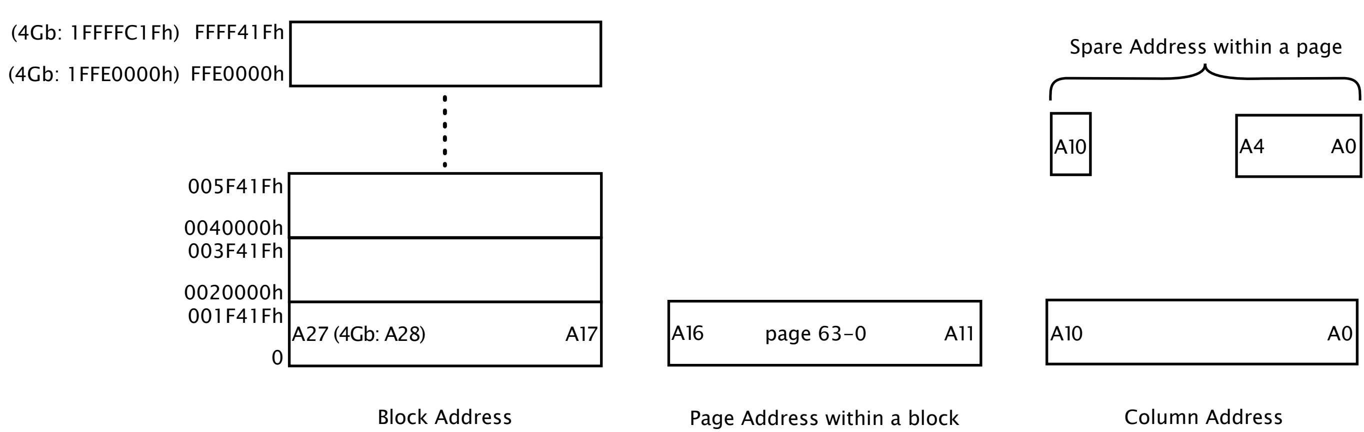


Figure 6: Memory Map x16



Note: Block address and page address = actual page address.

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Figure 7: Array Organization for MT29F2G08AxB (x8)

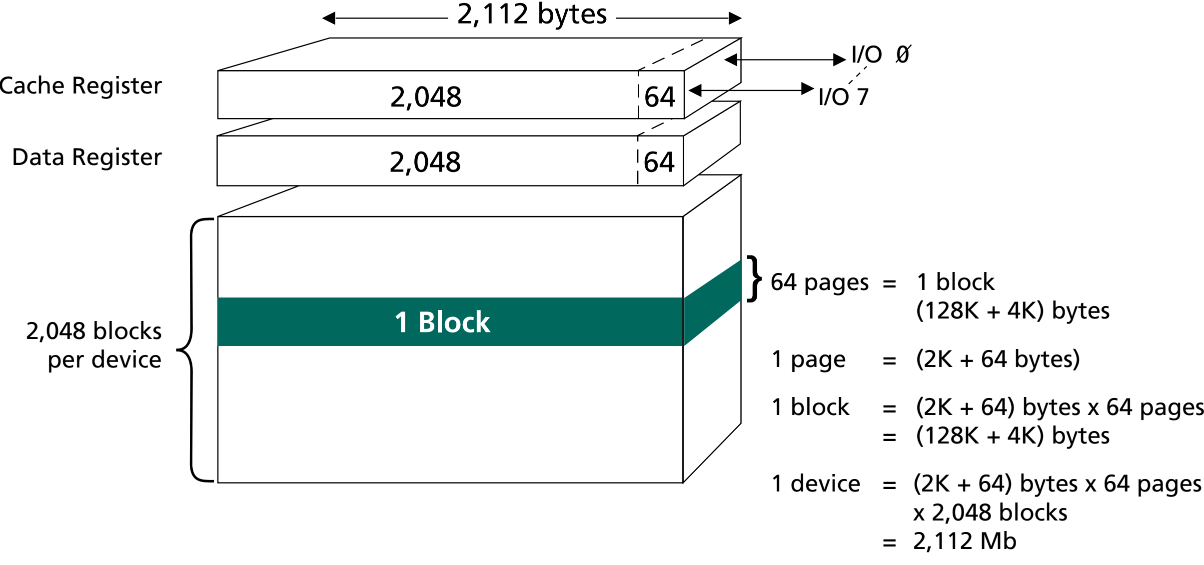

Table 2: Array Addressing: MT29F2G08AxB

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	RA19	RA18	RA17	RA16	RA15	RA14	RA13	RA12
Fourth	RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	RA28

Note: CAx = column address; RAx = row address.

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Figure 8: Array Organization for MT29F2G16AxB (x16)

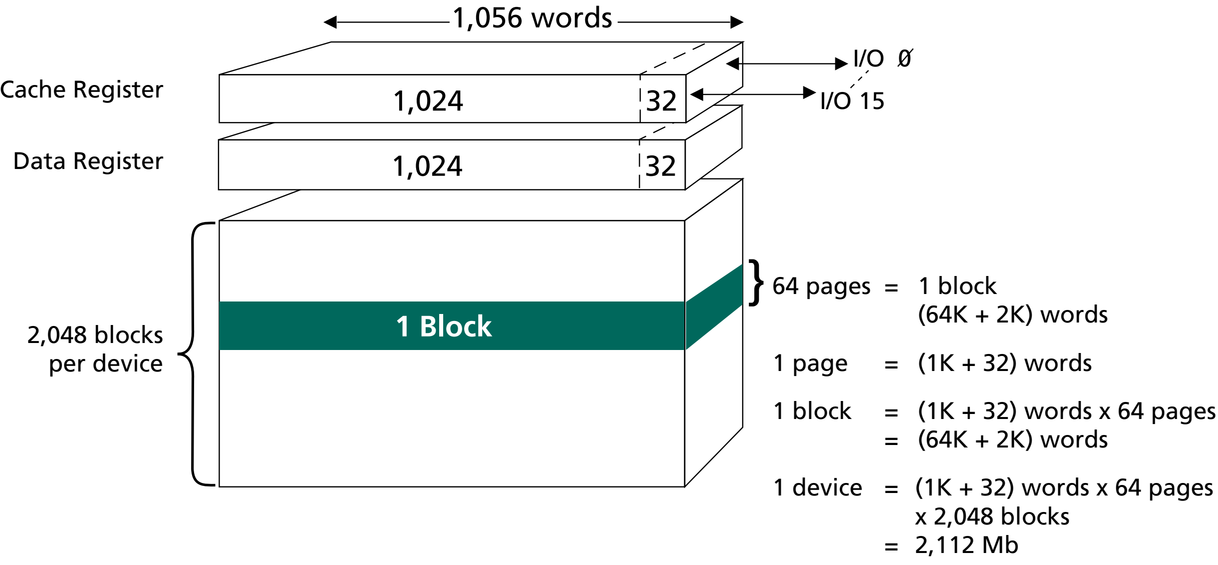

Table 3: Array Addressing: MT29F2G16AxB

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10	CA9	CA8
Third	LOW	RA18	RA17	RA16	RA15	RA14	RA13	RA12	RA11
Fourth	LOW	RA26	RA25	RA24	RA23	RA22	RA21	RA20	RA19
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	RA27

Notes: 1. CAx = column address; RAx = row address.
2. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

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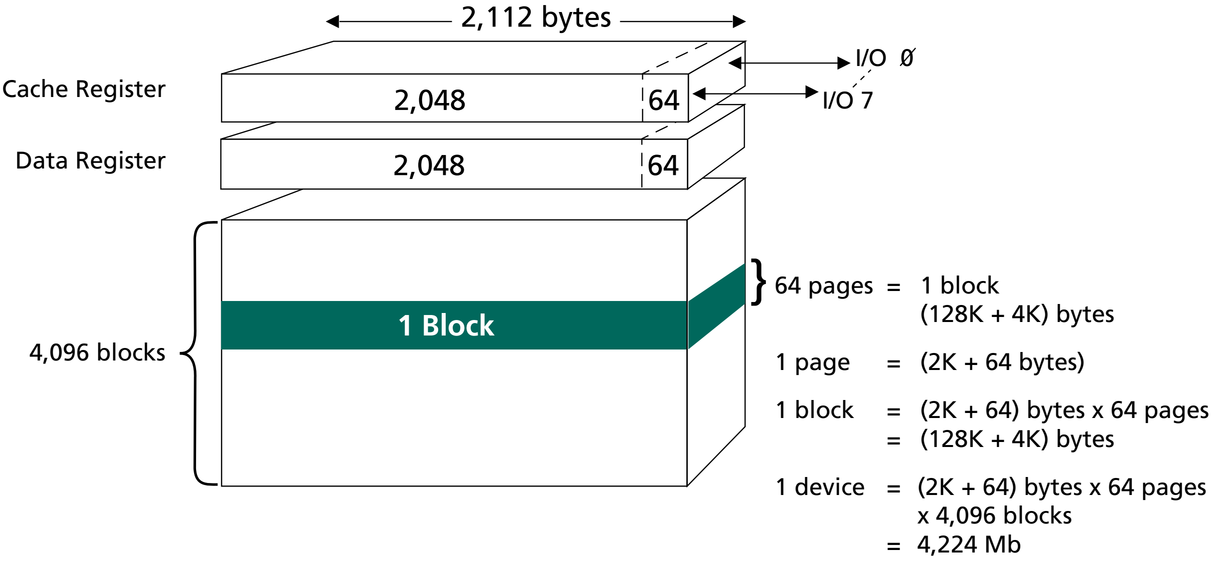
Figure 9: Array Organization for MT29F4G08BxB and MT29F8G08FxB (x8)



Note: For the 8Gb MT29F8G08F, the 4Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 4: Array Addressing: MT29F4G08BxB and MT29F8G08FxB

CAx = column address; RAx = row address.

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	RA19	RA18	RA17	RA16	RA15	RA14	RA13	RA12
Fourth	RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	RA29[1]	RA28

Notes: 1. Die address boundary: 0 = 0 – 2Gb, 1 = 2Gb – 4Gb.

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Figure 10: Array Organization for MT29F4G16BxB (x16)

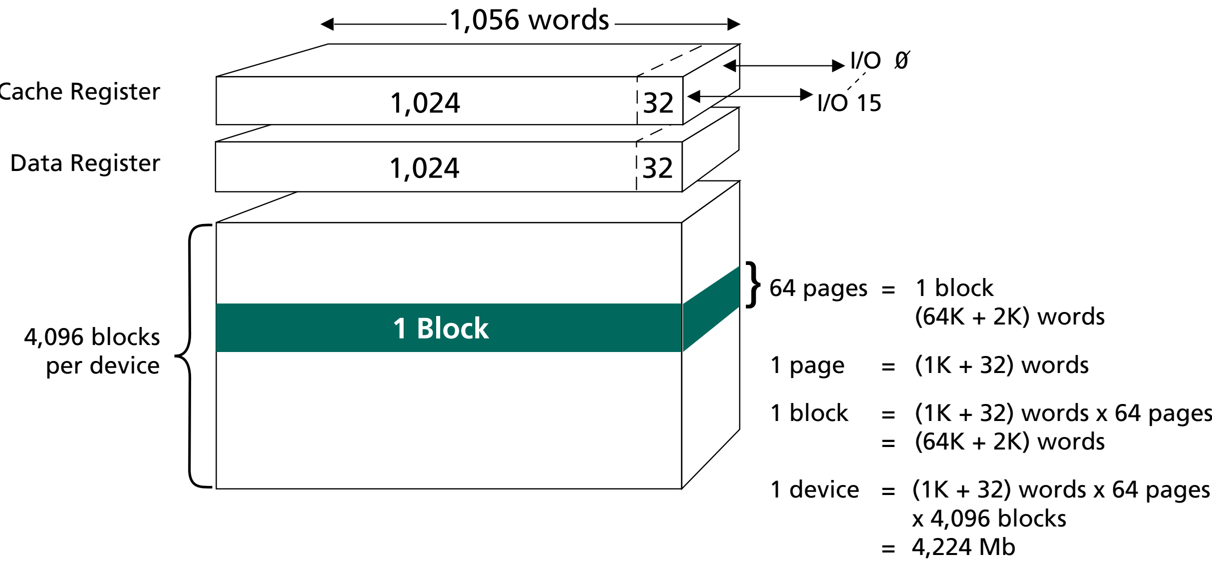

Table 5: Array Addressing: MT29F4G16BxB
CAx = column address; RAx = row address.

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10	CA9	CA8
Third	LOW	RA18	RA17	RA16	RA15	RA14	RA13	RA12	RA11
Fourth	LOW	RA26	RA25	RA24	RA23	RA22	RA21	RA20	RA19
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	RA28[1]	RA27

Notes: 1. Die address boundary: 0 = 0 – 2Gb, 1 = 2Gb – 4Gb.
2. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

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Bus Operation

The bus on the MT29Fxxx devices is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O pins I/O[15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O[7:0].

The command sequence normally consists of a command latch cycle, an ADDRESS LATCH cycle, and a DATA cycle—either READ or WRITE.

Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control Flash device READ and WRITE operations. On the 8Gb MT29F8G08FAB, CE# and CE2# each control independent 4Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the Flash memory will accept command, data, and address information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 40 on page 45 and Figure 47 on page 50 for examples of CE# “Don’t Care” operations.

The CE# “Don’t Care” operation allows the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus. One device can be programmed while another is being read.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an address input cycle is occurring.

Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- The device is not busy

The exceptions to this are the READ STATUS and RESET commands. Commands are transferred to the command register on the rising edge of WE#. See Figure 34 on page 42.

Commands are input on I/O[7:0] only. For devices with a x16 interface, I/O[15:8] must be written with zeros when issuing a command.

Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are LOW, and
- ALE is HIGH, and
- The device is not busy

Addresses are input on I/O[7:0] only. For devices with a x16 interface, I/O[15:8] must be written with zeros when issuing an address.

Generally all five ADDRESS cycles are written to the device. An exception to this is the BLOCK ERASE command, which requires only three ADDRESS cycles. See “BLOCK ERASE Operation” on page 33 for details.

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RANDOM DATA INPUT and OUTPUT commands need only column addresses, so only two ADDRESS cycles are required. Refer to the command descriptions to determine the addressing requirements for each command.

Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- The device is not busy

Data is input on I/O[7:0] for x8 devices, and I/O[15:0] on x16 devices. See Figure 36 on page 43 for additional data input details.

READs

After a READ command is sent to the memory device, data is transferred from the memory array to the data register in ^tR. Typically ^tR is 25µs. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 39 on page 44 for detailed timing information.

The READ STATUS (70h) command or the R/B# signal can be used to determine when the device is ready. See the STATUS READ command section on page 27 for details.

Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of a PROGRAM/ERASE/READ operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The signal requires a pull-up resistor for proper operation. The READ STATUS command can be used in place of R/B#. Typically R/B# would be connected to an interrupt pin on the system controller. See Figure 12 on page 18.

On the 8Gb MT29F8G08FAB, R/B# provides an indication for the 4Gb section enabled by CE#, and R/B2# does the same for the 4Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 4Gb section.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp (Rp = resistance of pull-up resistor) depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10- to 90-percent points on the R/B# waveform, rise time is approximately two time constants (TC).

Figure 11: Time Constants

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance.

Refer to Figure 13 on page 18, and Figure 14 on page 19, which depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

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Minimum Rp

$$Rp\ (MIN,\ 3.3V\ part) = \frac{V_{CC}\ (MAX) - V_{OL}\ (MAX)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where ΣIL is the sum of the input currents of all devices tied to the R/B# pin.

Figure 12: READY/BUSY# Open Drain

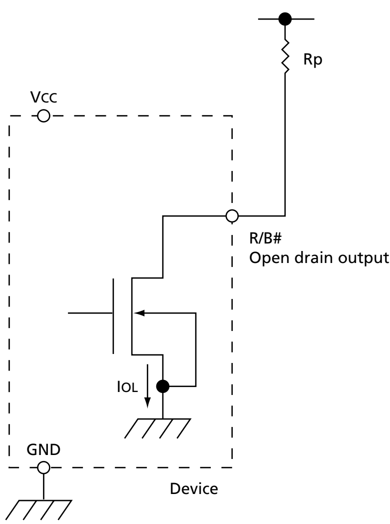
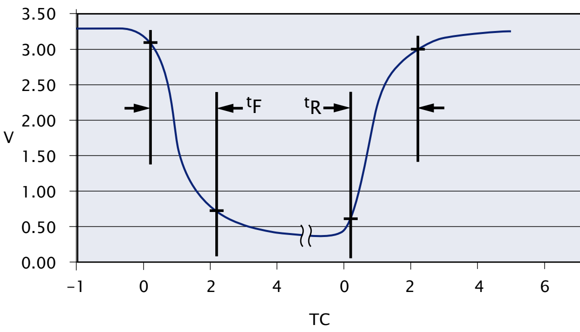


Figure 13: ^tR and ^tF



Notes:
1. ^tR and ^tF calculated at 10 percent and 90 percent points.
2. ^tR dependent on external capacitance and resistive loading and output transistor impedance.
3. ^tR primarily dependent on external pull-up resistor and external capacitive loading.
4. $^tF \approx$ 10ns at 3.3V.
5. See TC values in Figure 15 on page 19 for approximate Rp value and TC.

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Figure 14: IOL vs. Rp

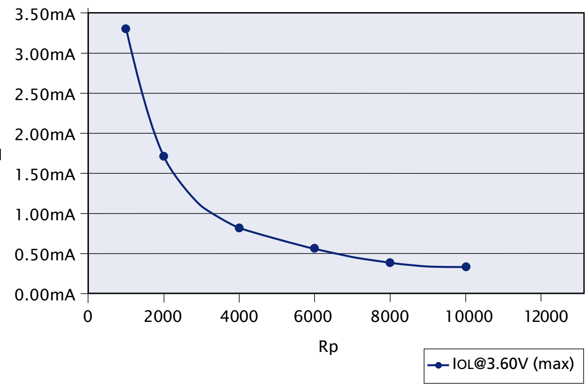

Figure 15: TC vs. Rp

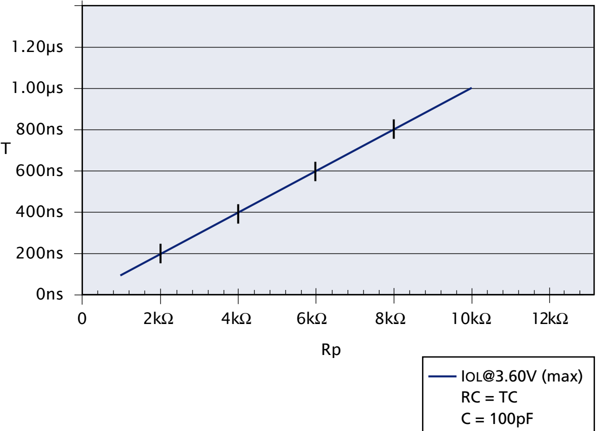

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Table 6: Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#[1]	PRE[2]	Mode	
H	L	L	↑	H	X	X	Read mode	Command input
L	H	L	↑	H	X	X		Address input
H	L	L	↑	H	H	X	Write mode	Command input
L	H	L	↑	H	H	X		Address input
L	L	L	↑	H	H	X	Data input	
L	L	L	H	↓	X	X	Sequential read and data output	
L	L	L	H	H	X	X	During read (busy)	
X	X	X	X	X	H	X	During program (busy)	
X	X	X	X	X	H	X	During erase (busy)	
X	X	X	X	X	L	X	Write protect	
X	X	H	X	X	0V/V_{CC}	0V/V_{CC}	Standby	

Notes: 1. WP# should be biased to CMOS HIGH or LOW for standby.
2. PRE should be tied to V_{CC} or ground. Do not transition PRE during device operations. The PRE function is not supported on extended-temperature devices.
3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

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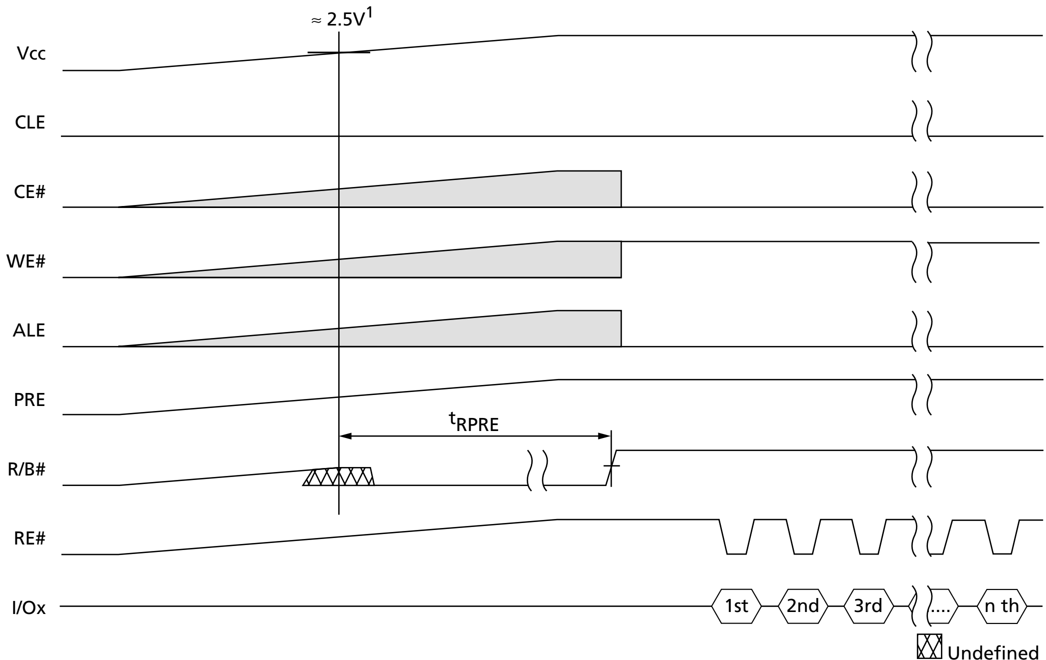
Power-On AUTO-READ

During power-on, with the PRE pin at VCC, 3V VCC devices automatically transfer the first page of the memory array to the data register without requiring a command or address-input sequence. As VCC reaches approximately 2.5V, the internal voltage detector initiates the power-on AUTO-READ function.

R/B# will stay LOW (^{t}RPRE) while the first page of data is copied into the data register. See Table 18 on page 41 for the ^{t}RPRE value. Once the READ is complete and R/B# goes HIGH, RE# can be pulsed to output the first page of data.

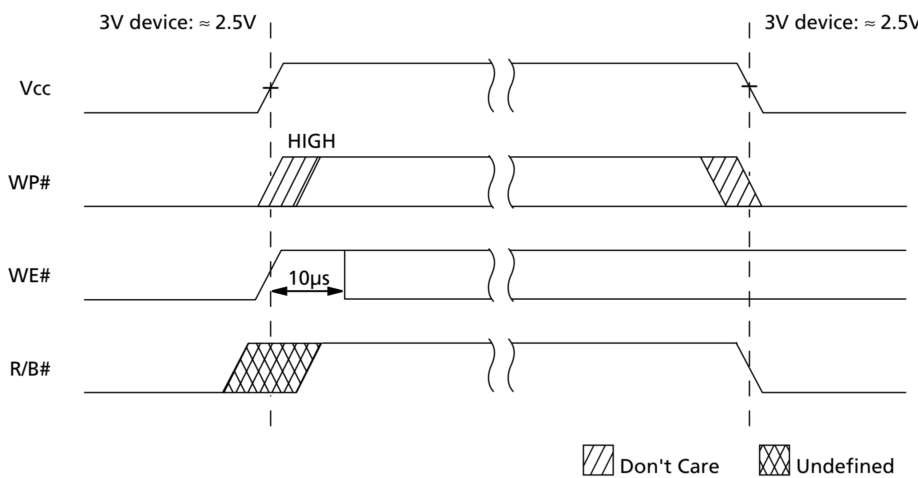
The PRE function is not supported on extended-temperature devices.

Figure 16: First Page Power-On AUTO-READ (3V Vcc only)



Notes: 1. Verified per device characterization; not 100 percent tested on all devices.
2. The PRE function is not supported on extended-temperature devices.

Figure 17: AC Waveforms During Power Transitions



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Command Definitions

Table 7: Command Set

Operation	Cycle 1	Cycle 2	Valid During Busy
PAGE READ	00h	30h	No
PAGE READ CACHE MODE START[1]	31h	–	No
PAGE READ CACHE MODE START LAST[1]	3Fh	–	No
READ for INTERNAL DATA MOVE[2]	00h	35h	No
RANDOM DATA READ[3]	05h	E0h	No
READ ID	90h	–	No
READ STATUS	70h	–	Yes
PROGRAM PAGE	80h	10h	No
PROGRAM PAGE CACHE[1]	80h	15h	No
PROGRAM for INTERNAL DATA MOVE[2]	85h	10h	No
RANDOM DATA INPUT for PROGRAM [4]	85h	–	No
BLOCK ERASE	60h	D0h	No
RESET	FFh	–	Yes

Notes:
1. Do not cross die address boundaries when using cache operations. See Tables 4 and 5 for definition of die address boundaries.
2. Do not cross die address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM FOR INTERNAL DATA MOVE. See Tables 4 and 5 for definition of die address boundaries.
3. RANDOM DATA READ command limited to use within a single page.
4. RANDOM DATA INPUT for PROGRAM command limited to use within a single page.

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READ Operations

PAGE READ 00h-30h

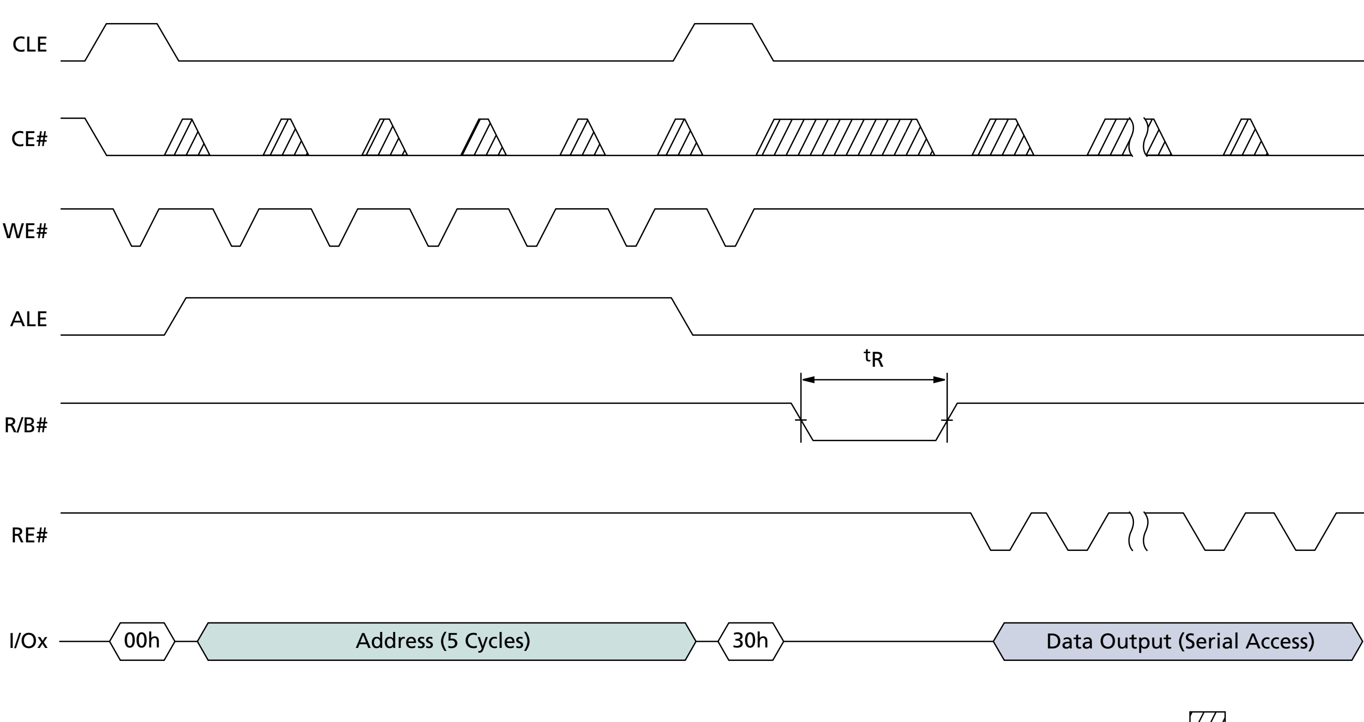
On initial power up, each device defaults to read mode. To enter the read mode while in operation, write the 00h-30h command sequence to the command register along with the five ADDRESS cycles.

Writing 00h to the command register starts the ADDRESS LATCH cycle. Five ADDRESS cycles are input next. Finally the 30h command is loaded into the command register.

While monitoring the read status to determine when the ^{t}R (transfer from Flash array to data register) is complete, the user must re-issue the READ (00h) command to make the change from STATUS to DATA. (See Figure 44 on page 48 and Figure 45 on page 49 for examples.) After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate. (See Figure 18 on page 23.)

Figure 18: PAGE READ Operation



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RANDOM DATA READ 05h-E0h

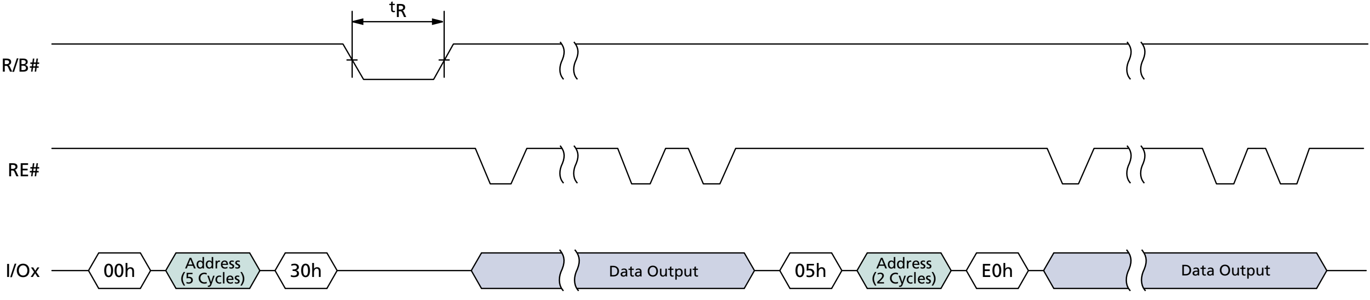
The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h sequence).

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (two cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially. See Figure 19 on page 24.

Figure 19: RANDOM DATA READ Operation



PAGE READ CACHE MODE START 31h; PAGE READ CACHE MODE START LAST 3Fh

Micron NAND Flash devices have a cache register that can be used to increase READ operation speed when accessing sequential pages in a block.

First, a normal PAGE READ (00h-30h) command sequence is issued. (See Figure 20 on page 25 for operation details.) The R/B# signal goes LOW for ^{t}R during the time it takes to transfer the first page of data from the memory to the data register. After R/B# returns to HIGH, the PAGE READ CACHE MODE START (31h) command is latched into the command register. R/B# goes LOW for ^{t}DCBSYR1 while data is being transferred from the data register to the cache register. Once the data register contents are transferred to the cache register, another PAGE READ is automatically started as part of the 31h command. Data is transferred from the next sequential page of the memory array to the data register during the same time data is being read serially (pulsing of RE#) from the cache register. If the total time to output data exceeds ^{t}R, then the PAGE READ is hidden.

The second and subsequent pages of data are transferred to the cache register by issuing additional 31h commands. R/B# will stay LOW up to ^{t}DCBSYR2. This time can vary, depending on whether the previous memory-to-data-register transfer was completed prior to issuing the next 31h command. If the data transfer from memory to the data register is not completed before the 31h command is issued, R/B# stays LOW until the transfer is complete.

It is not necessary to output a whole page of data before issuing another 31h command. R/B# will stay LOW until the previous PAGE READ is complete and the data has been transferred to the cache register.

To read out the last page of data, the PAGE READ CACHE MODE START LAST (3Fh) command is issued. This command transfers data from the data register to the cache register without issuing another PAGE READ. (See Figure 20 on page 25.)

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Figure 20: PAGE READ CACHE MODE

CLE

CE#

WE#

ALE

R/B#

RE#

I/Ox

00h

Address (5 Cycles)

30h

tR

31h

tDCBSYR1

Data Output (Serial Access)

31h

tDCBSYR2

Data Output (Serial Access)

3fh

tDCBSYR2

Data Output (Serial Access)

Don't Care

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