Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

DDR4 SDRAM

MT40A1G4

MT40A512M8

MT40A256M16

Features

- $V_{DD} = V_{DDQ} = 1.2V \pm 60mV$
- $V_{PP} = 2.5V, -125mV/+250mV$
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- T_C maximum up to 95°C
  - 64ms, 8192-cycle refresh up to 85°C
  - 32ms, 8192-cycle refresh at >85°C to 95°C
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test (x16)
- sPPR and hPPR capability
- JEDEC JESD-79-4 compliant

Options[1]   Marking

- Configuration
  - 1 Gig x 4   1G4
  - 512 Meg x 8   512M8
  - 256 Meg x 16   256M16[2]
- FBGA package (Pb-free) – x4, x8
  - 78-ball (9mm x 11.5mm) – Rev. A   HX
  - 78-ball (9mm x 10.5mm) – Rev. B   RH
- FBGA package (Pb-free) – x16
  - 96-ball (9mm x 14mm) – Rev. A   HA
  - 96-ball (9mm x 14mm) – Rev. B   GE
- Timing – cycle time
  - 0.625ns @ CL = 22 (DDR4-3200)   -062E
  - 0.682ns @ CL = 20 (DDR4-2933)   -068E
  - 0.682ns @ CL = 21 (DDR4-2933)   -068
  - 0.750ns @ CL = 18 (DDR4-2666)   -075E
  - 0.750ns @ CL = 19 (DDR4-2666)   -075
  - 0.833ns @ CL = 16 (DDR4-2400)   -083E
  - 0.833ns @ CL = 17 (DDR4-2400)   -083
  - 0.937ns @ CL = 15 (DDR4-2133)   -093E
  - 0.937ns @ CL = 16 (DDR4-2133)   -093
  - 1.071ns @ CL = 13 (DDR4-1866)   -107E
- Operating temperature
  - Commercial (0° ≤ T_C ≤ 95°C)   None
  - Industrial (–40° ≤ T_C ≤ 95°C)   IT
  - Revision   :A
                                            :B

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.
         2. Not available on Rev. A.
         3. Restricted and limited availability.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-062E[6]	3200	22-22-22	13.75	13.75	13.75
-068E[5]	2933	20-20-20	13.64	13.64	13.64
-068[5]	2933	21-21-21	14.32	14.32	14.32
-075E[4]	2666	18-18-18	13.5	13.5	13.5
-075[4]	2666	19-19-19	14.25	14.25	14.25
-083E[3]	2400	16-16-16	13.32	13.32	13.32
-083[3]	2400	17-17-17	14.16	14.16	14.16
-093E[2]	2133	15-15-15	14.06	14.06	14.06
-093[2]	2133	16-16-16	15	15	15
-107E[1]	1866	13-13-13	13.92	13.92	13.92

Notes: 1. Backward compatible to 1600, CL = 11.
2. Backward compatible to 1600, CL = 11 and 1866, CL = 13.
3. Backward compatible to 1600, CL = 11; 1866, CL = 13; and 2133, CL = 15.
4. Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; and 2400, CL = 17.
5. Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; 2400, CL = 17; and 2666, CL = 19. Speed offering may have restricted availability.
6. Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; 2400, CL = 17; 2666, CL = 19; and 2933, CL = 20 and CL = 21. Speed offering may have restricted availability.

Table 2: Addressing

Parameter	1024 Meg x 4	512 Meg x 8	256 Meg x 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	64K (A[15:0])	32K (A[14:0])	32K (A[14:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size[1]	512B / 1KB[2]	1KB	2KB

Notes: 1. Page size is per bank, calculated as follows:
Page size = $2^{COLBITS}$ × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.
2. Die revision dependant.

Figure 1: Order Part Number Example

Example Part Number: MT40A1G4-083:B

MT40A	Configuration	Package	Speed	-		Revision	:

Configuration	
1 Gig x 4	1G4
512 Meg x 8	512M8
256Meg x 16	256M16

Package	Mark
78-ball 9.0mm x 11.5mm FBGA	HX
78-ball 8.0mm x 10.5mm FBGA	RH
96-ball 9.0mm x 14.0mm FBGA	HA
96-ball 9.0mm x 14.0mm FBGA	GE

Revision
:A, :B

Case Temperature	
Commercial	None
Industrial	IT

Speed Grade	
−107E	$^tCK = 1.071ns$, CL = 13
−093	$^tCK = 0.937ns$, CL = 16
−093E	$^tCK = 0.937ns$, CL = 15
−083	$^tCK = 0.833ns$, CL = 17
−083E	$^tCK = 0.833ns$, CL = 16
−075	$^tCK = 0.750ns$, CL = 19
−075E	$^tCK = 0.750ns$, CL = 18
−068	$^tCK = 0.682ns$, CL = 21
−068E	$^tCK = 0.682ns$, CL = 20
−062E	$^tCK = 0.625ns$, CL = 22

Contents

List of Figures

List of Tables

General Notes and Description

Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM for the x16 configuration and as a 16-bank DRAM for the x4 and x8 configurations. The DDR4 SDRAM uses an $8n$-prefetch architecture to achieve high-speed operation. The $8n$-prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins.

A single READ or WRITE operation for the DDR4 SDRAM consists of a single $8n$-bit wide, four-clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Industrial Temperature

An industrial temperature (IT) device option requires that the case temperature not exceed below –40°C or above 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when operating outside of the commercial temperature range, when T_C is between –40°C and 0°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation), unless specifically stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#" and/or overbar characters. For example, differential data strobe pair DQS, DQS# is now referred to as DQS_t, DQS_c.
- The term "_n" is used to represent a signal that is active LOW and replaces the previously used "#" and/or overbar characters. For example: CS# is now referred to as CS_n.
- The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported, and can result in unknown operation.
- Addressing is denoted as BG[n] for bank group, BA[n] for bank address, and A[n] for row/col address.
- The NOP command is not allowed, except when exiting maximum power savings mode or when entering gear-down mode, and only a DES command should be used.

- Not all features described within this document may be available on the Rev. A (first) version.
- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after V_{DD} has reached the stable power-on level, which is achieved by toggling CKE at least once every 8192 × ^{t}REFI. However, in the event CKE is fixed HIGH, toggling CS_n at least once every 8192 × ^{t}REFI is an acceptable alternative. Placing the DRAM into self refresh mode also alleviates the need to toggle CKE.
- Not all features designated in the data sheet may be supported by earlier die revisions due to late definition by JEDEC.

Definitions of the Device-Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z: A device pin is tri-state.
- ODT: A device pin terminates with the ODT setting, which could be terminating or tristate depending on the mode register setting.

Definitions of the Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDQ}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally $V_{OL(DC)}$ if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z: All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.
- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDQ}.
- The specification requires 8,192 refresh commands within 64ms between 0 ⁰C and 85 ⁰C. This allows for a ^{t}REFI of 7.8125µs (the use of "7.8µs" is truncated from 7.8125µs). The specification also requires 8,192 refresh commands within 32ms between 85 ⁰C and 95 ⁰C. This allows for a ^{t}REFI of 3.90625µs (the use of "3.9µs" is truncated from 3.90625µs).

Functional Block Diagrams

DDR4 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 16-bank (4-banks per Bank Group) DRAM.

Figure 2: 1 Gig x 4 Functional Block Diagram
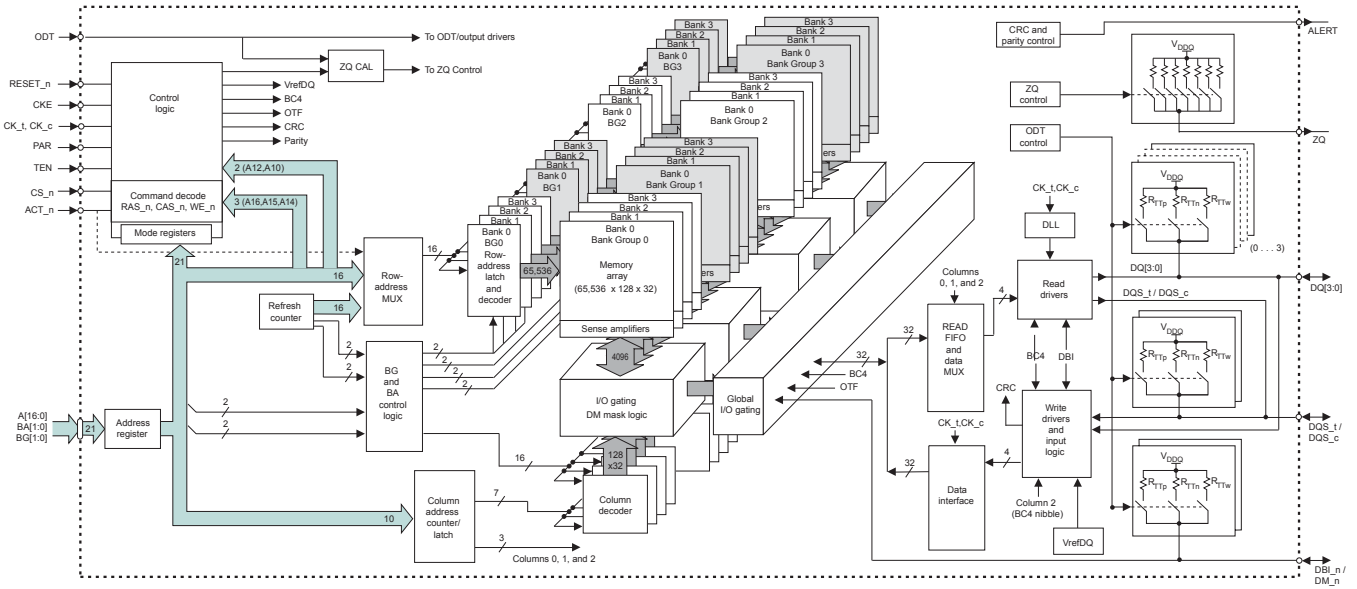
Figure 3: 512 Meg x 8 Functional Block Diagram
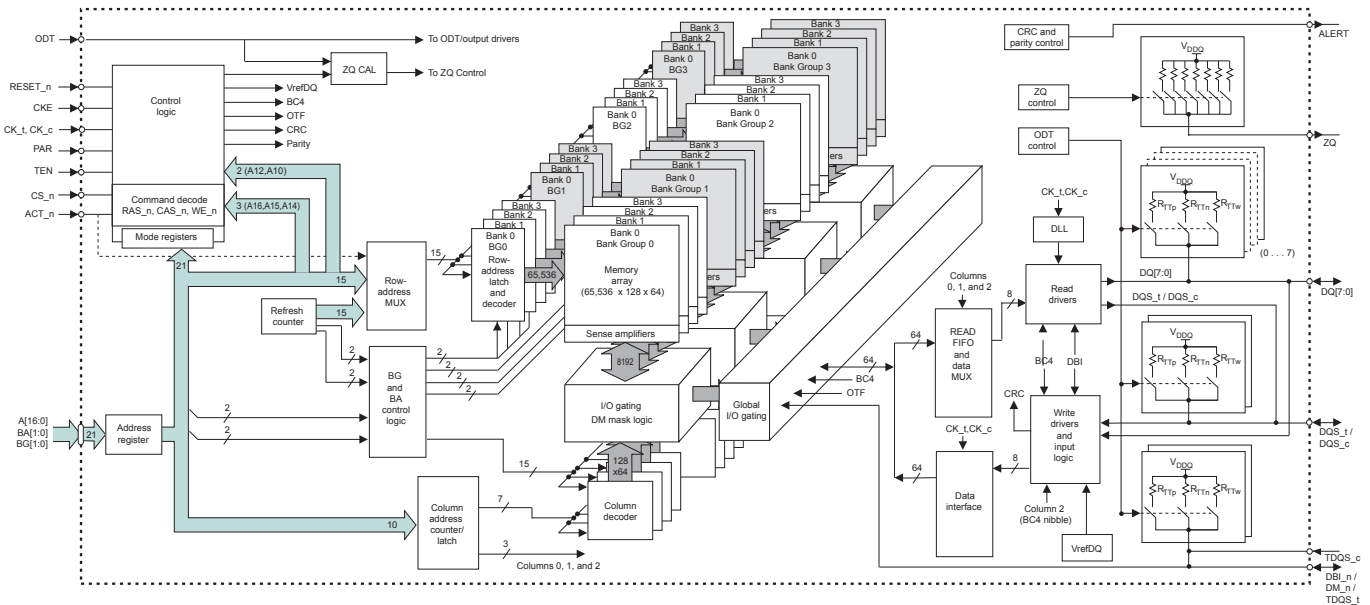
Figure 4: 256 Meg x 16 Functional Block Diagram
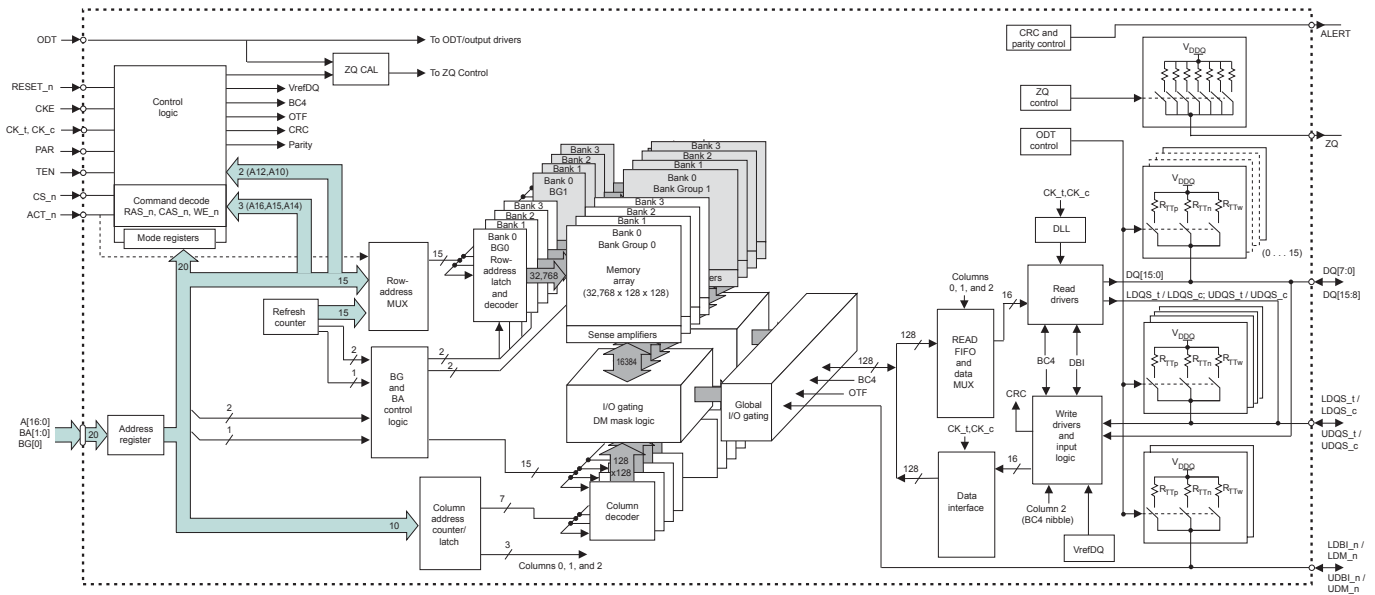
Ball Assignments

Figure 5: 78-Ball x4, x8 Ball Assignments
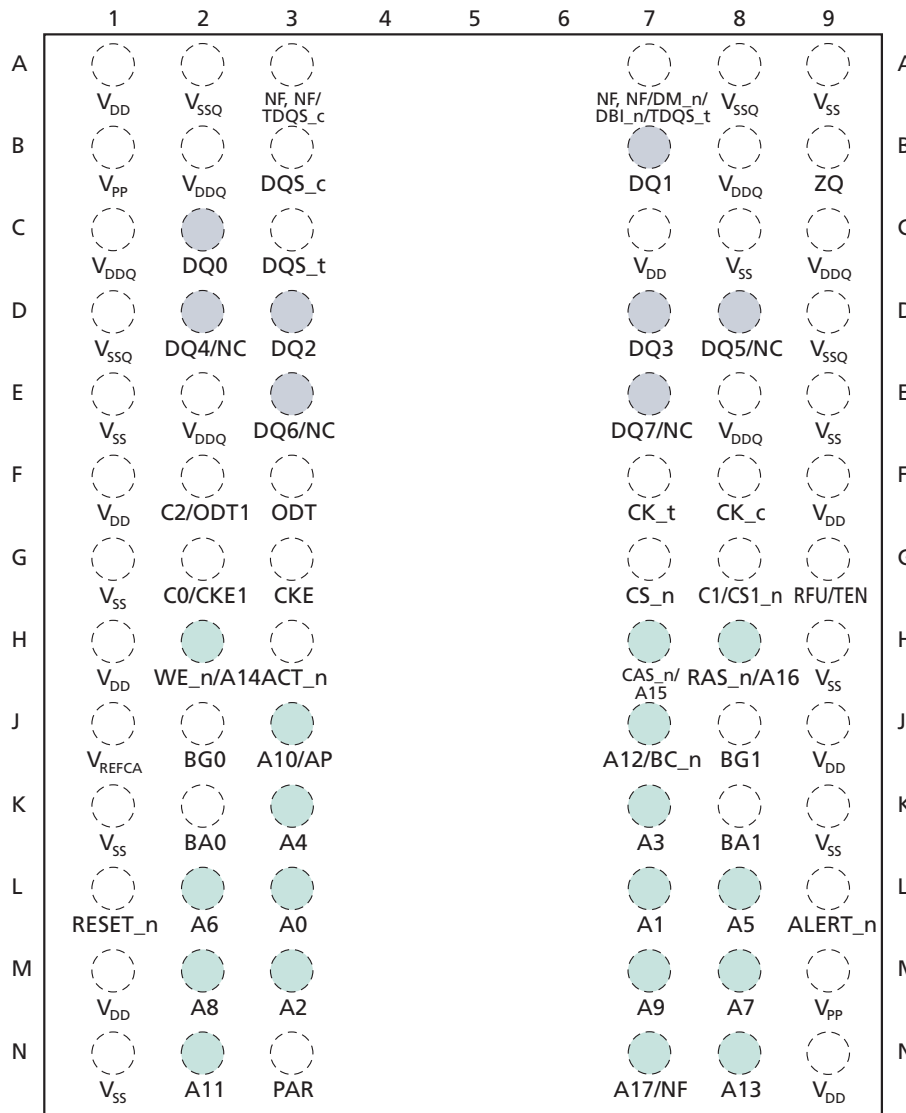
Notes: 1. See Ball Descriptions.
2. A comma "," separates the configuration; a slash "/" defines a selectable function. For example: Ball A7 = NF, NF/DM_n/DBI_n/TDQS_t where NF applies to the x4 configuration only. NF/DM_n/DBI_n/TDQS_t applies to the x8 configuration only and is selectable between NF, DM_n, DBI_n, or TDQS_t via MRS.
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Figure 6: 96-Ball x16 Ball Assignments
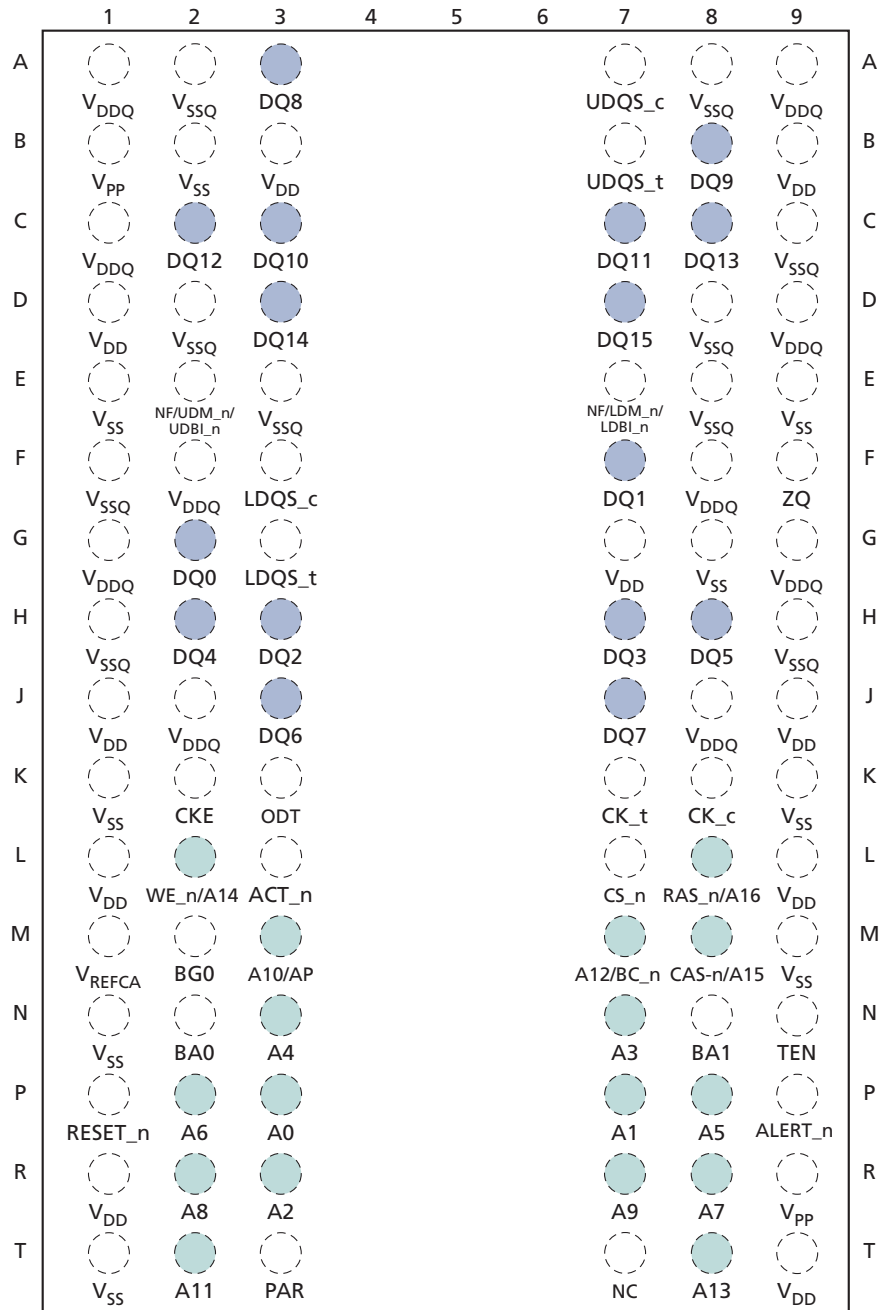
Notes: 1. See Ball Descriptions.
2. A slash "/" defines a selectable function. For example: Ball E7 = NF/LDM_n. If data mask is enabled via the MRS, ball E7 = LDM_n. If data mask is disabled in the MRS, E7 = NF (no function).
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Ball Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 devices. All pins listed may not be supported on the device defined in this data sheet. See the Ball Assignments section to review all pins used on this device.

Table 3: Ball Descriptions

Symbol	Type	Description
A[17:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts, and A17 is only used on some 16Gb parts.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
ACT_n	Input	**Command input:** ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	**Bank address inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	**Stack address inputs:** These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.