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DDR4 SDRAM

MT40A2G4
MT40A1G8
MT40A512M16

Features

- $V_{DD} = V_{DDQ}$ = 1.2V ±60mV
- V_{PP} = 2.5V, –125mV, +250mV
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- T_C maximum up to 95°C
  - 64ms, 8192-cycle refresh up to 85°C
  - 32ms, 8192-cycle refresh at >85°C to 95°C
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- 8*n*-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test (x16)
- JEDEC JESD-79-4 compliant
- sPPR and hPPR capability

Options[1]	Marking
• Configuration	
– 2 Gig x 4	2G4
– 1 Gig x 8	1G8
– 512 Meg x 16	512M16
• 78-ball FBGA package (Pb-free) – x4, x8	
– 9mm x 13.2mm – Rev. A	PM
– 8mm x 12mm – Rev. B, D, G	WE
– 7.5mm x 11mm – Rev. E, H	SA
• 96-ball FBGA package (Pb-free) – x16	
– 9mm x 14mm – Rev. A	HA
– 8mm x 14mm – Rev. B	JY
– 7.5mm x 13.5mm – Rev. D, E, H	LY
• Timing – cycle time	
– 0.625ns @ CL = 22 (DDR4-3200)	-062E
– 0.682ns @ CL = 20 (DDR4-2933)	-068E
– 0.682ns @ CL = 21 (DDR4-2933)	-068
– 0.750ns @ CL = 18 (DDR4-2666)	-075E
– 0.750ns @ CL = 19 (DDR4-2666)	-075
– 0.833ns @ CL = 16 (DDR4-2400)	-083E
– 0.833ns @ CL = 17 (DDR4-2400)	-083
– 0.937ns @ CL = 15 (DDR4-2133)	-093E
– 0.937ns @ CL = 16 (DDR4-2133)	-093
– 1.071ns @ CL = 13 (DDR4-1866)	-107E
• Operating temperature	
– Commercial (0° ≤ T_C ≤ 95°C)	None
– Industrial (–40° ≤ T_C ≤ 95°C)	IT
• Revision	:A, :B, :D, :G, :E, :H

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-062E[6]	3200	22-22-22	13.75	13.75	13.75
-068E[5]	2933	20-20-20	13.64	13.64	13.64
-068[5]	2933	21-21-21	14.32	14.32	14.32

Table 1: Key Timing Parameters (Continued)

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-075E[4]	2666	18-18-18	13.5	13.5	13.5
-075[4]	2666	19-19-19	14.25	14.25	14.25
-083E[3]	2400	16-16-16	13.32	13.32	13.32
-083[3]	2400	17-17-17	14.16	14.16	14.16
-093E[2]	2133	15-15-15	14.06	14.06	14.06
-093[2]	2133	16-16-16	15	15	15
-107E[1]	1866	13-13-13	13.92	13.92	13.92

Notes:
1. Backward compatible to 1600, CL = 11.
2. Backward compatible to 1600, CL = 11 and 1866, CL = 13.
3. Backward compatible to 1600, CL = 11; 1866, CL = 13; and 2133, CL = 15.
4. Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; and 2400, CL = 17.
5. Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; 2400, CL = 17; and 2666, CL = 19. Speed offering may have restricted availability.
6. Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; 2400, CL = 17; 2666, CL = 19; and 2933, CL = 20 and CL = 21. Speed offering may have restricted availability.

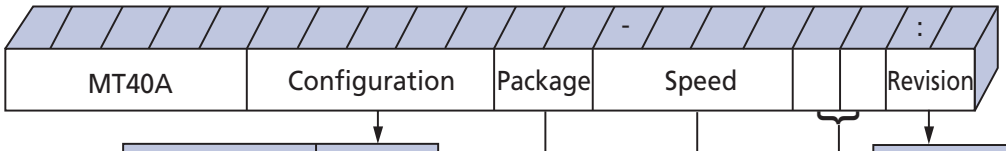
Table 2: Addressing

Parameter	2048 Meg x 4	1024 Meg x 8	512 Meg x 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	128K (A[16:0])	64K (A[15:0])	64K (A[15:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size[1]	512B/1KB[2]	1KB	2KB

Notes:
1. Page size is per bank, calculated as follows:
   Page size = $2^{COLBITS}$ × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.
2. Die Rev. dependant.

Figure 1: Order Part Number Example

Example Part Number: MT40A1G8-083:B



Configuration	
2 Gig x 4	2G4
1 Gig x 8	1G8
512 Meg x 16	512M16

Revision
:A, :B, :D, :G, :E, :H

Case Temperature	
Commercial	None
Industrial temperature	IT

Package	Mark
78-ball 9.0mm x 13.2mm FBGA	PM
78-ball 8.0mm x 12.0mm FBGA	WE
78-ball 7.5mm x 11.0mm FBGA	SA
96-ball 9.0mm x 14.0mm FBGA	HA
96-ball 8.0mm x 14.0mm FBGA	JY
96-ball 7.5mm x 13.5mm FBGA	LY

	Speed Grade
-107E	t_{CK} = 1.071ns, CL = 13
-093	t_{CK} = 0.937ns, CL = 16
-093E	t_{CK} = 0.937ns, CL = 15
-083	t_{CK} = 0.833ns, CL = 17
-083E	t_{CK} = 0.833ns, CL = 16
-075	t_{CK} = 0.750ns, CL = 19
-075E	t_{CK} = 0.750ns, CL = 18
-068	t_{CK} = 0.682ns, CL = 21
-068E	t_{CK} = 0.682ns, CL = 20
-062E	t_{CK} = 0.625ns, CL = 22

Contents

General Notes and Description 19
Description 19
Industrial Temperature 19
General Notes 19
Definitions of the Device-Pin Signal Level 20
Definitions of the Bus Signal Level 20
Functional Block Diagrams 21
Ball Assignments 23
Ball Descriptions 25
Package Dimensions 28
State Diagram 34
Functional Description 36
RESET and Initialization Procedure 37
Power-Up and Initialization Sequence 37
RESET Initialization with Stable Power Sequence 40
Uncontrolled Power-Down Sequence 41
Programming Mode Registers 42
Mode Register 0 45
Burst Length, Type, and Order 47
CAS Latency 48
Test Mode 48
Write Recovery(WR)/READ-to-PRECHARGE 48
DLL RESET 48
Mode Register 1 49
DLL Enable/DLL Disable 50
Output Driver Impedance Control 51
ODT $R_{TT(NOM)}$ Values 51
Additive Latency 51
Write Leveling 51
Output Disable 52
Termination Data Strobe 52
Mode Register 2 53
CAS WRITE Latency 55
Low-Power Auto Self Refresh 55
Dynamic ODT 55
Write Cyclic Redundancy Check Data Bus 55
Mode Register 3 56
Multipurpose Register 57
WRITE Command Latency When CRC/DM is Enabled 58
Fine Granularity Refresh Mode 58
Temperature Sensor Status 58
Per-DRAM Addressability 58
Gear-Down Mode 58
Mode Register 4 59
Hard Post Package Repair Mode 60
Soft Post Package Repair Mode 60
WRITE Preamble 61
READ Preamble 61
READ Preamble Training 61
Temperature-Controlled Refresh 61

Command Address Latency ... 61
Internal V_{REF} Monitor ... 61
Maximum Power Savings Mode ... 62
Mode Register 5 ... 63
Data Bus Inversion ... 64
Data Mask ... 65
CA Parity Persistent Error Mode ... 65
ODT Input Buffer for Power-Down ... 65
CA Parity Error Status ... 65
CRC Error Status ... 65
CA Parity Latency Mode ... 65
Mode Register 6 ... 66
^{t}CCD_L Programming ... 67
V_{REFDQ} Calibration Enable ... 67
V_{REFDQ} Calibration Range ... 67
V_{REFDQ} Calibration Value ... 67
Truth Tables ... 68
NOP Command ... 71
DESELECT Command ... 71
DLL-Off Mode ... 71
DLL-On/Off Switching Procedures ... 73
DLL Switch Sequence from DLL-On to DLL-Off ... 73
DLL-Off to DLL-On Procedure ... 75
Input Clock Frequency Change ... 76
Write Leveling ... 77
DRAM Setting for Write Leveling and DRAM TERMINATION Function in that Mode ... 78
Procedure Description ... 79
Write Leveling Mode Exit ... 80
Command Address Latency ... 82
Low-Power Auto Self Refresh Mode ... 87
Manual Self Refresh Mode ... 87
Multipurpose Register ... 89
MPR Reads ... 90
MPR Readout Format ... 92
MPR Readout Serial Format ... 92
MPR Readout Parallel Format ... 93
MPR Readout Staggered Format ... 94
MPR READ Waveforms ... 95
MPR Writes ... 97
MPR WRITE Waveforms ... 98
MPR REFRESH Waveforms ... 99
Gear-Down Mode ... 102
Maximum Power-Saving Mode ... 105
Maximum Power-Saving Mode Entry ... 105
Maximum Power-Saving Mode Entry in PDA ... 106
CKE Transition During Maximum Power-Saving Mode ... 106
Maximum Power-Saving Mode Exit ... 106
Command/Address Parity ... 108
Per-DRAM Addressability ... 116
V_{REFDQ} Calibration ... 119
V_{REFDQ} Range and Levels ... 120
V_{REFDQ} Step Size ... 120

V_{REFDQ} Increment and Decrement Timing 121
V_{REFDQ} Target Settings 125
Connectivity Test Mode 127
Pin Mapping 127
Minimum Terms Definition for Logic Equations 128
Logic Equations for a x4 Device, When Supported 128
Logic Equations for a x8 Device, When Supported 129
Logic Equations for a x16 Device 129
CT Input Timing Requirements 129
Excessive Row Activation 131
Post Package Repair 132
Post Package Repair 132
Hard Post Package Repair 133
hPPR Row Repair - Entry 133
hPPR Row Repair – WRA Initiated (REF Commands Allowed) 133
hPPR Row Repair – WR Initiated (REF Commands NOT Allowed) 135
sPPR Row Repair 137
hPPR/sPPR Support Identifier 140
ACTIVATE Command 140
PRECHARGE Command 141
REFRESH Command 141
Temperature-Controlled Refresh Mode 144
TCR Mode – Normal Temperature Range 144
TCR Mode – Extended Temperature Range 144
Fine Granularity Refresh Mode 146
Mode Register and Command Truth Table 146
^{t}REFI and ^{t}RFC Parameters 146
Changing Refresh Rate 149
Usage with TCR Mode 149
Self Refresh Entry and Exit 149
SELF REFRESH Operation 151
Self Refresh Abort 153
Self Refresh Exit with NOP Command 154
Power-Down Mode 156
Power-Down Clarifications – Case 1 161
Power-Down Entry, Exit Timing with CAL 162
ODT Input Buffer Disable Mode for Power-Down 164
CRC Write Data Feature 166
CRC Write Data 166
WRITE CRC DATA Operation 166
DBI_n and CRC Both Enabled 167
DM_n and CRC Both Enabled 167
DM_n and DBI_n Conflict During Writes with CRC Enabled 167
CRC and Write Preamble Restrictions 167
CRC Simultaneous Operation Restrictions 167
CRC Polynomial 167
CRC Combinatorial Logic Equations 168
Burst Ordering for BL8 169
CRC Data Bit Mapping 169
CRC Enabled With BC4 170
CRC with BC4 Data Bit Mapping 170
CRC Equations for x8 Device in BC4 Mode with A2 = 0 and A2 = 1 173

CRC Error Handling 174
CRC Write Data Flow Diagram 176
Data Bus Inversion 177
DBI During a WRITE Operation 177
DBI During a READ Operation 178
Data Mask 179
Programmable Preamble Modes and DQS Postambles 181
WRITE Preamble Mode 181
READ Preamble Mode 184
READ Preamble Training 184
WRITE Postamble 185
READ Postamble 185
Bank Access Operation 187
READ Operation 191
Read Timing Definitions 191
Read Timing – Clock-to-Data Strobe Relationship 192
Read Timing – Data Strobe-to-Data Relationship 194
^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), and ^{t}HZ(DQ) Calculations 195
^{t}RPRE Calculation 196
^{t}RPST Calculation 197
READ Burst Operation 198
READ Operation Followed by Another READ Operation 200
READ Operation Followed by WRITE Operation 205
READ Operation Followed by PRECHARGE Operation 211
READ Operation with Read Data Bus Inversion (DBI) 214
READ Operation with Command/Address Parity (CA Parity) 215
READ Followed by WRITE with CRC Enabled 217
READ Operation with Command/Address Latency (CAL) Enabled 218
WRITE Operation 220
Write Timing Definitions 220
Write Timing – Clock-to-Data Strobe Relationship 220
^{t}WPRE Calculation 222
^{t}WPST Calculation 223
Write Timing – Data Strobe-to-Data Relationship 223
WRITE Burst Operation 227
WRITE Operation Followed by Another WRITE Operation 229
WRITE Operation Followed by READ Operation 235
WRITE Operation Followed by PRECHARGE Operation 239
WRITE Operation with WRITE DBI Enabled 242
WRITE Operation with CA Parity Enabled 244
WRITE Operation with Write CRC Enabled 245
Write Timing Violations 250
Motivation 250
Data Setup and Hold Violations 250
Strobe-to-Strobe and Strobe-to-Clock Violations 250
ZQ CALIBRATION Commands 251
On-Die Termination 253
ODT Mode Register and ODT State Table 253
ODT Read Disable State Table 254
Synchronous ODT Mode 255
ODT Latency and Posted ODT 255
Timing Parameters 255

ODT During Reads 257
Dynamic ODT 258
Functional Description 258
Asynchronous ODT Mode 261
Electrical Specifications 262
Absolute Ratings 262
DRAM Component Operating Temperature Range 262
Electrical Characteristics – AC and DC Operating Conditions 263
Supply Operating Conditions 263
Leakages 264
V_{REFCA} Supply 264
V_{REFDQ} Supply and Calibration Ranges 265
V_{REFDQ} Ranges 266
Electrical Characteristics – AC and DC Single-Ended Input Measurement Levels 267
RESET_n Input Levels 267
Command/Address Input Levels 267
Command, Control, and Address Setup, Hold, and Derating 269
Data Receiver Input Requirements 271
Connectivity Test (CT) Mode Input Levels 275
Electrical Characteristics – AC and DC Differential Input Measurement Levels 279
Differential Inputs 279
Single-Ended Requirements for CK Differential Signals 280
Slew Rate Definitions for CK Differential Input Signals 281
CK Differential Input Cross Point Voltage 282
DQS Differential Input Signal Definition and Swing Requirements 283
DQS Differential Input Cross Point Voltage 285
Slew Rate Definitions for DQS Differential Input Signals 286
Electrical Characteristics – Overshoot and Undershoot Specifications 288
Address, Command, and Control Overshoot and Undershoot Specifications 288
Clock Overshoot and Undershoot Specifications 289
Data, Strobe, and Mask Overshoot and Undershoot Specifications 290
Electrical Characteristics – AC and DC Output Measurement Levels 290
Single-Ended Outputs 290
Differential Outputs 292
Reference Load for AC Timing and Output Slew Rate 293
Connectivity Test Mode Output Levels 294
Electrical Characteristics – AC and DC Output Driver Characteristics 295
Connectivity Test Mode Output Driver Electrical Characteristics 295
Output Driver Electrical Characteristics 297
Output Driver Temperature and Voltage Sensitivity 300
Alert Driver 300
Electrical Characteristics – On-Die Termination Characteristics 301
ODT Levels and I-V Characteristics 301
ODT Temperature and Voltage Sensitivity 303
ODT Timing Definitions 303
DRAM Package Electrical Specifications 307
Thermal Characteristics 311
Current Specifications – Measurement Conditions 312
I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions 312
I_{DD} Definitions 314
Current Specifications – Patterns and Test Conditions 318
Current Test Definitions and Patterns 318

I_{DD} Specifications 327
Current Specifications – Limits 328
Speed Bin Tables 338
Refresh Parameters By Device Density 346
Electrical Characteristics and AC Timing Parameters 347
Electrical Characteristics and AC Timing Parameters: 2666 Through 3200 359
Converting Time-Based Specifications to Clock-Based Requirements 371
Options Tables 372

List of Figures

Figure 1: Order Part Number Example 3
Figure 2: 2 Gig x 4 Functional Block Diagram 21
Figure 3: 1 Gig x 8 Functional Block Diagram 21
Figure 4: 512 Meg x 16 Functional Block Diagram 22
Figure 5: 78-Ball x4, x8 Ball Assignments 23
Figure 6: 96-Ball x16 Ball Assignments 24
Figure 7: 78-Ball FBGA – x4, x8 (PM) 28
Figure 8: 78-Ball FBGA – x4, x8 (WE) 29
Figure 9: 78-Ball FBGA – x4, x8 (SA) 30
Figure 10: 96-Ball FBGA – x16 (HA) 31
Figure 11: 96-Ball FBGA – x16 (JY) 32
Figure 12: 96-Ball FBGA – x16 (LY) 33
Figure 13: Simplified State Diagram 34
Figure 14: RESET and Initialization Sequence at Power-On Ramping 40
Figure 15: RESET Procedure at Power Stable Condition 41
Figure 16: ^{t}MRD Timing 43
Figure 17: ^{t}MOD Timing 43
Figure 18: DLL-Off Mode Read Timing Operation 72
Figure 19: DLL Switch Sequence from DLL-On to DLL-Off 74
Figure 20: DLL Switch Sequence from DLL-Off to DLL-On 75
Figure 21: Write Leveling Concept, Example 1 77
Figure 22: Write Leveling Concept, Example 2 78
Figure 23: Write Leveling Sequence (DQS Capturing CK LOW at T1 and CK HIGH at T2) 80
Figure 24: Write Leveling Exit 81
Figure 25: CAL Timing Definition 82
Figure 26: CAL Timing Example (Consecutive CS_n = LOW) 82
Figure 27: CAL Enable Timing – ^{t}MOD_CAL 83
Figure 28: ^{t}MOD_CAL, MRS to Valid Command Timing with CAL Enabled 83
Figure 29: CAL Enabling MRS to Next MRS Command, ^{t}MRD_CAL 84
Figure 30: ^{t}MRD_CAL, Mode Register Cycle Time With CAL Enabled 84
Figure 31: Consecutive READ BL8, CAL3, 1^{t}CK Preamble, Different Bank Group 85
Figure 32: Consecutive READ BL8, CAL4, 1^{t}CK Preamble, Different Bank Group 85
Figure 33: Auto Self Refresh Ranges 88
Figure 34: MPR Block Diagram 89
Figure 35: MPR READ Timing 95
Figure 36: MPR Back-to-Back READ Timing 96
Figure 37: MPR READ-to-WRITE Timing 97
Figure 38: MPR WRITE and WRITE-to-READ Timing 98
Figure 39: MPR Back-to-Back WRITE Timing 99
Figure 40: REFRESH Timing 99
Figure 41: READ-to-REFRESH Timing 100
Figure 42: WRITE-to-REFRESH Timing 100
Figure 43: Clock Mode Change from 1/2 Rate to 1/4 Rate (Initialization) 103
Figure 44: Clock Mode Change After Exiting Self Refresh 103
Figure 45: Comparison Between Gear-Down Disable and Gear-Down Enable 104
Figure 46: Maximum Power-Saving Mode Entry 105
Figure 47: Maximum Power-Saving Mode Entry with PDA 106
Figure 48: Maintaining Maximum Power-Saving Mode with CKE Transition 106
Figure 49: Maximum Power-Saving Mode Exit 107
Figure 50: Command/Address Parity Operation 108

Figure 51: Command/Address Parity During Normal Operation 110
Figure 52: Persistent CA Parity Error Checking Operation 111
Figure 53: CA Parity Error Checking – SRE Attempt 111
Figure 54: CA Parity Error Checking – SRX Attempt 112
Figure 55: CA Parity Error Checking – PDE/PDX 112
Figure 56: Parity Entry Timing Example – ^{t}MRD_PAR 113
Figure 57: Parity Entry Timing Example – ^{t}MOD_PAR 113
Figure 58: Parity Exit Timing Example – ^{t}MRD_PAR 113
Figure 59: Parity Exit Timing Example – ^{t}MOD_PAR 114
Figure 60: CA Parity Flow Diagram 115
Figure 61: PDA Operation Enabled, BL8 117
Figure 62: PDA Operation Enabled, BC4 117
Figure 63: MRS PDA Exit 118
Figure 64: V_{REFDQ} Voltage Range 119
Figure 65: Example of V_{REF} Set Tolerance and Step Size 121
Figure 66: V_{REFDQ} Timing Diagram for $V_{REF,time}$ Parameter 122
Figure 67: V_{REFDQ} Training Mode Entry and Exit Timing Diagram 123
Figure 68: V_{REF} Step: Single Step Size Increment Case 124
Figure 69: V_{REF} Step: Single Step Size Decrement Case 124
Figure 70: V_{REF} Full Step: From $V_{REF,min}$ to $V_{REF,max}$Case 125
Figure 71: V_{REF} Full Step: From $V_{REF,max}$ to $V_{REF,min}$Case 125
Figure 72: V_{REFDQ} Equivalent Circuit 126
Figure 73: Connectivity Test Mode Entry 130
Figure 74: hPPR WRA – Entry 135
Figure 75: hPPR WRA – Repair and Exit 135
Figure 76: hPPR WR – Entry 136
Figure 77: hPPR WR – Repair and Exit 136
Figure 78: sPPR – Entry 139
Figure 79: sPPR – Repair, and Exit 139
Figure 80: ^{t}RRD Timing 140
Figure 81: ^{t}FAW Timing 141
Figure 82: REFRESH Command Timing 142
Figure 83: Postponing REFRESH Commands (Example) 143
Figure 84: Pulling In REFRESH Commands (Example) 143
Figure 85: TCR Mode Example[1] 145
Figure 86: 4Gb with Fine Granularity Refresh Mode Example 148
Figure 87: OTF REFRESH Command Timing 149
Figure 88: Self Refresh Entry/Exit Timing 152
Figure 89: Self Refresh Entry/Exit Timing with CAL Mode 153
Figure 90: Self Refresh Abort 154
Figure 91: Self Refresh Exit with NOP Command 155
Figure 92: Active Power-Down Entry and Exit 157
Figure 93: Power-Down Entry After Read and Read with Auto Precharge 158
Figure 94: Power-Down Entry After Write and Write with Auto Precharge 158
Figure 95: Power-Down Entry After Write 159
Figure 96: Precharge Power-Down Entry and Exit 159
Figure 97: REFRESH Command to Power-Down Entry 160
Figure 98: Active Command to Power-Down Entry 160
Figure 99: PRECHARGE/PRECHARGE ALL Command to Power-Down Entry 161
Figure 100: MRS Command to Power-Down Entry 161
Figure 101: Power-Down Entry/Exit Clarifications – Case 1 162
Figure 102: Active Power-Down Entry and Exit Timing with CAL 162

Figure 103: REFRESH Command to Power-Down Entry with CAL 163
Figure 104: ODT Power-Down Entry with ODT Buffer Disable Mode 164
Figure 105: ODT Power-Down Exit with ODT Buffer Disable Mode 165
Figure 106: CRC Write Data Operation 166
Figure 107: CRC Error Reporting 175
Figure 108: CA Parity Flow Diagram 176
Figure 109: 1tCK vs. 2tCK WRITE Preamble Mode 181
Figure 110: 1tCK vs. 2tCK WRITE Preamble Mode, tCCD = 4 182
Figure 111: 1tCK vs. 2tCK WRITE Preamble Mode, tCCD = 5 183
Figure 112: 1tCK vs. 2 tCK WRITE Preamble Mode, tCCD = 6 183
Figure 113: 1tCK vs. 2tCK READ Preamble Mode 184
Figure 114: READ Preamble Training 185
Figure 115: WRITE Postamble 185
Figure 116: READ Postamble 186
Figure 117: Bank Group x4/x8 Block Diagram 187
Figure 118: READ Burst tCCD_S and tCCD_L Examples 188
Figure 119: Write Burst tCCD_S and tCCD_L Examples 188
Figure 120: tRRD Timing 189
Figure 121: tWTR_S Timing (WRITE-to-READ, Different Bank Group, CRC and DM Disabled) 189
Figure 122: tWTR_L Timing (WRITE-to-READ, Same Bank Group, CRC and DM Disabled) 190
Figure 123: Read Timing Definition 192
Figure 124: Clock-to-Data Strobe Relationship 193
Figure 125: Data Strobe-to-Data Relationship 194
Figure 126: tLZ and tHZ Method for Calculating Transitions and Endpoints 195
Figure 127: tRPRE Method for Calculating Transitions and Endpoints 196
Figure 128: tRPST Method for Calculating Transitions and Endpoints 197
Figure 129: READ Burst Operation, RL = 11 (AL = 0, CL = 11, BL8) 198
Figure 130: READ Burst Operation, RL = 21 (AL = 10, CL = 11, BL8) 199
Figure 131: Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group 200
Figure 132: Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group 200
Figure 133: Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group 201
Figure 134: Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group 201
Figure 135: READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group 202
Figure 136: READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group 202
Figure 137: READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group 203
Figure 138: READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group 203
Figure 139: READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group 204
Figure 140: READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group 204
Figure 141: READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group 205
Figure 142: READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group 205
Figure 143: READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group 206
Figure 144: READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group 207
Figure 145: READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group 207
Figure 146: READ (BC4) Fixed to WRITE (BC4) Fixed with 2tCK Preamble in Same or Different Bank Group 208
Figure 147: READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group 209
Figure 148: READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group 209
Figure 149: READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group 210
Figure 150: READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group 210
Figure 151: READ to PRECHARGE with 1tCK Preamble 211
Figure 152: READ to PRECHARGE with 2tCK Preamble 212
Figure 153: READ to PRECHARGE with Additive Latency and 1tCK Preamble 212
Figure 154: READ with Auto Precharge and 1tCK Preamble 213

Figure 155: READ with Auto Precharge, Additive Latency, and 1tCK Preamble 214
Figure 156: Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group 214
Figure 157: Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group 215
Figure 158: READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA Parity in Same or Different Bank Group ... 216
Figure 159: READ (BL8) to WRITE (BL8 or BC4: OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group 217
Figure 160: READ (BC4: Fixed) to WRITE (BC4: Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group 218
Figure 161: Consecutive READ (BL8) with CAL (3tCK) and 1tCK Preamble in Different Bank Group 218
Figure 162: Consecutive READ (BL8) with CAL (4tCK) and 1tCK Preamble in Different Bank Group 219
Figure 163: Write Timing Definition 221
Figure 164: tWPRE Method for Calculating Transitions and Endpoints 222
Figure 165: tWPST Method for Calculating Transitions and Endpoints 223
Figure 166: Rx Compliance Mask 224
Figure 167: V_{CENT_DQ} V_{REFDQ} Voltage Variation 224
Figure 168: Rx Mask DQ-to-DQS Timings 225
Figure 169: Rx Mask DQ-to-DQS DRAM-Based Timings 226
Figure 170: Example of Data Input Requirements Without Training 227
Figure 171: WRITE Burst Operation, WL = 9 (AL = 0, CWL = 9, BL8) 228
Figure 172: WRITE Burst Operation, WL = 19 (AL = 10, CWL = 9, BL8) 229
Figure 173: Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group 229
Figure 174: Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group 230
Figure 175: Nonconsecutive WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group 231
Figure 176: Nonconsecutive WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group 231
Figure 177: WRITE (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group 232
Figure 178: WRITE (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Different Bank Group 233
Figure 179: WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Different Bank Group 233
Figure 180: WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group 234
Figure 181: WRITE (BC4) OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group 235
Figure 182: WRITE (BL8) to READ (BL8) with 1tCK Preamble in Different Bank Group 235
Figure 183: WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group 236
Figure 184: WRITE (BC4) OTF to READ (BC4) OTF with 1tCK Preamble in Different Bank Group 237
Figure 185: WRITE (BC4) OTF to READ (BC4) OTF with 1tCK Preamble in Same Bank Group 237
Figure 186: WRITE (BC4) Fixed to READ (BC4) Fixed with 1 tCK Preamble in Different Bank Group 238
Figure 187: WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Same Bank Group 238
Figure 188: WRITE (BL8/BC4-OTF) to PRECHARGE with 1tCK Preamble 239
Figure 189: WRITE (BC4-Fixed) to PRECHARGE with 1tCK Preamble 240
Figure 190: WRITE (BL8/BC4-OTF) to Auto PRECHARGE with 1tCK Preamble 240
Figure 191: WRITE (BC4-Fixed) to Auto PRECHARGE with 1tCK Preamble 241
Figure 192: WRITE (BL8/BC4-OTF) with 1tCK Preamble and DBI 242
Figure 193: WRITE (BC4-Fixed) with 1tCK Preamble and DBI 243
Figure 194: Consecutive Write (BL8) with 1tCK Preamble and CA Parity in Different Bank Group 244
Figure 195: Consecutive WRITE (BL8/BC4-OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group 245
Figure 196: Consecutive WRITE (BC4-Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group 246
Figure 197: Nonconsecutive WRITE (BL8/BC4-OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group 247
Figure 198: Nonconsecutive WRITE (BL8/BC4-OTF) with 2tCK Preamble and Write CRC in Same or Different Bank Group 248
Figure 199: WRITE (BL8/BC4-OTF/Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group 249
Figure 200: ZQ Calibration Timing 252

Figure 201: Functional Representation of ODT 253
Figure 202: Synchronous ODT Timing with BL8 256
Figure 203: Synchronous ODT with BC4 256
Figure 204: ODT During Reads 257
Figure 205: Dynamic ODT (1^{t} CK Preamble; CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled) 259
Figure 206: Dynamic ODT Overlapped with $R_{TT(NOM)}$ (CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled) 260
Figure 207: Asynchronous ODT Timings with DLL Off 261
Figure 208: V_{REFDQ} Voltage Range 264
Figure 209: RESET_n Input Slew Rate Definition 267
Figure 210: Single-Ended Input Slew Rate Definition 269
Figure 211: DQ Slew Rate Definitions 272
Figure 212: Rx Mask Relative to ^{t}DS/^{t}DH 274
Figure 213: Rx Mask Without Write Training 275
Figure 214: TEN Input Slew Rate Definition 276
Figure 215: CT Type-A Input Slew Rate Definition 276
Figure 216: CT Type-B Input Slew Rate Definition 277
Figure 217: CT Type-C Input Slew Rate Definition 278
Figure 218: CT Type-D Input Slew Rate Definition 278
Figure 219: Differential AC Swing and “Time Exceeding AC-Level” ^{t}DVAC 279
Figure 220: Single-Ended Requirements for CK 281
Figure 221: Differential Input Slew Rate Definition for CK_t, CK_c 282
Figure 222: $V_{IX(CK)}$ Definition 282
Figure 223: Differential Input Signal Definition for DQS_t, DQS_c 283
Figure 224: DQS_t, DQS_c Input Peak Voltage Calculation and Range of Exempt non-Monotonic Signaling 284
Figure 225: V_{IXDQS} Definition 285
Figure 226: Differential Input Slew Rate and Input Level Definition for DQS_t, DQS_c 286
Figure 227: ADDR, CMD, CNTL Overshoot and Undershoot Definition 288
Figure 228: CK Overshoot and Undershoot Definition 289
Figure 229: Data, Strobe, and Mask Overshoot and Undershoot Definition 290
Figure 230: Single-ended Output Slew Rate Definition 291
Figure 231: Differential Output Slew Rate Definition 293
Figure 232: Reference Load For AC Timing and Output Slew Rate 294
Figure 233: Connectivity Test Mode Reference Test Load 294
Figure 234: Connectivity Test Mode Output Slew Rate Definition 295
Figure 235: Output Driver During Connectivity Test Mode 296
Figure 236: Output Driver: Definition of Voltages and Currents 297
Figure 237: Alert Driver 301
Figure 238: ODT Definition of Voltages and Currents 302
Figure 239: ODT Timing Reference Load 303
Figure 240: ^{t}ADC Definition with Direct ODT Control 305
Figure 241: ^{t}ADC Definition with Dynamic ODT Control 305
Figure 242: ^{t}AOFAS and ^{t}AONAS Definitions 306
Figure 243: Thermal Measurement Point 312
Figure 244: Measurement Setup and Test Load for I_{DDx}, I_{DDPx}, and I_{DDQx} 314
Figure 245: Correlation: Simulated Channel I/O Power to Actual Channel I/O Power 314

List of Tables

Table 1: Key Timing Parameters 1
Table 2: Addressing 2
Table 3: Ball Descriptions 25
Table 4: State Diagram Command Definitions 35
Table 5: Supply Power-up Slew Rate 37
Table 6: Address Pin Mapping 45
Table 7: MR0 Register Definition 45
Table 8: Burst Type and Burst Order 47
Table 9: Address Pin Mapping 49
Table 10: MR1 Register Definition 49
Table 11: Additive Latency (AL) Settings 51
Table 12: TDQS Function Matrix 52
Table 13: Address Pin Mapping 53
Table 14: MR2 Register Definition 53
Table 15: Address Pin Mapping 56
Table 16: MR3 Register Definition 56
Table 17: Address Pin Mapping 59
Table 18: MR4 Register Definition 59
Table 19: Address Pin Mapping 63
Table 20: MR5 Register Definition 63
Table 21: Address Pin Mapping 66
Table 22: MR6 Register Definition 66
Table 23: Truth Table – Command 68
Table 24: Truth Table – CKE 70
Table 25: MR Settings for Leveling Procedures 78
Table 26: DRAM TERMINATION Function in Leveling Mode 78
Table 27: Auto Self Refresh Mode 87
Table 28: MR3 Setting for the MPR Access Mode 89
Table 29: DRAM Address to MPR UI Translation 89
Table 30: MPR Page and MPR*x* Definitions 90
Table 31: MPR Readout Serial Format 92
Table 32: MPR Readout – Parallel Format 93
Table 33: MPR Readout Staggered Format, x4 94
Table 34: MPR Readout Staggered Format, x4 – Consecutive READs 94
Table 35: MPR Readout Staggered Format, x8 and x16 95
Table 36: Mode Register Setting for CA Parity 110
Table 37: V_{REFDQ} Range and Levels 120
Table 38: V_{REFDQ} Settings (V_{DDQ} = 1.2V) 126
Table 39: Connectivity Mode Pin Description and Switching Levels 128
Table 40: MAC Encoding of MPR Page 3 MPR3 131
Table 41: PPR MR0 Guard Key Settings 133
Table 42: DDR4 hPPR Timing Parameters DDR4-1600 through DDR4-3200 137
Table 43: sPPR Associated Rows 137
Table 44: PPR MR0 Guard Key Settings 138
Table 45: DDR4 sPPR Timing Parameters DDR4-1600 through DDR4-3200 139
Table 46: DDR4 Repair Mode Support Identifier 140
Table 47: Normal ^{t}REFI Refresh (TCR Disabled) 144
Table 48: Normal ^{t}REFI Refresh (TCR Enabled) 145
Table 49: MRS Definition 146
Table 50: REFRESH Command Truth Table 146

Table 51: tREFI and tRFC Parameters 147
Table 52: Power-Down Entry Definitions 156
Table 53: CRC Error Detection Coverage 167
Table 54: CRC Data Mapping for x4 Devices, BL8 169
Table 55: CRC Data Mapping for x8 Devices, BL8 169
Table 56: CRC Data Mapping for x16 Devices, BL8 170
Table 57: CRC Data Mapping for x4 Devices, BC4 170
Table 58: CRC Data Mapping for x8 Devices, BC4 171
Table 59: CRC Data Mapping for x16 Devices, BC4 172
Table 60: DBI vs. DM vs. TDQS Function Matrix 177
Table 61: DBI Write, DQ Frame Format (x8) 177
Table 62: DBI Write, DQ Frame Format (x16) 177
Table 63: DBI Read, DQ Frame Format (x8) 178
Table 64: DBI Read, DQ Frame Format (x16) 178
Table 65: DM vs. TDQS vs. DBI Function Matrix 179
Table 66: Data Mask, DQ Frame Format (x8) 179
Table 67: Data Mask, DQ Frame Format (x16) 179
Table 68: CWL Selection 182
Table 69: DDR4 Bank Group Timing Examples 187
Table 70: Read to Write and Write to Read Command Intervals 192
Table 71: Termination State Table 254
Table 72: Read Termination Disable Window 254
Table 73: ODT Latency at DDR4-1600/-1866/-2133/-2400/-2666/-3200 255
Table 74: Dynamic ODT Latencies and Timing (1tCK Preamble Mode and CRC Disabled) 258
Table 75: Dynamic ODT Latencies and Timing with Preamble Mode and CRC Mode Matrix 259
Table 76: Absolute Maximum Ratings 262
Table 77: Temperature Range 262
Table 78: Recommended Supply Operating Conditions 263
Table 79: V_{DD} Slew Rate 263
Table 80: Leakages 264
Table 81: V_{REFDQ} Specification 265
Table 82: V_{REFDQ} Range and Levels 266
Table 83: RESET_n Input Levels (CMOS) 267
Table 84: Command and Address Input Levels: DDR4-1600 Through DDR4-2400 267
Table 85: Command and Address Input Levels: DDR4-2666 268
Table 86: Command and Address Input Levels: DDR4-2933 and DDR4-3200 268
Table 87: Single-Ended Input Slew Rates 269
Table 88: Command and Address Setup and Hold Values Referenced – AC/DC-Based 270
Table 89: Derating Values for tIS/tIH – AC100DC75-Based 270
Table 90: Derating Values for tIS/tIH – AC90/DC65-Based 271
Table 91: DQ Input Receiver Specifications 272
Table 92: Rx Mask and tDS/tDH without Write Training 275
Table 93: TEN Input Levels (CMOS) 275
Table 94: CT Type-A Input Levels 276
Table 95: CT Type-B Input Levels 277
Table 96: CT Type-C Input Levels (CMOS) 277
Table 97: CT Type-D Input Levels 278
Table 98: Differential Input Swing Requirements for CK_t, CK_c 279
Table 99: Minimum Time AC Time tDVAC for CK 280
Table 100: Single-Ended Requirements for CK 281
Table 101: CK Differential Input Slew Rate Definition 281
Table 102: Cross Point Voltage For CK Differential Input Signals at DDR4-1600 through DDR4-2400 283

Table 103: Cross Point Voltage For CK Differential Input Signals at DDR4-2666 through DDR4-3200 283
Table 104: DDR4-1600 through DDR4-2400 Differential Input Swing Requirements for DQS_t, DQS_c 284
Table 105: DDR4-2633 through DDR4-3200 Differential Input Swing Requirements for DQS_t, DQS_c 284
Table 106: Cross Point Voltage For Differential Input Signals DQS 285
Table 107: DQS Differential Input Slew Rate Definition 286
Table 108: DDR4-1600 through DDR4-2400 Differential Input Slew Rate and Input Levels for DQS_t, DQS_c ... 286
Table 109: DDR4-2666 through DDR4-3200 Differential Input Slew Rate and Input Levels for DQS_t, DQS_c ... 287
Table 110: ADDR, CMD, CNTL Overshoot and Undershoot/Specifications 288
Table 111: CK Overshoot and Undershoot/ Specifications 289
Table 112: Data, Strobe, and Mask Overshoot and Undershoot/ Specifications 290
Table 113: Single-Ended Output Levels 290
Table 114: Single-Ended Output Slew Rate Definition 291
Table 115: Single-Ended Output Slew Rate 292
Table 116: Differential Output Levels 292
Table 117: Differential Output Slew Rate Definition 292
Table 118: Differential Output Slew Rate 293
Table 119: Connectivity Test Mode Output Levels 294
Table 120: Connectivity Test Mode Output Slew Rate 295
Table 121: Output Driver Electrical Characteristics During Connectivity Test Mode 297
Table 122: Strong Mode (34Ω) Output Driver Electrical Characteristics 298
Table 123: Weak Mode (48Ω) Output Driver Electrical Characteristics 299
Table 124: Output Driver Sensitivity Definitions 300
Table 125: Output Driver Voltage and Temperature Sensitivity 300
Table 126: Alert Driver Voltage 301
Table 127: ODT DC Characteristics 302
Table 128: ODT Sensitivity Definitions 303
Table 129: ODT Voltage and Temperature Sensitivity 303
Table 130: ODT Timing Definitions 304
Table 131: Reference Settings for ODT Timing Measurements 304
Table 132: DRAM Package Electrical Specifications for x4 and x8 Devices 307
Table 133: DRAM Package Electrical Specifications for x16 Devices 308
Table 134: Pad Input/Output Capacitance 310
Table 135: Thermal Characteristics 311
Table 136: Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions 314
Table 137: I_{DD0} and I_{PP0} Measurement-Loop Pattern[1] 318
Table 138: I_{DD1} Measurement – Loop Pattern[1] 319
Table 139: I_{DD2N}, I_{DD3N}, and I_{PP3P} Measurement – Loop Pattern[1] 320
Table 140: I_{DD2NT} and I_{DDQ2NT} Measurement – Loop Pattern[1] 321
Table 141: I_{DD4R} Measurement – Loop Pattern[1] 322
Table 142: I_{DD4W} Measurement – Loop Pattern[1] 323
Table 143: I_{DD4Wc} Measurement – Loop Pattern[1] 324
Table 144: I_{DD5R} Measurement – Loop Pattern[1] 325
Table 145: I_{DD7} Measurement – Loop Pattern[1] 326
Table 146: Timings used for I_{DD}, I_{PP}, and I_{DDQ} Measurement – Loop Patterns 327
Table 147: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. A 328
Table 148: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. B 330
Table 149: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. D 332
Table 150: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. E, G, H 334
Table 151: DDR4-1600 Speed Bins and Operating Conditions 338
Table 152: DDR4-1866 Speed Bins and Operating Conditions 339
Table 153: DDR4-2133 Speed Bins and Operating Conditions 340
Table 154: DDR4-2400 Speed Bins and Operating Conditions 341

Table 155: DDR4-2666 Speed Bins and Operating Conditions 342
Table 156: DDR4-2933 Speed Bins and Operating Conditions 343
Table 157: DDR4-3200 Speed Bins and Operating Conditions 345
Table 158: Refresh Parameters by Device Density 346
Table 159: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 347
Table 160: Electrical Characteristics and AC Timing Parameters 359
Table 161: Options - Speed Based 372
Table 162: Options - Width Based 373

General Notes and Description

Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM for the x16 configuration and as a 16-bank DRAM for the x4 and x8 configurations. The DDR4 SDRAM uses an 8*n*-prefetch architecture to achieve high-speed operation. The 8*n*-prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins.

A single READ or WRITE operation for the DDR4 SDRAM consists of a single 8*n*-bit wide, four-clock data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Industrial Temperature

An industrial temperature (IT) device option requires that the case temperature not exceed below –40°C or above 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when operating outside of the commercial temperature range, when T_C is between –40°C and 0°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation), unless specifically stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#" and/or overbar characters. For example, differential data strobe pair DQS, DQS# is now referred to as DQS_t, DQS_c.
- The term "_n" is used to represent a signal that is active LOW and replaces the previously used "#" and/or overbar characters. For example: CS# is now referred to as CS_n.
- The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported, and can result in unknown operation.
- Addressing is denoted as BG[*n*] for bank group, BA[*n*] for bank address, and A[*n*] for row/col address.
- The NOP command is not allowed, except when exiting maximum power savings mode or when entering gear-down mode, and only a DES command should be used.

- Not all features described within this document may be available on the Rev. A (first) version.
- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after V_{DD} has reached the stable power-on level, which is achieved by toggling CKE at least once every 8192 × ^{t}REFI. However, in the event CKE is fixed HIGH, toggling CS_n at least once every 8192 × ^{t}REFI is an acceptable alternative. Placing the DRAM into self refresh mode also alleviates the need to toggle CKE.
- Not all features designated in the data sheet may be supported by earlier die revisions due to late definition by JEDEC.

Definitions of the Device-Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z: A device pin is tri-state.
- ODT: A device pin terminates with the ODT setting, which could be terminating or tri-state depending on the mode register setting.

Definitions of the Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDQ}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally $V_{OL(DC)}$ if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z: All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.
- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDQ}.
- The specification requires 8,192 refresh commands within 64ms between 0 °C and 85 °C. This allows for a ^{t}REFI of 7.8125µs (the use of "7.8µs" is truncated from 7.8125µs). The specification also requires 8,192 refresh commands within 32ms between 85 °C and 95 °C. This allows for a ^{t}REFI of 3.90625µs (the use of "3.9µs" is truncated from 3.90625µs).

Functional Block Diagrams

DDR4 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 16-bank (4-banks per Bank Group) DRAM.

Figure 2: 2 Gig x 4 Functional Block Diagram

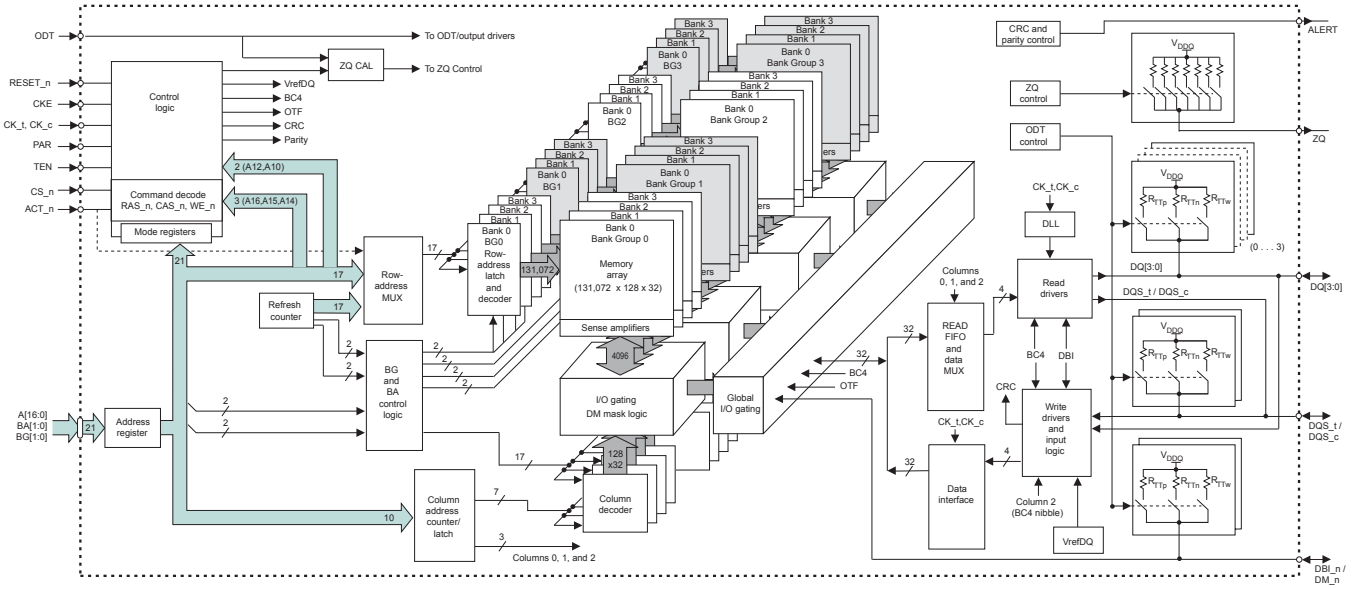


Figure 3: 1 Gig x 8 Functional Block Diagram

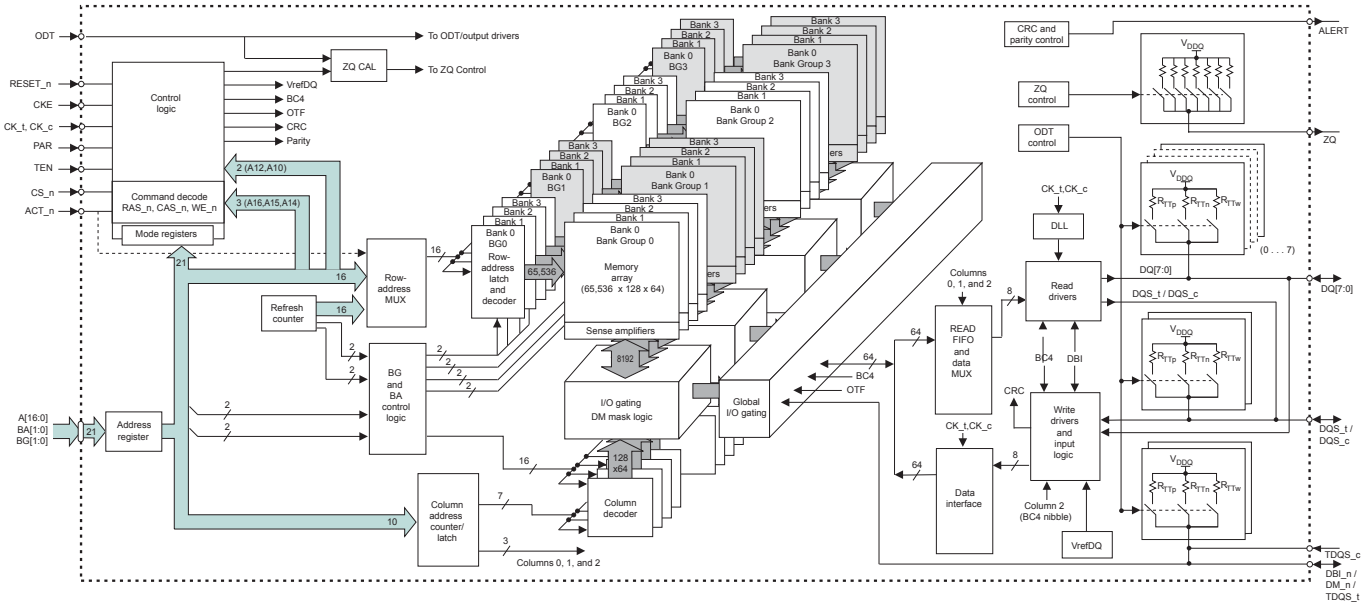
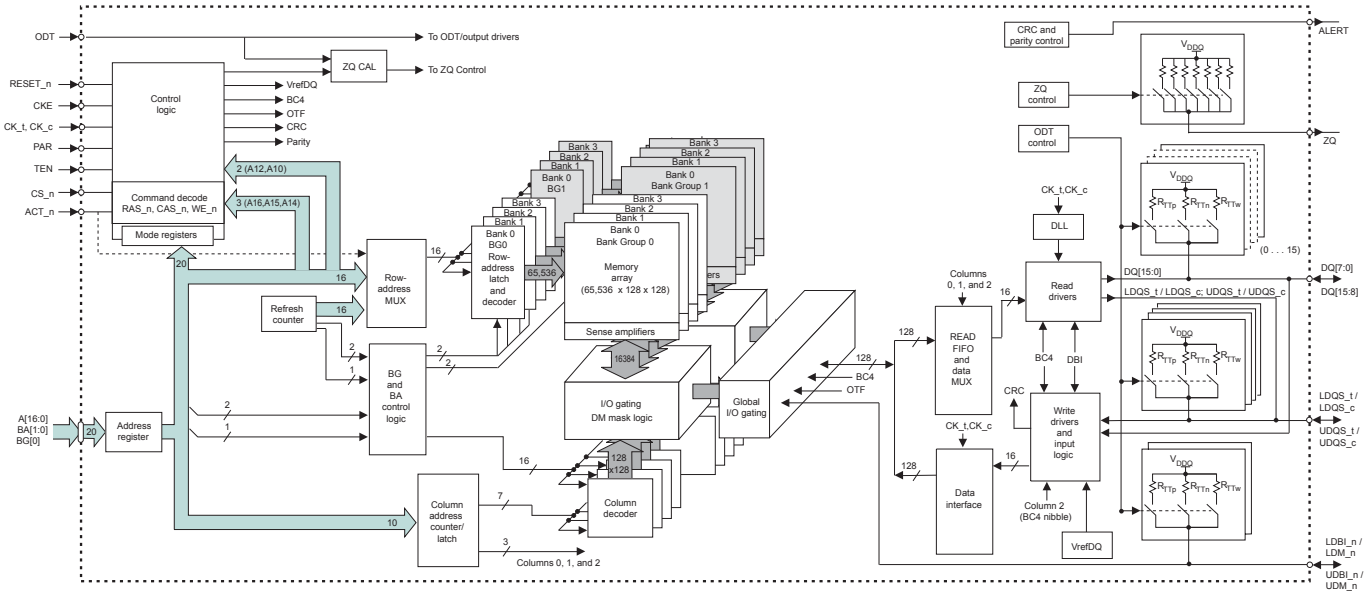
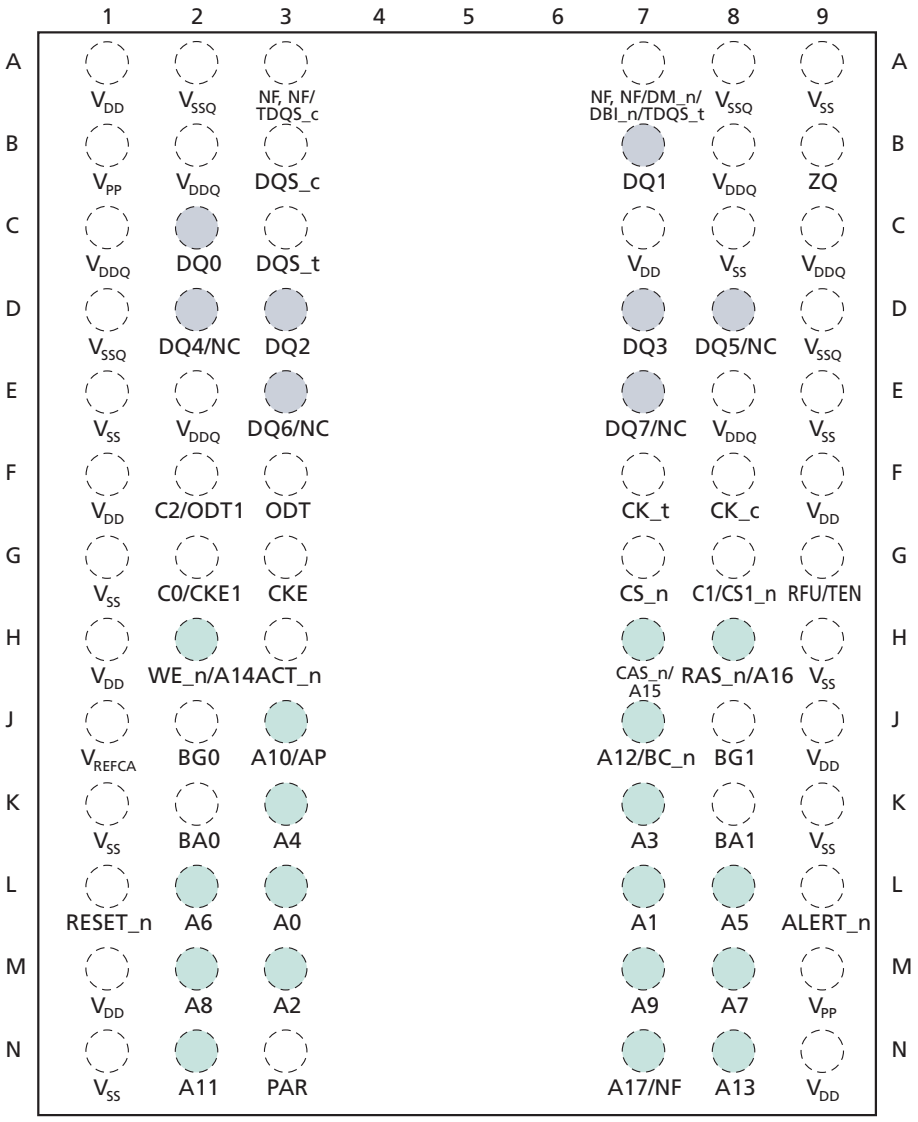


Figure 4: 512 Meg x 16 Functional Block Diagram



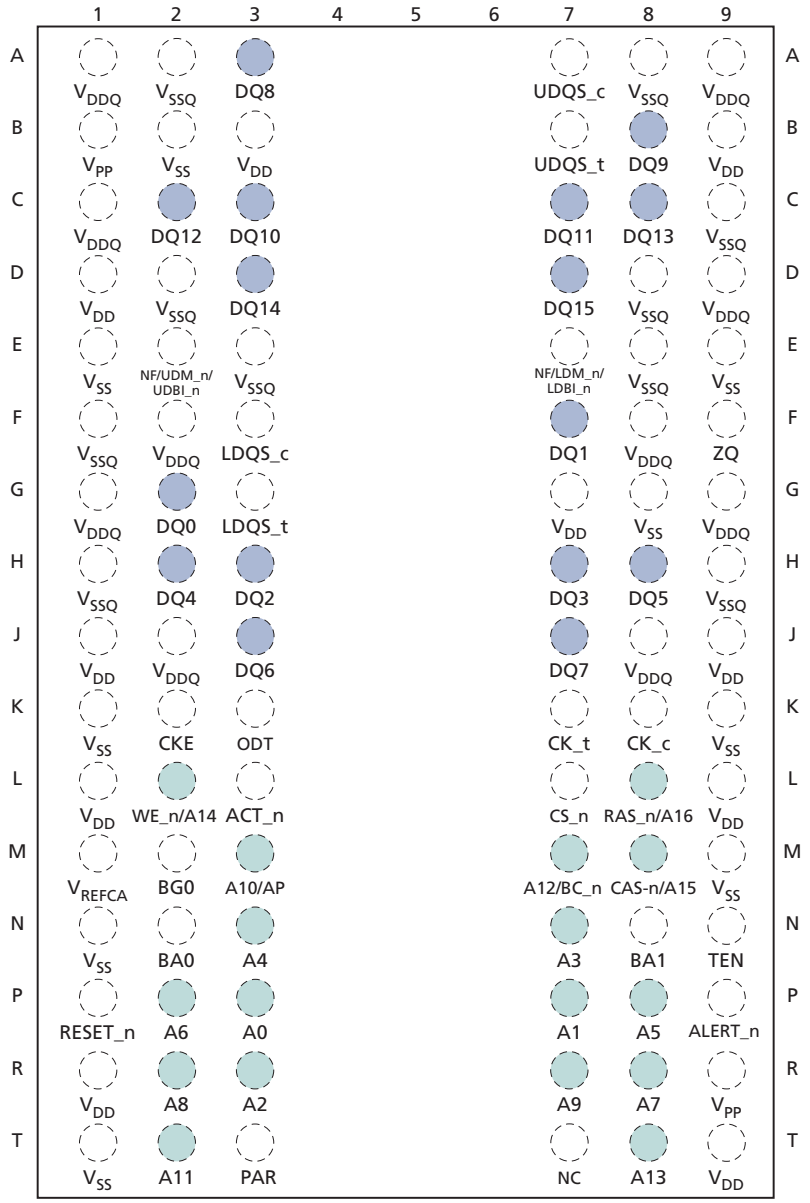
Ball Assignments

Figure 5: 78-Ball x4, x8 Ball Assignments



Notes:
1. See Ball Descriptions.
2. A comma "," separates the configuration; a slash "/" defines a selectable function. For example: Ball A7 = NF, NF/DM_n/DBI_n/TDQS_t where NF applies to the x4 configuration only. NF/DM_n/DBI_n/TDQS_t applies to the x8 configuration only and is selectable between NF, DM_n, DBI_n, or TDQS_t via MRS.
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Figure 6: 96-Ball x16 Ball Assignments



Notes:
1. See Ball Descriptions.
2. A slash "/" defines a selectable function. For example: Ball E7 = NF/LDM_n. If data mask is enabled via the MRS, ball E7 = LDM_n. If data mask is disabled in the MRS, E7 = NF (no function).
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Ball Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 devices. All pins listed may not be supported on the device defined in this data sheet. See the Ball Assignments section to review all pins used on this device.

Table 3: Ball Descriptions

Symbol	Type	Description
A[17:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts, and A17 is only used on some 16Gb parts.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
ACT_n	Input	**Command input:** ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	**Bank address inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	**Stack address inputs:** These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.