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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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DDR3 SDRAM

MT41J512M4 – 64 Meg x 4 x 8 Banks
MT41J256M8 – 32 Meg x 8 x 8 Banks
MT41J128M16 – 16 Meg x 16 x 8 Banks

Features

- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on ^{t}CK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8192 cycle refresh at 0°C to 85°C
  - 32ms, 8192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration

Options[1]	Marking
• Configuration	
– 512 Meg x 4	512M4
– 256 Meg x 8	256M8
– 128 Meg x 16	128M16
• FBGA package (Pb-free) – x4, x8	
– 78-ball (8mm x 10.5mm) Rev. H,M,J,K	DA
– 78-ball (9mm x 11.5mm) Rev. D	HX
• FBGA package (Pb-free) – x16	
– 96-ball (9mm x 14mm) Rev. D	HA
– 96-ball (8mm x 14mm) Rev. K	JT
• Timing – cycle time	
– 938ps @ CL = 14 (DDR3-2133)	-093
– 1.071ns @ CL = 13 (DDR3-1866)	-107
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.87ns @ CL = 7 (DDR3-1066)	-187E
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
• Revision	:D/:H/:J/:K/:M

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

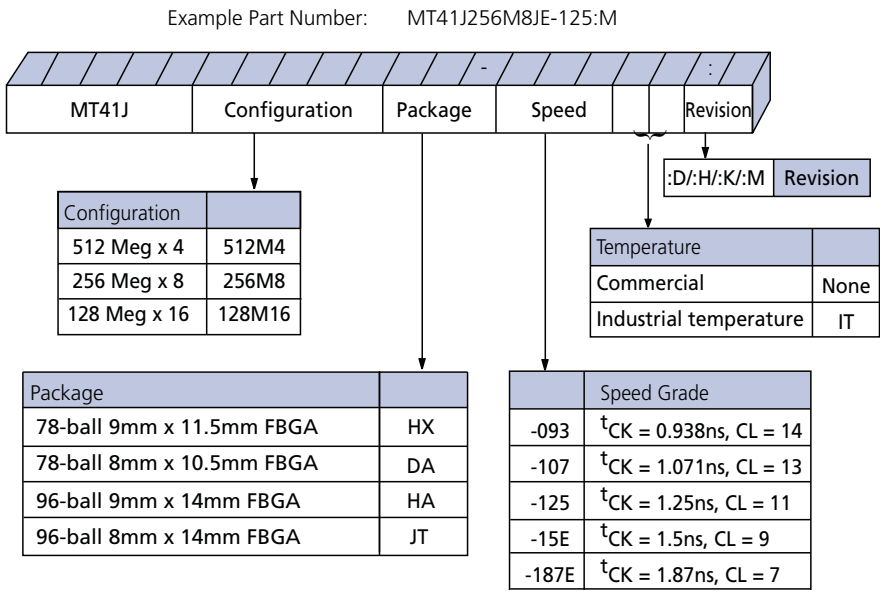
Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-093[1, 2, 3, 4]	2133	14-14-14	13.09	13.09	13.09
-107[1, 2, 3]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2,]	1600	11-11-11	13.75	13.75	13.75
-15E[1,]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Notes:
1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).
3. Backward compatible to 1600, CL = 11 (-125).
4. Backward compatible to 1866, CL = 13 (-107).

Table 2: Addressing

Parameter	512 Meg x 4	256 Meg x 8	128 Meg x 16
Configuration	64 Meg x 4 x 8 banks	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	32K (A[14:0])	32K (A[14:0])	16K (A[13:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page size	1KB	1KB	2KB

Figure 1: DDR3 Part Numbers



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

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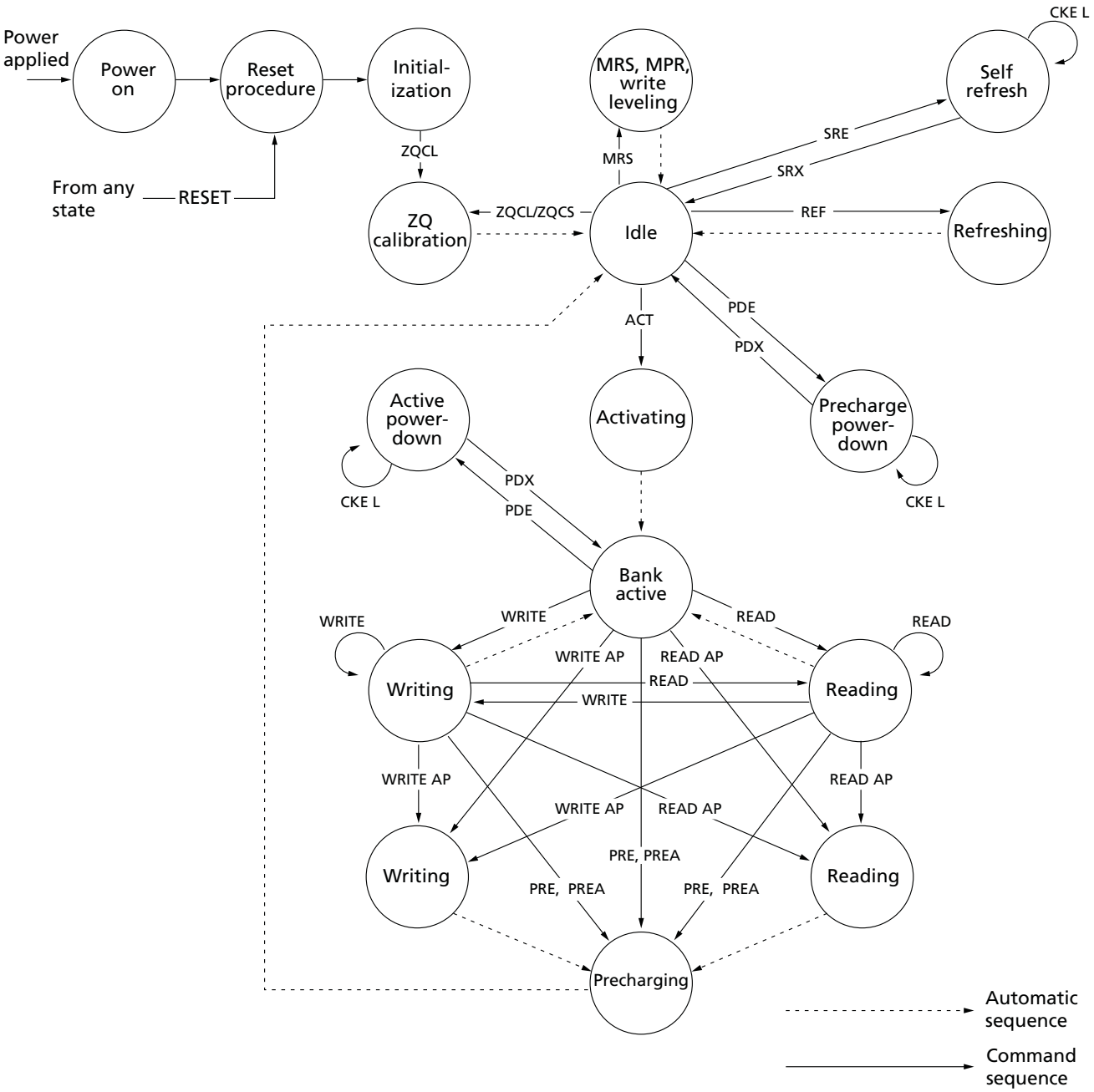
Figure 2: Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE
PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry
SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Functional Description

DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Industrial Temperature

The industrial temperature (IT) device requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is < 0°C or >95°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout this data sheet, various figures and text refer to DQs as "DQ." DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "DQS" and "CK" found throughout this data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.

- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Row addressing is denoted as A[*n*:0]. *For example,* 1Gb: *n* = 12 (x16); 1Gb: *n* = 13 (x4, x8); 2Gb: *n* = 13 (x16) and 2Gb: *n* = 14 (x4, x8); 4Gb: *n* = 14 (x16); and 4Gb: *n* = 15 (x4, x8).
- Dynamic ODT has a special use case: when DDR3 devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed. Refer to the Dynamic ODT Special Use Case section.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
  - Connect UDQS to ground via 1kΩ* resistor.
  - Connect UDQS# to V_{DD} via 1kΩ* resistor.
  - Connect UDM to V_{DD} via 1kΩ* resistor.
  - Connect DQ[15:8] individually to either V_{SS}, V_{DD}, or V_{REF} via 1kΩ resistors,* or float DQ[15:8].

  *If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.

Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

Figure 3: 512 Meg x 4 Functional Block Diagram

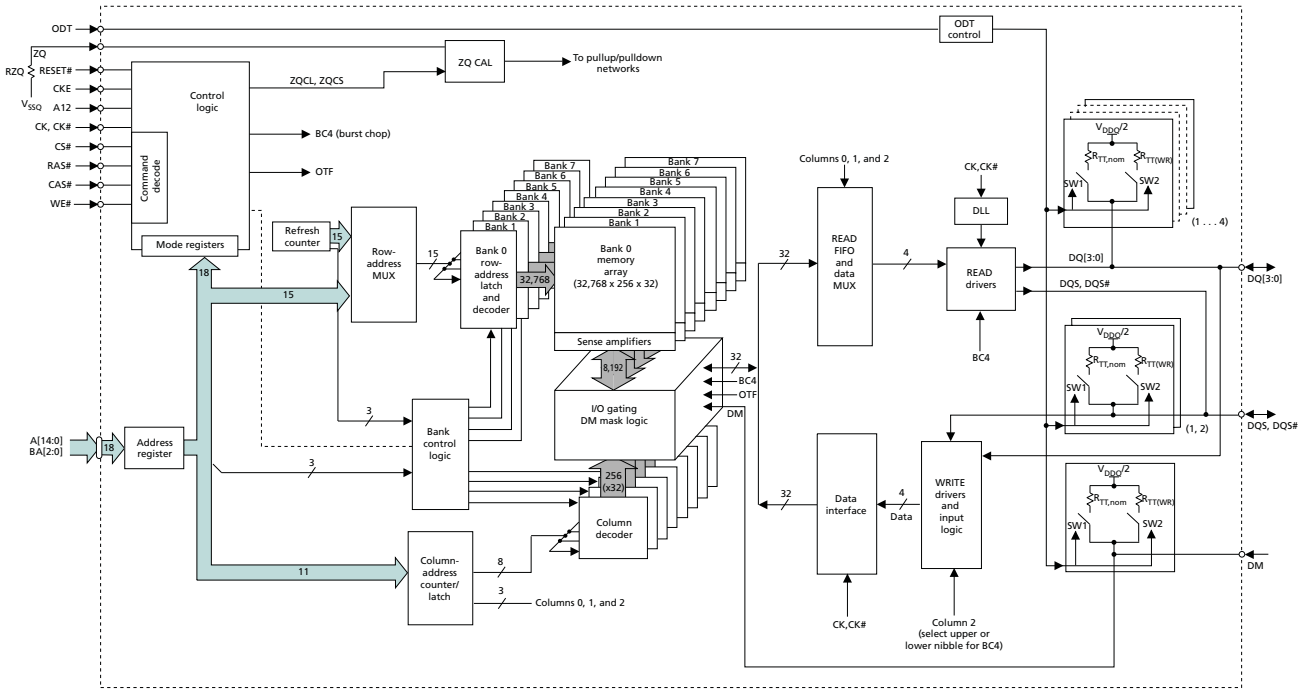


Figure 4: 256 Meg x 8 Functional Block Diagram

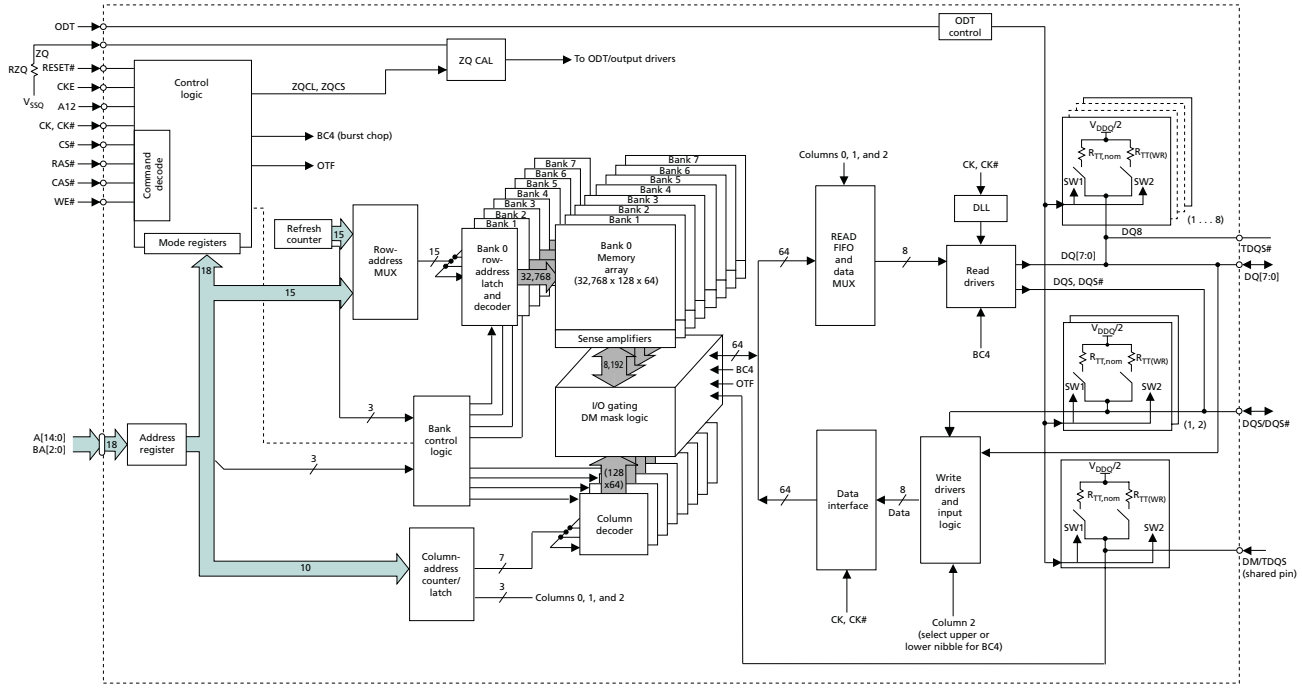
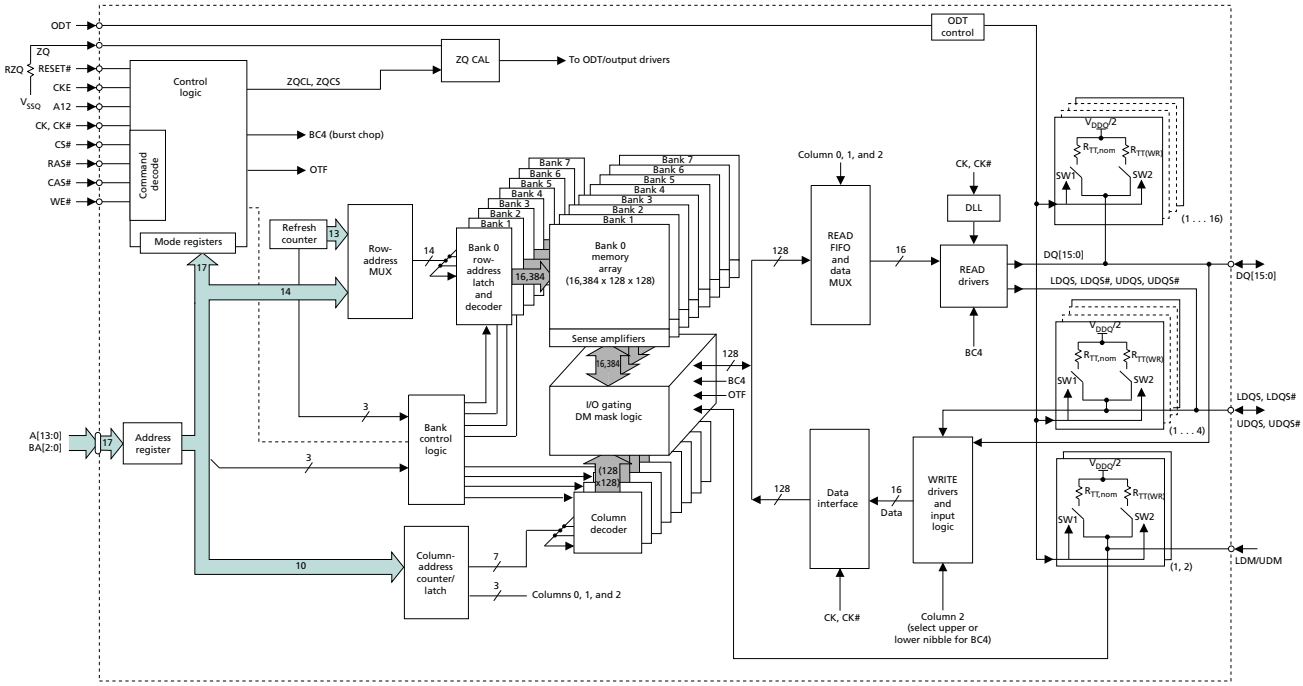
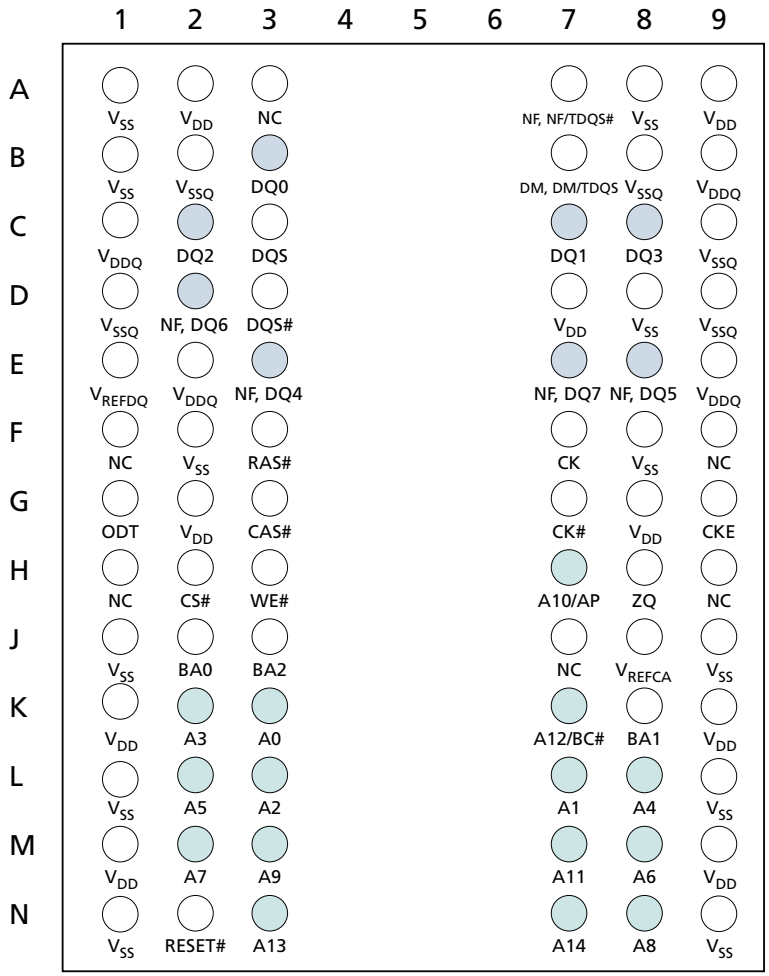


Figure 5: 128 Meg x 16 Functional Block Diagram



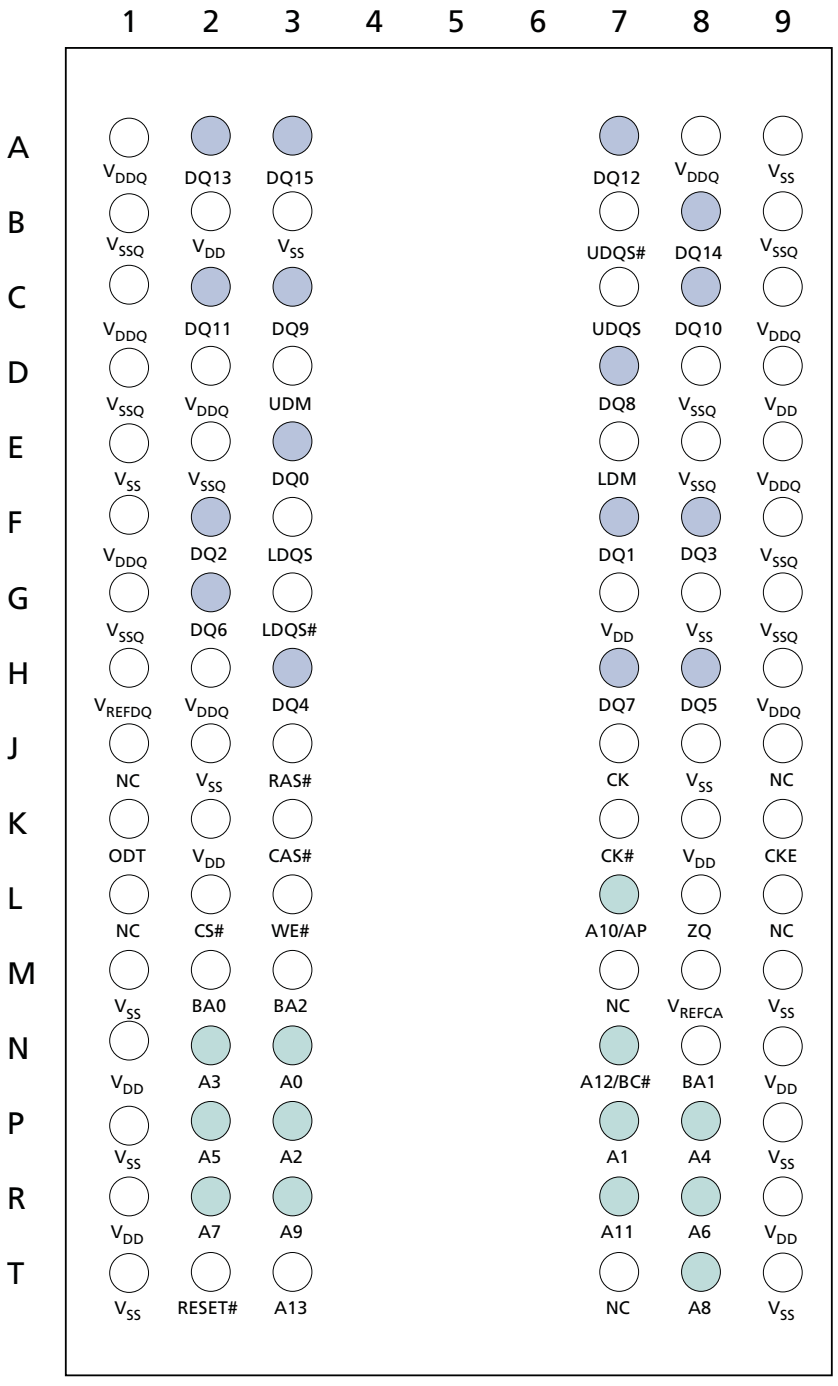
Ball Assignments and Descriptions

Figure 6: 78-Ball FBGA – x4, x8 (Top View)



Notes:
1. Ball descriptions listed in Table 3 (page 18) are listed as "x4, x8" if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function. Example: D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

Figure 7: 96-Ball FBGA – x16 (Top View)



Note: 1. Ball descriptions listed in Table 4 (page 20).

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Table 71 (page 114).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. DM has an optional use as TDQS on the x8.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	Output	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to external 240Ω resistor RZQ, which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

Table 4: 96-Ball FBGA – x16 Ball Descriptions

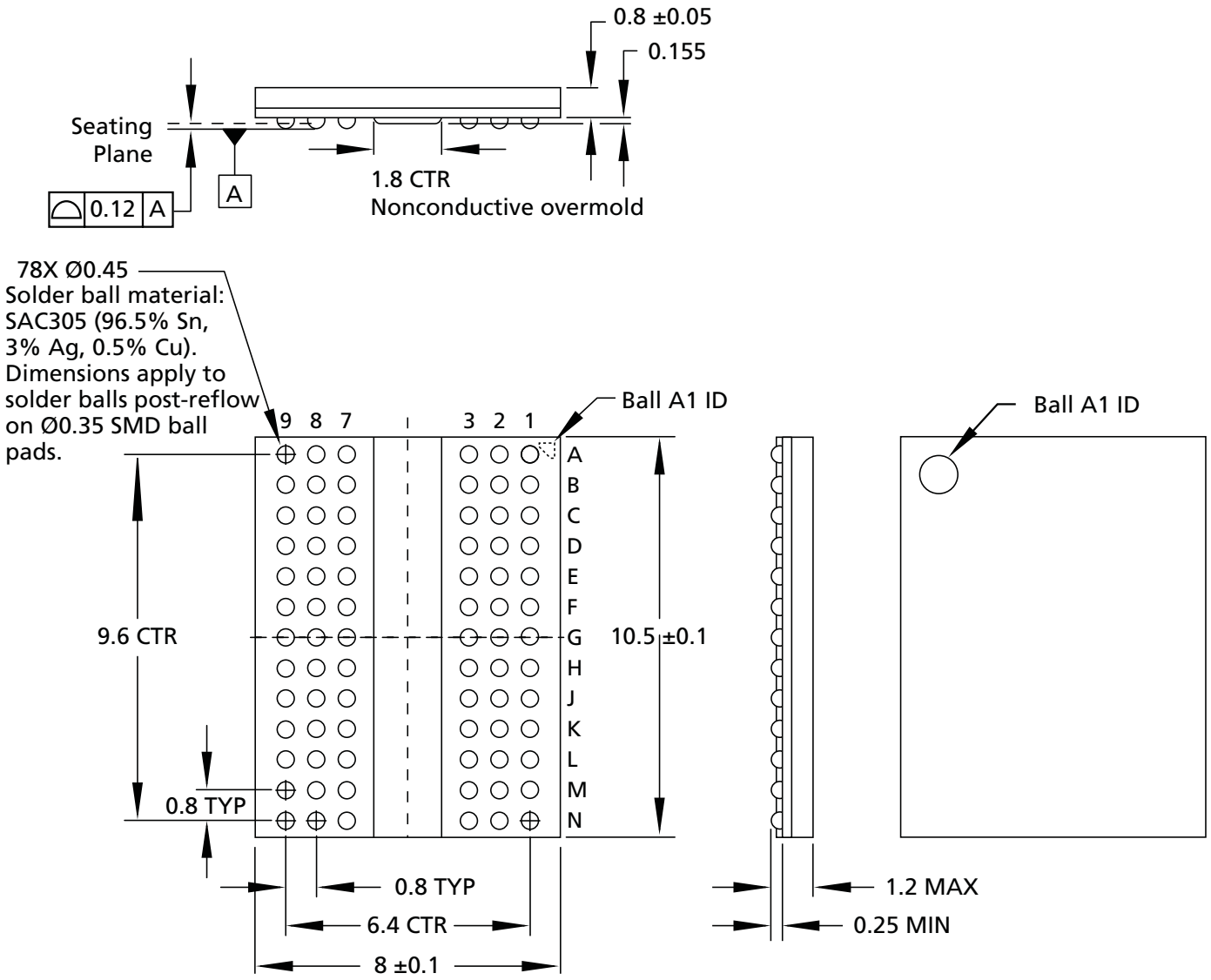
Symbol	Type	Description
A13, A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Table 71 (page 114).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.

Table 4: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to external 240Ω resistor RZQ, which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

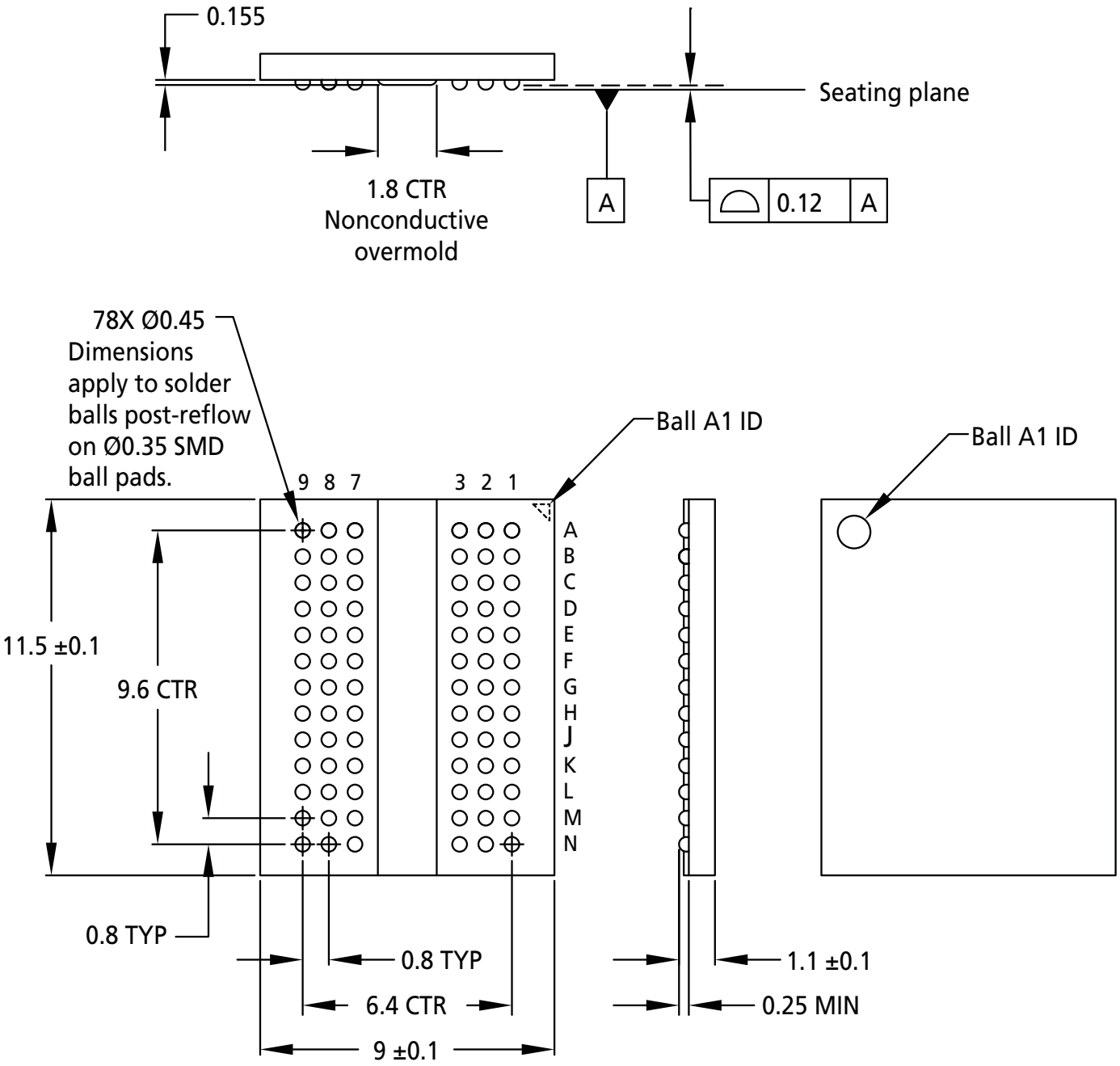
Package Dimensions

Figure 8: 78-Ball FBGA – x4, x8 (DA)



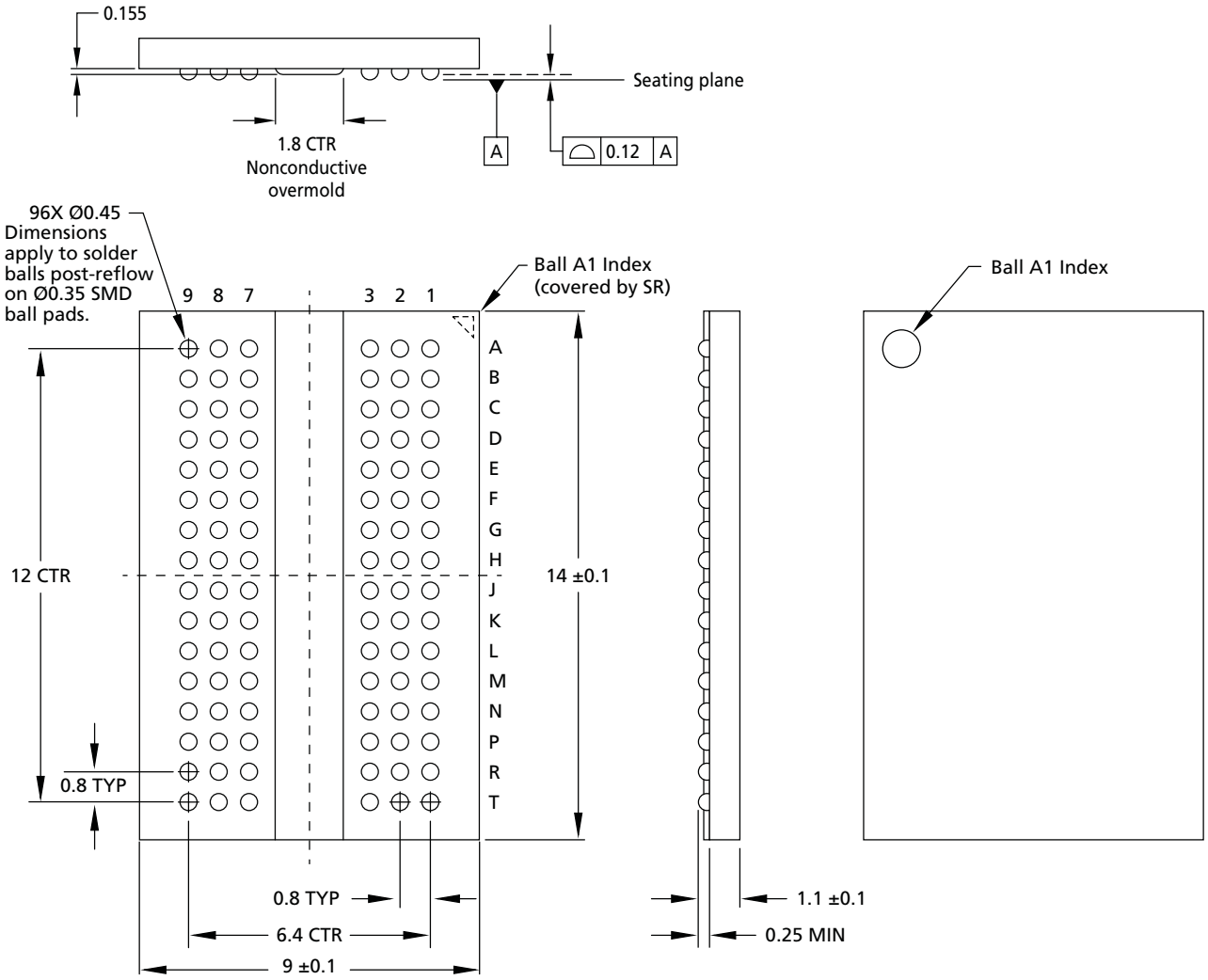
Note: 1. All dimensions are in millimeters.

Figure 9: 78-Ball FBGA – x4, x8 (HX)



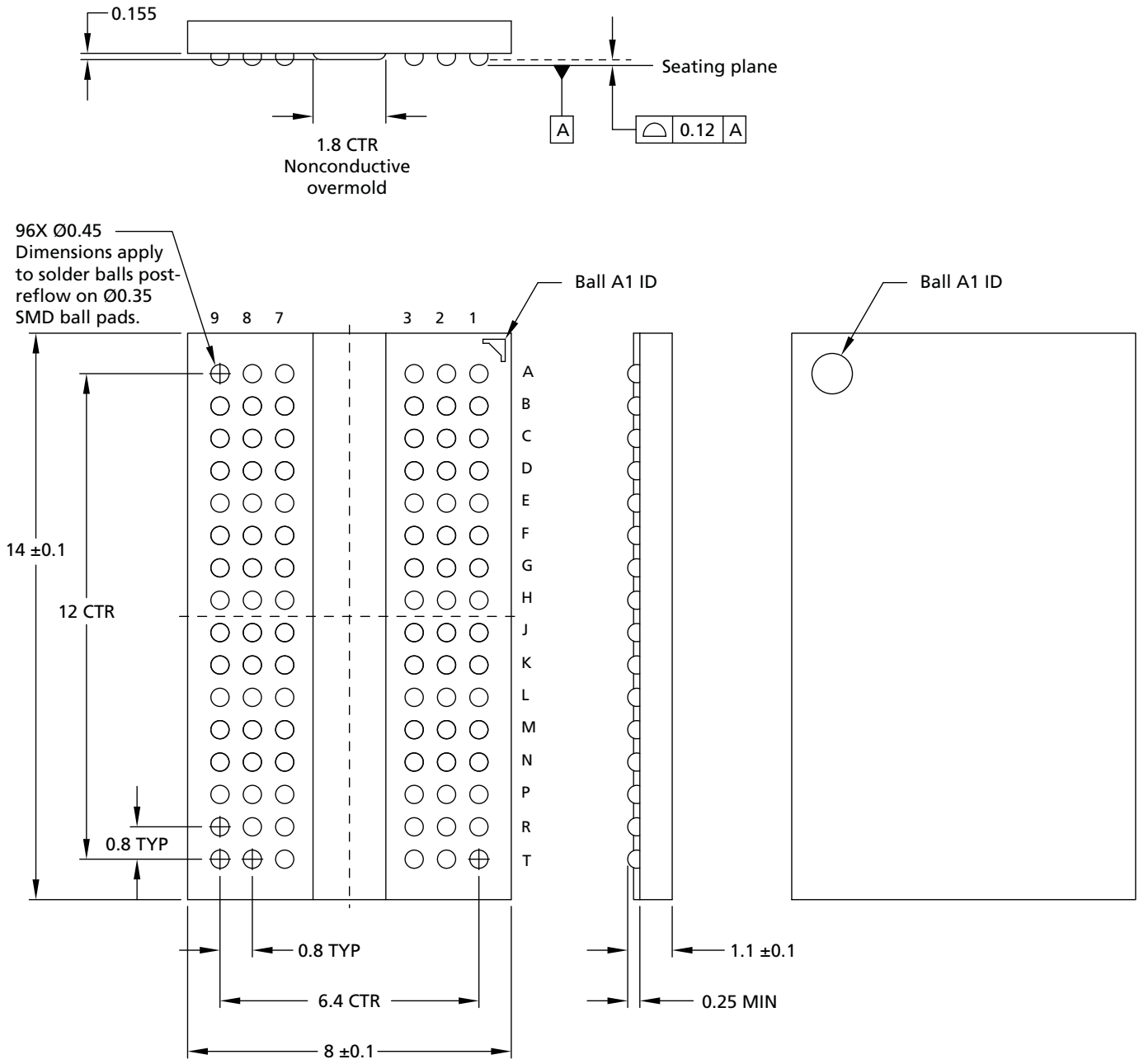
Note: 1. All dimensions are in millimeters.

Figure 10: 96-Ball FBGA – x16 (HA)



Note: 1. All dimensions are in millimeters.

Figure 11: 96-Ball FBGA – x16 (JT)



Note: 1. All dimensions are in millimeters.