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DDR3L SDRAM

MT41K256M4 – 32 Meg x 4 x 8 banks
MT41K128M8 – 16 Meg x 8 x 8 banks
MT41K64M16 – 8 Meg x 16 x 8 banks

Description

The 1.35V DDR3L SDRAM device is a low-voltage version of the 1.5V DDR3 SDRAM device. Refer to the DDR3 (1.5V) SDRAM data sheet specifications when running in 1.5V compatible mode.

Features

- $V_{DD} = V_{DDQ}$ = +1.35V (1.283V to 1.45V)
- Backward compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8192-cycle refresh at 0°C to 85°C
  - 32ms at 85°C to 95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

Options[1]	Marking
• Configuration	
– 256 Meg x 4	256M4
– 128 Meg x 8	128M8
– 64 Meg x 16	64M16
• FBGA package (Pb-free) – x4, x8	
– 78-ball FBGA (8mm x 11.5mm) Rev. G	JP
– 78-ball FBGA (8mm x 10.5mm) Rev. J	DA
• FBGA package (Pb-free) – x16	
– 96-ball FBGA (8mm x 14mm) Rev. G	JT
– 96-ball FBGA (8mm x 14mm) Rev. J	TW
• Timing – cycle time	
– 1.07ns @ CL = 13 (DDR3-1866)	-107
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.87ns @ CL = 7 (DDR3-1066)	-187E
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
• Revision	:G / :J

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-107[1, 2, 3]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
187E	1066	7-7-7	13.1	13.1	13.1

Notes: 1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).
3. Backward compatible to 1600, CL = 11 (-125).

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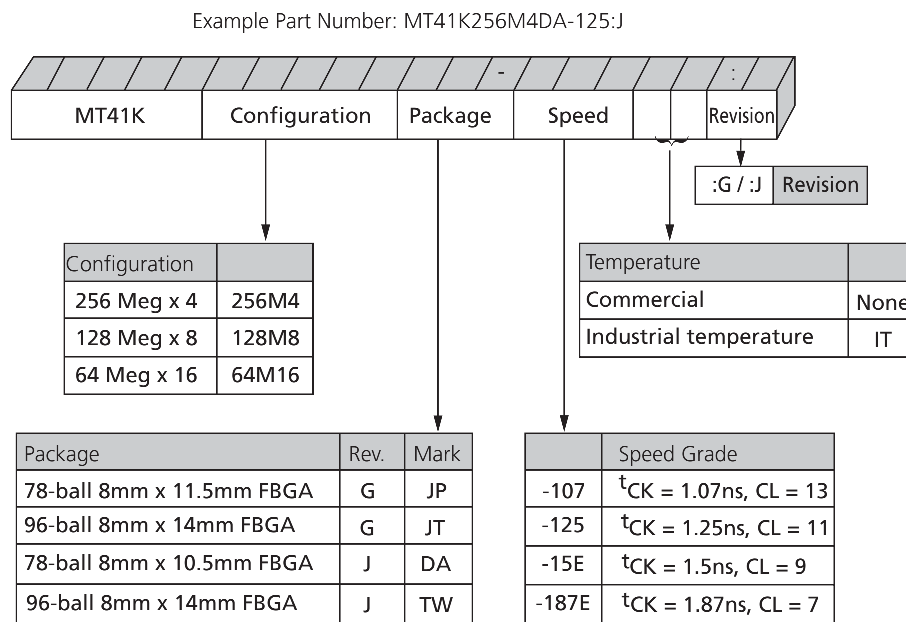
Table 2: Addressing

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	16K A[13:0]	16K A[13:0]	8K A[12:0]
Bank address	8 BA[2:0]	8 BA[2:0]	8 BA[2:0]
Column address	2K A[11, 9:0]	1K A[9:0]	1K A[9:0]
Page Size	1KB	1KB	2KB

Figure 1: DDR3 Part Numbers



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Contents

State Diagram 11
Functional Description 12
  Industrial Temperature 12
  General Notes 12
Functional Block Diagrams 14
Ball Assignments and Descriptions 16
Package Dimensions 22
Electrical Specifications 26
  Absolute Ratings 26
  Input/Output Capacitance 27
Thermal Characteristics 28
Electrical Specifications – I_{DD} Specifications and Conditions 29
Electrical Characteristics – I_{DD} Specifications 40
Electrical Specifications – DC and AC 44
  DC Operating Conditions 44
  Input Operating Conditions 45
  DDR3L 1.35V AC Overshoot/Undershoot Specification 49
  DDR3L 1.35V Slew Rate Definitions for Single-Ended Input Signals 52
  DDR3L 1.35V Slew Rate Definitions for Differential Input Signals 54
ODT Characteristics 55
  1.35V ODT Resistors 56
  ODT Sensitivity 57
  ODT Timing Definitions 57
Output Driver Impedance 61
  34 Ohm Output Driver Impedance 62
  DDR3L 34 Ohm Driver 63
  DDR3L 34 Ohm Output Driver Sensitivity 64
  DDR3L Alternative 40 Ohm Driver 65
  DDR3L 40 Ohm Output Driver Sensitivity 65
Output Characteristics and Operating Conditions 67
  Reference Output Load 70
  Slew Rate Definitions for Single-Ended Output Signals 70
  Slew Rate Definitions for Differential Output Signals 72
Speed Bin Tables 73
Electrical Characteristics and AC Operating Conditions 77
Command and Address Setup, Hold, and Derating 95
Data Setup, Hold, and Derating 102
Commands – Truth Tables 110
Commands 113
  DESELECT 113
  NO OPERATION 113
  ZQ CALIBRATION LONG 113
  ZQ CALIBRATION SHORT 113
  ACTIVATE 113
  READ 113
  WRITE 114
  PRECHARGE 115
  REFRESH 115
  SELF REFRESH 116
  DLL Disable Mode 117

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Input Clock Frequency Change 121
Write Leveling 123
Write Leveling Procedure 125
Write Leveling Mode Exit Procedure 127
Initialization 128
Voltage Initialization / Change 130
V_{DD} Voltage Switching 131
Mode Registers 132
Mode Register 0 (MR0) 133
Burst Length 133
Burst Type 134
DLL RESET 135
Write Recovery 135
Precharge Power-Down (Precharge PD) 136
CAS Latency (CL) 136
Mode Register 1 (MR1) 137
DLL Enable/DLL Disable 137
Output Drive Strength 138
OUTPUT ENABLE/DISABLE 138
TDQS Enable 138
On-Die Termination 139
WRITE LEVELING 139
POSTED CAS ADDITIVE Latency 139
Mode Register 2 (MR2) 140
CAS WRITE Latency (CWL) 141
AUTO SELF REFRESH (ASR) 141
SELF REFRESH TEMPERATURE (SRT) 142
SRT vs. ASR 142
DYNAMIC ODT 142
Mode Register 3 (MR3) 143
MULTIPURPOSE REGISTER (MPR) 143
MPR Functional Description 144
MPR Register Address Definitions and Bursting Order 145
MPR Read Predefined Pattern 151
MODE REGISTER SET (MRS) Command 151
ZQ CALIBRATION Operation 152
ACTIVATE Operation 153
READ Operation 155
WRITE Operation 166
DQ Input Timing 174
PRECHARGE Operation 176
SELF REFRESH Operation 176
Extended Temperature Usage 178
Power-Down Mode 179
RESET Operation 187
On-Die Termination (ODT) 189
Functional Representation of ODT 189
Nominal ODT 189
Dynamic ODT 191
Dynamic ODT Special Use Case 191
Functional Description 191
Synchronous ODT Mode 197

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ODT Latency and Posted ODT 197
Timing Parameters 197
ODT Off During READs 200
Asynchronous ODT Mode 202
Synchronous to Asynchronous ODT Mode Transition (Power-Down Entry) 204
Asynchronous to Synchronous ODT Mode Transition (Power-Down Exit) 206
Asynchronous to Synchronous ODT Mode Transition (Short CKE Pulse) 208

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List of Figures

Figure 1: DDR3 Part Numbers 2
Figure 2: Simplified State Diagram 11
Figure 3: 256 Meg x 4 Functional Block Diagram 14
Figure 4: 128 Meg x 8 Functional Block Diagram 15
Figure 5: 64 Meg x 16 Functional Block Diagram 15
Figure 6: 78-Ball FBGA – x4, x8 Ball Assignments (Top View) 16
Figure 7: 96-Ball FBGA – x16 Ball Assignments (Top View) 17
Figure 8: 78-Ball FBGA – x4, x8 (JP) 22
Figure 9: 78-Ball FBGA – x4, x8 (DA) 23
Figure 10: 96-Ball FBGA – x16 (JT) 24
Figure 11: 96-Ball FBGA – x16 (TW) 25
Figure 12: Thermal Measurement Point 28
Figure 13: DDR3L 1.35V Input Signal 48
Figure 14: Overshoot 49
Figure 15: Undershoot 49
Figure 16: V_{IX} for Differential Signals 50
Figure 17: Single-Ended Requirements for Differential Signals 50
Figure 18: Definition of Differential AC-Swing and ^{t}DVAC 51
Figure 19: Nominal Slew Rate Definition for Single-Ended Input Signals 53
Figure 20: DDR3L 1.35V Nominal Differential Input Slew Rate Definition for DQS, DQS# and CK, CK# 54
Figure 21: ODT Levels and I-V Characteristics 55
Figure 22: ODT Timing Reference Load 58
Figure 23: ^{t}AON and ^{t}AOF Definitions 59
Figure 24: ^{t}AONPD and ^{t}AOFPD Definitions 59
Figure 25: ^{t}ADC Definition 60
Figure 26: Output Driver 61
Figure 27: DQ Output Signal 68
Figure 28: Differential Output Signal 69
Figure 29: Reference Output Load for AC Timing and Output Slew Rate 70
Figure 30: Nominal Slew Rate Definition for Single-Ended Output Signals 71
Figure 31: Nominal Differential Output Slew Rate Definition for DQS, DQS# 72
Figure 32: Nominal Slew Rate and ^{t}VAC for ^{t}IS (Command and Address – Clock) 98
Figure 33: Nominal Slew Rate for ^{t}IH (Command and Address – Clock) 99
Figure 34: Tangent Line for ^{t}IS (Command and Address – Clock) 100
Figure 35: Tangent Line for ^{t}IH (Command and Address – Clock) 101
Figure 36: Nominal Slew Rate and ^{t}VAC for ^{t}DS (DQ – Strobe) 106
Figure 37: Nominal Slew Rate for ^{t}DH (DQ – Strobe) 107
Figure 38: Tangent Line for ^{t}DS (DQ – Strobe) 108
Figure 39: Tangent Line for ^{t}DH (DQ – Strobe) 109
Figure 40: Refresh Mode 116
Figure 41: DLL Enable Mode to DLL Disable Mode 118
Figure 42: DLL Disable Mode to DLL Enable Mode 119
Figure 43: DLL Disable ^{t}DQSCK 120
Figure 44: Change Frequency During Precharge Power-Down 122
Figure 45: Write Leveling Concept 123
Figure 46: Write Leveling Sequence 126
Figure 47: Write Leveling Exit Procedure 127
Figure 48: Initialization Sequence 129
Figure 49: V_{DD} Voltage Switching 131
Figure 50: MRS to MRS Command Timing (^{t}MRD) 132

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Figure 51: MRS to nonMRS Command Timing (^{t}MOD) ... 133
Figure 52: Mode Register 0 (MR0) Definitions ... 134
Figure 53: READ Latency ... 136
Figure 54: Mode Register 1 (MR1) Definition ... 137
Figure 55: READ Latency (AL = 5, CL = 6) ... 140
Figure 56: Mode Register 2 (MR2) Definition ... 141
Figure 57: CAS WRITE Latency ... 141
Figure 58: Mode Register 3 (MR3) Definition ... 143
Figure 59: Multipurpose Register (MPR) Block Diagram ... 144
Figure 60: MPR System Read Calibration with BL8: Fixed Burst Order Single Readout ... 147
Figure 61: MPR System Read Calibration with BL8: Fixed Burst Order, Back-to-Back Readout ... 148
Figure 62: MPR System Read Calibration with BC4: Lower Nibble, Then Upper Nibble ... 149
Figure 63: MPR System Read Calibration with BC4: Upper Nibble, Then Lower Nibble ... 150
Figure 64: ZQ CALIBRATION Timing (ZQCL and ZQCS) ... 152
Figure 65: Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN) ... 153
Figure 66: Example: ^{t}FAW ... 154
Figure 67: READ Latency ... 155
Figure 68: Consecutive READ Bursts (BL8) ... 157
Figure 69: Consecutive READ Bursts (BC4) ... 157
Figure 70: Nonconsecutive READ Bursts ... 158
Figure 71: READ (BL8) to WRITE (BL8) ... 158
Figure 72: READ (BC4) to WRITE (BC4) OTF ... 159
Figure 73: READ to PRECHARGE (BL8) ... 159
Figure 74: READ to PRECHARGE (BC4) ... 160
Figure 75: READ to PRECHARGE (AL = 5, CL = 6) ... 160
Figure 76: READ with Auto Precharge (AL = 4, CL = 6) ... 160
Figure 77: Data Output Timing – ^{t}DQSQ and Data Valid Window ... 162
Figure 78: Data Strobe Timing – READs ... 163
Figure 79: Method for Calculating ^{t}LZ and ^{t}HZ ... 164
Figure 80: ^{t}RPRE Timing ... 164
Figure 81: ^{t}RPST Timing ... 165
Figure 82: ^{t}WPRE Timing ... 167
Figure 83: ^{t}WPST Timing ... 167
Figure 84: WRITE Burst ... 168
Figure 85: Consecutive WRITE (BL8) to WRITE (BL8) ... 169
Figure 86: Consecutive WRITE (BC4) to WRITE (BC4) via OTF ... 169
Figure 87: Nonconsecutive WRITE to WRITE ... 170
Figure 88: WRITE (BL8) to READ (BL8) ... 170
Figure 89: WRITE to READ (BC4 Mode Register Setting) ... 171
Figure 90: WRITE (BC4 OTF) to READ (BC4 OTF) ... 172
Figure 91: WRITE (BL8) to PRECHARGE ... 173
Figure 92: WRITE (BC4 Mode Register Setting) to PRECHARGE ... 173
Figure 93: WRITE (BC4 OTF) to PRECHARGE ... 174
Figure 94: Data Input Timing ... 175
Figure 95: Self Refresh Entry/Exit Timing ... 177
Figure 96: Active Power-Down Entry and Exit ... 181
Figure 97: Precharge Power-Down (Fast-Exit Mode) Entry and Exit ... 181
Figure 98: Precharge Power-Down (Slow-Exit Mode) Entry and Exit ... 182
Figure 99: Power-Down Entry After READ or READ with Auto Precharge (RDAP) ... 182
Figure 100: Power-Down Entry After WRITE ... 183
Figure 101: Power-Down Entry After WRITE with Auto Precharge (WRAP) ... 183
Figure 102: REFRESH to Power-Down Entry ... 184

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Figure 103: ACTIVATE to Power-Down Entry 184
Figure 104: PRECHARGE to Power-Down Entry 185
Figure 105: MRS Command to Power-Down Entry 185
Figure 106: Power-Down Exit to Refresh to Power-Down Entry 186
Figure 107: RESET Sequence 188
Figure 108: On-Die Termination 189
Figure 109: Dynamic ODT: ODT Asserted Before and After the WRITE, BC4 194
Figure 110: Dynamic ODT: Without WRITE Command 194
Figure 111: Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8 195
Figure 112: Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4 196
Figure 113: Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4 196
Figure 114: Synchronous ODT 198
Figure 115: Synchronous ODT (BC4) 199
Figure 116: ODT During READs 201
Figure 117: Asynchronous ODT Timing with Fast ODT Transition 203
Figure 118: Synchronous to Asynchronous Transition During Precharge Power-Down (DLL Off) Entry 205
Figure 119: Asynchronous to Synchronous Transition During Precharge Power-Down (DLL Off) Exit 207
Figure 120: Transition Period for Short CKE LOW Cycles with Entry and Exit Period Overlapping 209
Figure 121: Transition Period for Short CKE HIGH Cycles with Entry and Exit Period Overlapping 209

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List of Tables

Table 1: Key Timing Parameters 1
Table 2: Addressing 2
Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions 18
Table 4: 96-Ball FBGA – x16 Ball Descriptions 20
Table 5: Absolute Maximum Ratings 26
Table 6: DDR3L Input/Output Capacitance 27
Table 7: Thermal Characteristics 28
Table 8: DDR3L Timing Parameters Used for I_{DD} Measurements – Clock Units 29
Table 9: DDR3L I_{DD0} Measurement Loop 30
Table 10: DDR3L I_{DD1} Measurement Loop 31
Table 11: DDR3L I_{DD} Measurement Conditions for Power-Down Currents 32
Table 12: DDR3L I_{DD2N} and I_{DD3N} Measurement Loop 33
Table 13: DDR3L I_{DD2NT} Measurement Loop 33
Table 14: DDR3L I_{DD4R} Measurement Loop 34
Table 15: DDR3L I_{DD4W} Measurement Loop 35
Table 16: DDR3L I_{DD5B} Measurement Loop 36
Table 17: DDR3L I_{DD} Measurement Conditions for I_{DD6}, I_{DD6ET}, and I_{DD8} 37
Table 18: DDR3L I_{DD7} Measurement Loop 38
Table 19: I_{DD} Maximum Limits – Rev. G 40
Table 20: I_{DD} Maximum Limits – Rev. J 42
Table 21: DDR3L 1.35V DC Electrical Characteristics and Operating Conditions 44
Table 22: DDR3L 1.35V DC Electrical Characteristics and Input Conditions 45
Table 23: DDR3L 1.35V Input Switching Conditions - Command and Address 46
Table 24: DDR3L 1.35V Differential Input Operating Conditions (CK, CK# and DQS, DQS#) 47
Table 25: DDR3L Control and Address Pins 49
Table 26: DDR3L 1.35V Clock, Data, Strobe, and Mask Pins 49
Table 27: DDR3L 1.35V - Minimum Required Time ^{t}DVAC for CK/CK#, DQS/DQS# Differential for AC Ringback .51
Table 28: Single-Ended Input Slew Rate Definition 52
Table 29: DDR3L 1.35V Differential Input Slew Rate Definition 54
Table 30: On-Die Termination DC Electrical Characteristics 55
Table 31: 1.35V R_{TT} Effective Impedance 56
Table 32: ODT Sensitivity Definition 57
Table 33: ODT Temperature and Voltage Sensitivity 57
Table 34: ODT Timing Definitions 58
Table 35: DDR3L(1.35V) Reference Settings for ODT Timing Measurements 58
Table 36: DDR3L 34 Ohm Driver Impedance Characteristics 62
Table 37: DDR3L 34 Ohm Driver Pull-Up and Pull-Down Impedance Calculations 63
Table 38: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ}$ = DDR3L@1.35V 63
Table 39: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ}$ = DDR3L@1.45V 63
Table 40: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ}$ = DDR3L@1.283 64
Table 41: DDR3L 34 Ohm Output Driver Sensitivity Definition 64
Table 42: DDR3L 34 Ohm Output Driver Voltage and Temperature Sensitivity 64
Table 43: DDR3L 40 Ohm Driver Impedance Characteristics 65
Table 44: DDR3L 40 Ohm Output Driver Sensitivity Definition 65
Table 45: 40 Ohm Output Driver Voltage and Temperature Sensitivity 66
Table 46: DDR3L Single-Ended Output Driver Characteristics 67
Table 47: DDR3L Differential Output Driver Characteristics 68
Table 48: DDR3L Differential Output Driver Characteristics $V_{OX(AC)}$ 69
Table 49: Single-Ended Output Slew Rate Definition 70
Table 50: Differential Output Slew Rate Definition 72

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Table 51: DDR3L-1066 Speed Bins 73
Table 52: DDR3L-1333 Speed Bins 74
Table 53: DDR3L-1600 Speed Bins 75
Table 54: DDR3L-1866 Speed Bins 76
Table 55: Electrical Characteristics and AC Operating Conditions 77
Table 56: Electrical Characteristics and AC Operating Conditions for Speed Extensions 87
Table 57: DDR3L Command and Address Setup and Hold Values 1 V/ns Referenced – AC/DC-Based 96
Table 58: DDR3L-800/1066/1333/1600 Derating Values ^{t}IS/^{t}IH – AC160/DC90-Based 96
Table 59: DDR3L-800/1066/1333/1600 Derating Values for ^{t}IS/^{t}IH – AC135/DC90-Based 96
Table 60: DDR3L-1866 Derating Values for ^{t}IS/^{t}IH – AC125/DC90-Based 97
Table 61: DDR3L Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL[AC]}$) for Valid ADD/CMD Transition .. 97
Table 62: DDR3L Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based 103
Table 63: DDR3L Derating Values for ^{t}DS/^{t}DH – AC160/DC90-Based 103
Table 64: DDR3L Derating Values for ^{t}DS/^{t}DH – AC135/DC100-Based 103
Table 65: DDR3L Derating Values for ^{t}DS/^{t}DH – AC130/DC100-Based at 2V/ns 104
Table 66: DDR3L Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQ Transition 105
Table 67: Truth Table – Command 110
Table 68: Truth Table – CKE 112
Table 69: READ Command Summary 114
Table 70: WRITE Command Summary 114
Table 71: READ Electrical Characteristics, DLL Disable Mode 120
Table 72: Write Leveling Matrix 124
Table 73: Burst Order 135
Table 74: MPR Functional Description of MR3 Bits 144
Table 75: MPR Readouts and Burst Order Bit Mapping 145
Table 76: Self Refresh Temperature and Auto Self Refresh Description 178
Table 77: Self Refresh Mode Summary 178
Table 78: Command to Power-Down Entry Parameters 179
Table 79: Power-Down Modes 180
Table 80: Truth Table – ODT (Nominal) 190
Table 81: ODT Parameters 190
Table 82: Write Leveling with Dynamic ODT Special Case 191
Table 83: Dynamic ODT Specific Parameters 192
Table 84: Mode Registers for $R_{TT,nom}$ 192
Table 85: Mode Registers for $R_{TT(WR)}$ 193
Table 86: Timing Diagrams for Dynamic ODT 193
Table 87: Synchronous ODT Parameters 198
Table 88: Asynchronous ODT Timing Parameters for All Speed Bins 203
Table 89: ODT Parameters for Power-Down (DLL Off) Entry and Exit Transition Period 205

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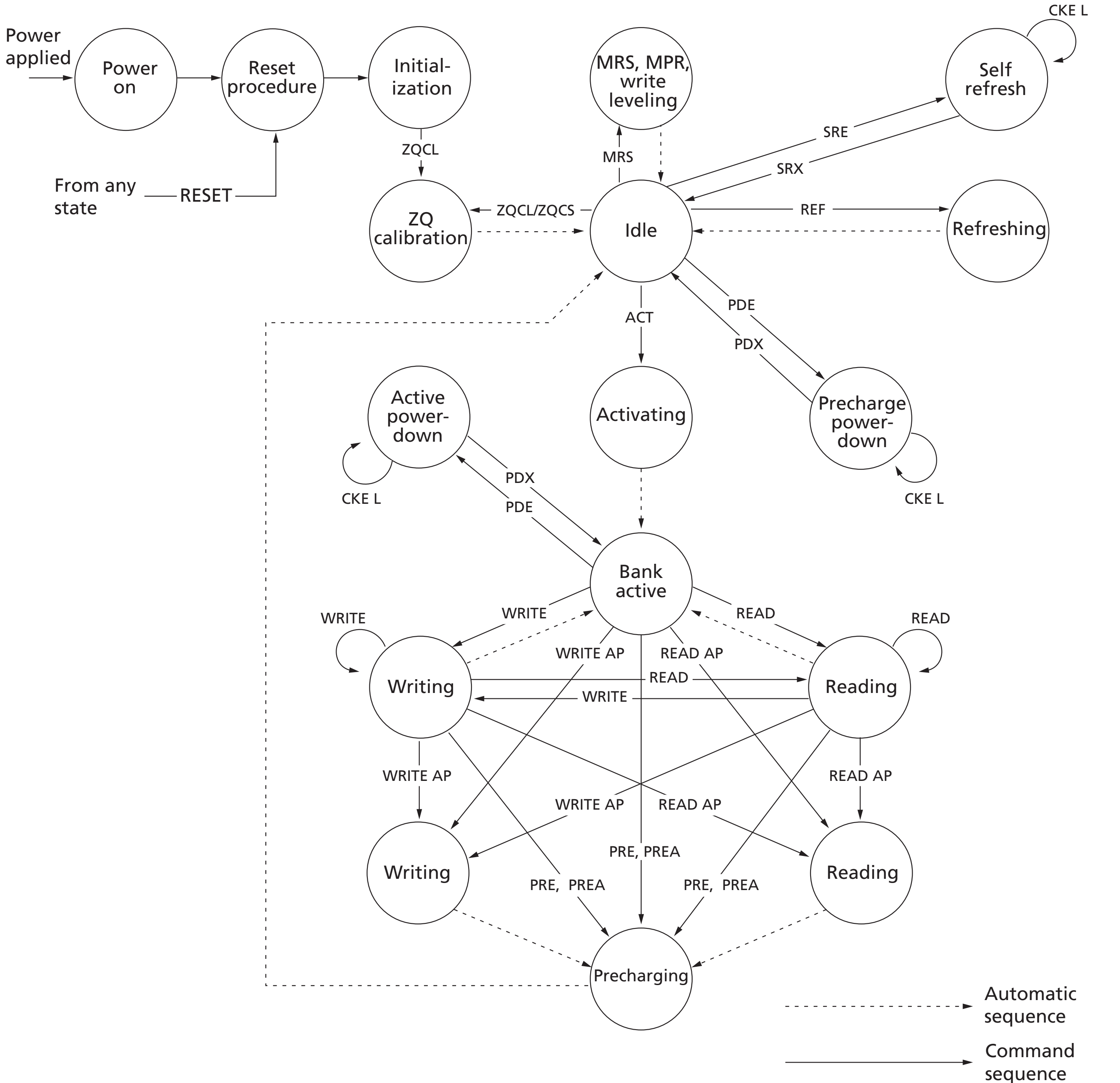
State Diagram

Figure 2: Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

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Functional Description

DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Industrial Temperature

The industrial temperature (IT) device requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is < 0°C or >95°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout this data sheet, various figures and text refer to DQs as "DQ." DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "DQS" and "CK" found throughout this data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.

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- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Row addressing is denoted as A[n:0]. *For example,* 1Gb: n = 12 (x16); 1Gb: n = 13 (x4, x8); 2Gb: n = 13 (x16) and 2Gb: n = 14 (x4, x8); 4Gb: n = 14 (x16); and 4Gb: n = 15 (x4, x8).
- Dynamic ODT has a special use case: when DDR3 devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed. Refer to the Dynamic ODT Special Use Case section.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
  - Connect UDQS to ground via 1kΩ* resistor.
  - Connect UDQS# to V_{DD} via 1kΩ* resistor.
  - Connect UDM to V_{DD} via 1kΩ* resistor.
  - Connect DQ[15:8] individually to either V_{SS}, V_{DD}, or V_{REF} via 1kΩ resistors,* or float DQ[15:8].

  *If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.

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Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

Figure 3: 256 Meg x 4 Functional Block Diagram

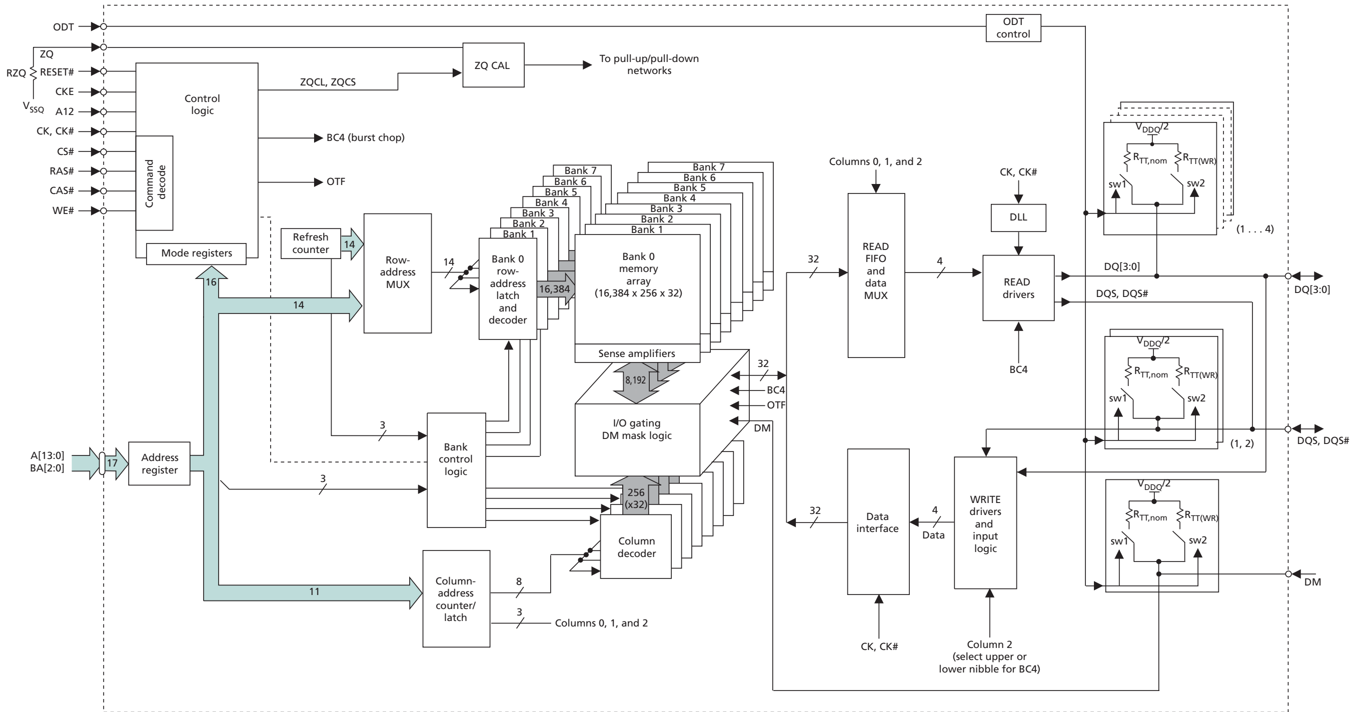

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Figure 4: 128 Meg x 8 Functional Block Diagram

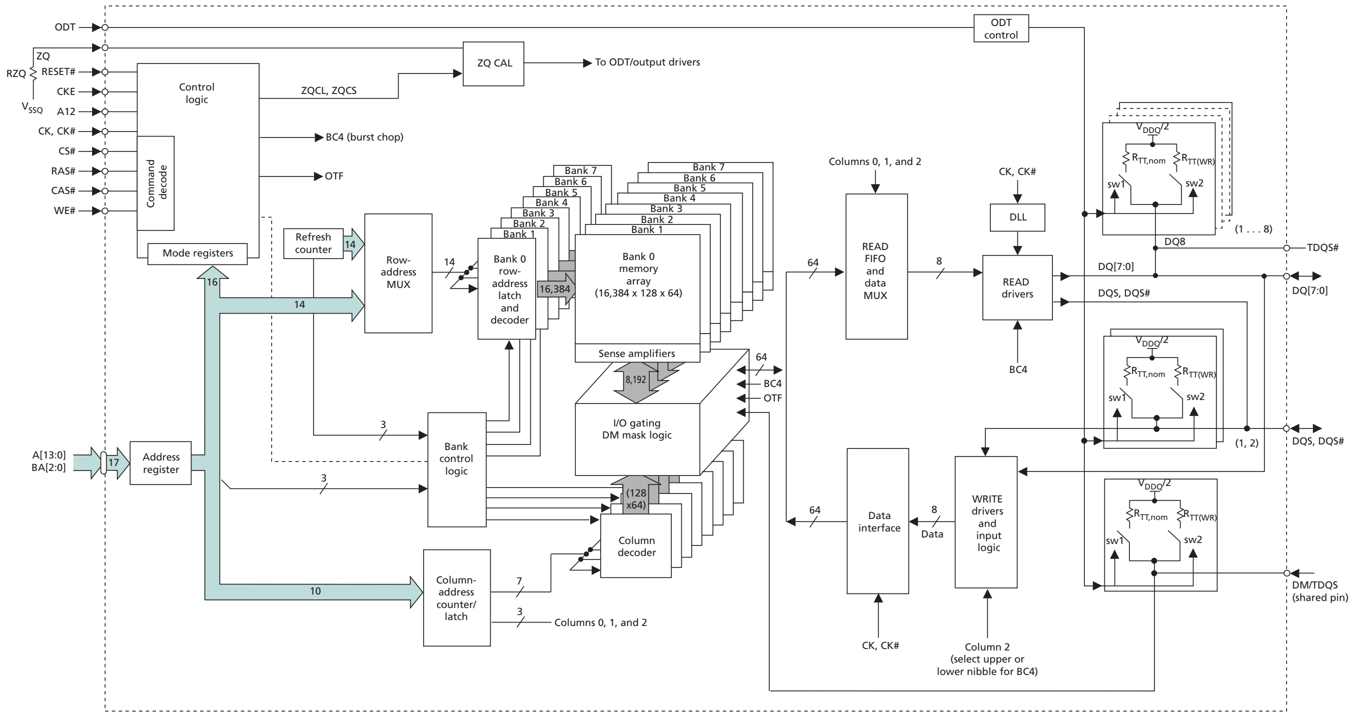
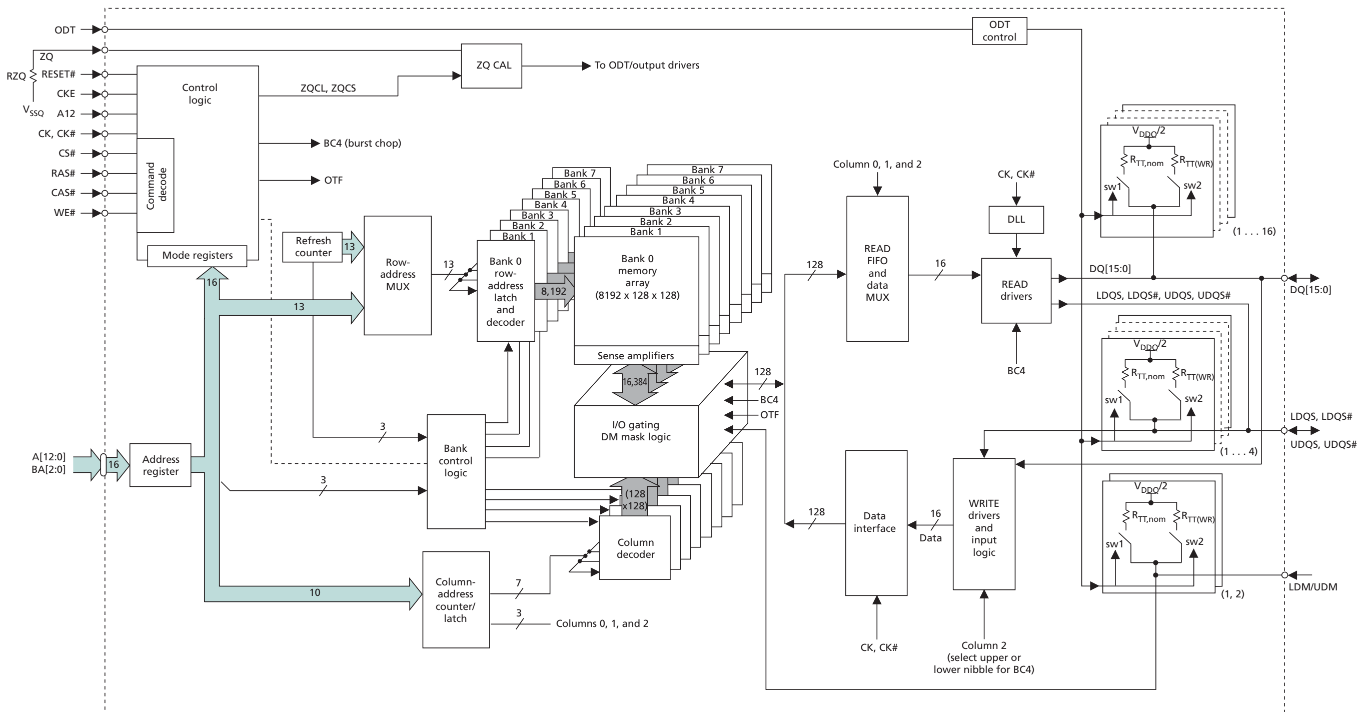


Figure 5: 64 Meg x 16 Functional Block Diagram



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Ball Assignments and Descriptions

Figure 6: 78-Ball FBGA – x4, x8 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DD}	NC				NF, NF/TDQS#	V_{SS}	V_{DD}
B	V_{SS}	V_{SSQ}	DQ0				DM, DM/TDQS	V_{SSQ}	V_{DDQ}
C	V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}
D	V_{SSQ}	NF, DQ6	DQS#				V_{DD}	V_{SS}	V_{SSQ}
E	V_{REFDQ}	V_{DDQ}	NF, DQ4				NF, DQ7	NF, DQ5	V_{DDQ}
F	NC	V_{SS}	RAS#				CK	V_{SS}	NC
G	ODT	V_{DD}	CAS#				CK#	V_{DD}	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}
K	V_{DD}	A3	A0				A12/BC#	BA1	V_{DD}
L	V_{SS}	A5	A2				A1	A4	V_{SS}
M	V_{DD}	A7	A9				A11	A6	V_{DD}
N	V_{SS}	RESET#	A13				NC	A8	V_{SS}

Notes:
1. Ball descriptions listed in Table 3 (page 18) are listed as x4, x8 if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function.
   Example: D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

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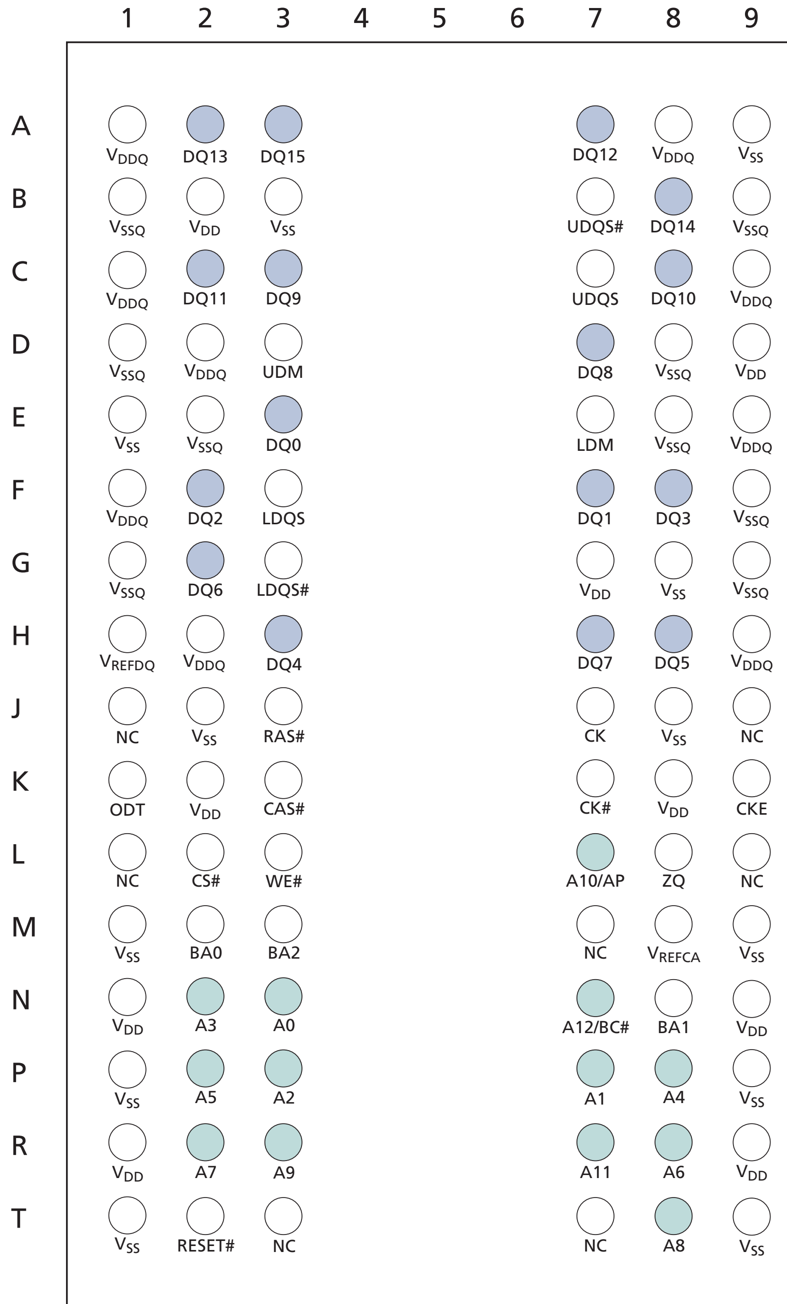
Figure 7: 96-Ball FBGA – x16 Ball Assignments (Top View)



Notes: 1. Ball descriptions listed in Table 3 (page 18) are listed as x16.
2. A comma separates the configuration; a slash defines a selectable function.

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Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Symbol	Type	Description
A[9:0], A10/AP, A11, A12/BC#, A13	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: when enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. DM has an optional use as TDQS on the x8 device.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to V_{REFDQ}.

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Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	I/O	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	**Power supply:** 1.35V, 1.283V to 1.45V operational; compatible with 1.5V operation.
V_{DDQ}	Supply	**DQ power supply:** 1.35V, 1.283V to 1.45V operational; compatible with 1.5V operation.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

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Table 4: 96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
A[9:0], A10/AP, A11, A12/BC#	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: when enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.

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Table 4: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.35V, 1.283V to 1.45V.
V_{DDQ}	Supply	**DQ power supply:** 1.35V, 1.283V to 1.45V.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

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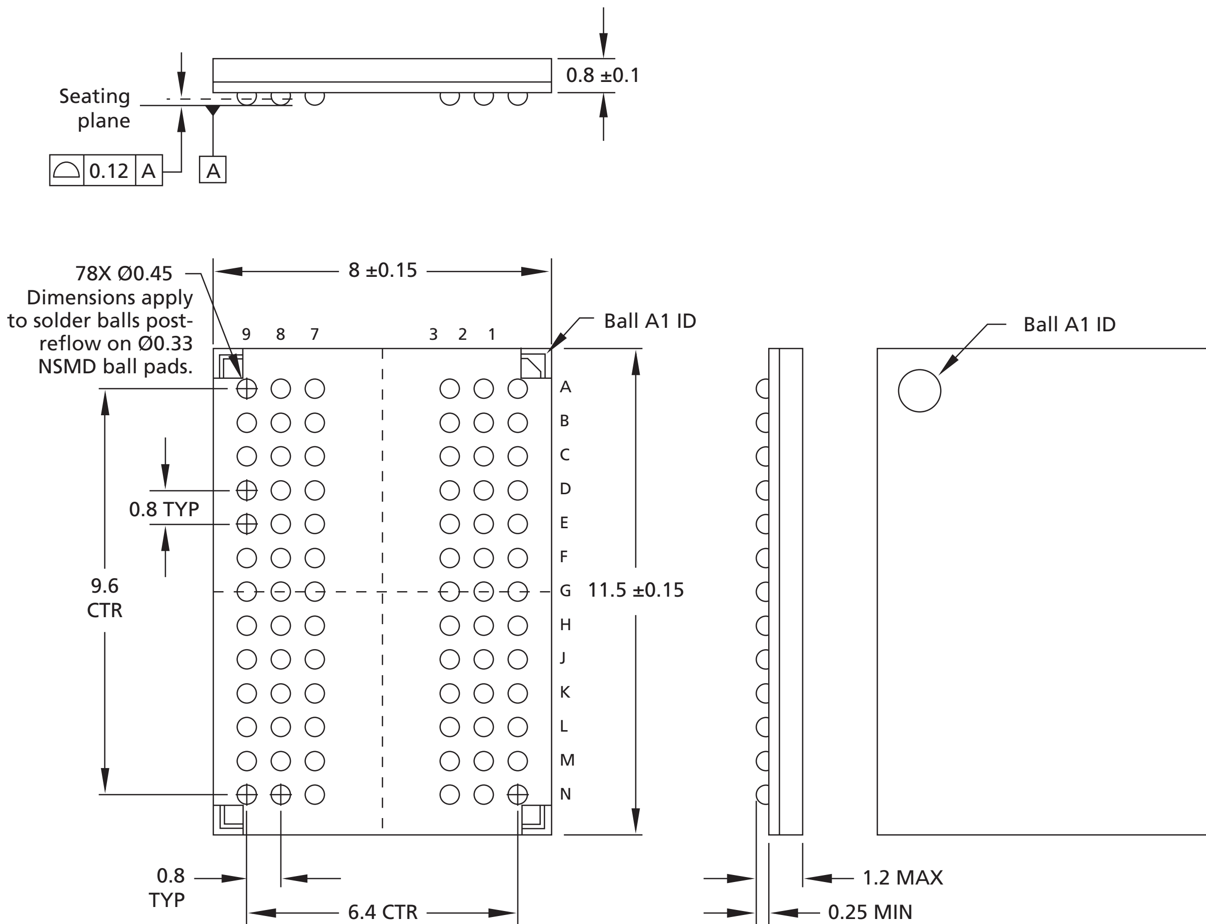
Package Dimensions

Figure 8: 78-Ball FBGA – x4, x8 (JP)



Notes: 1. All dimensions are in millimeters.
2. Material composition: Pb-free SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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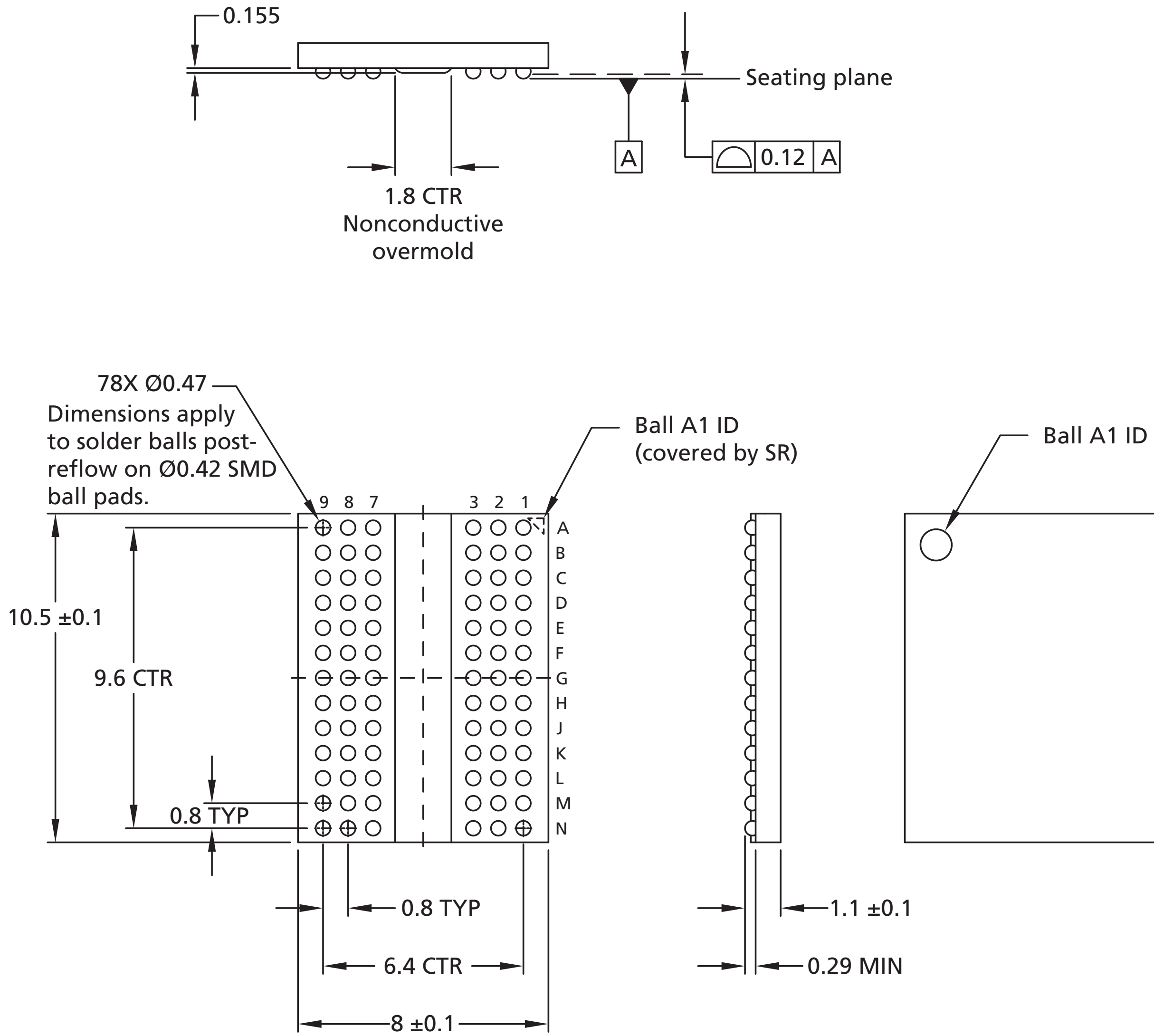
Figure 9: 78-Ball FBGA – x4, x8 (DA)



Notes: 1. All dimensions are in millimeters.
2. Material composition: Pb-free SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

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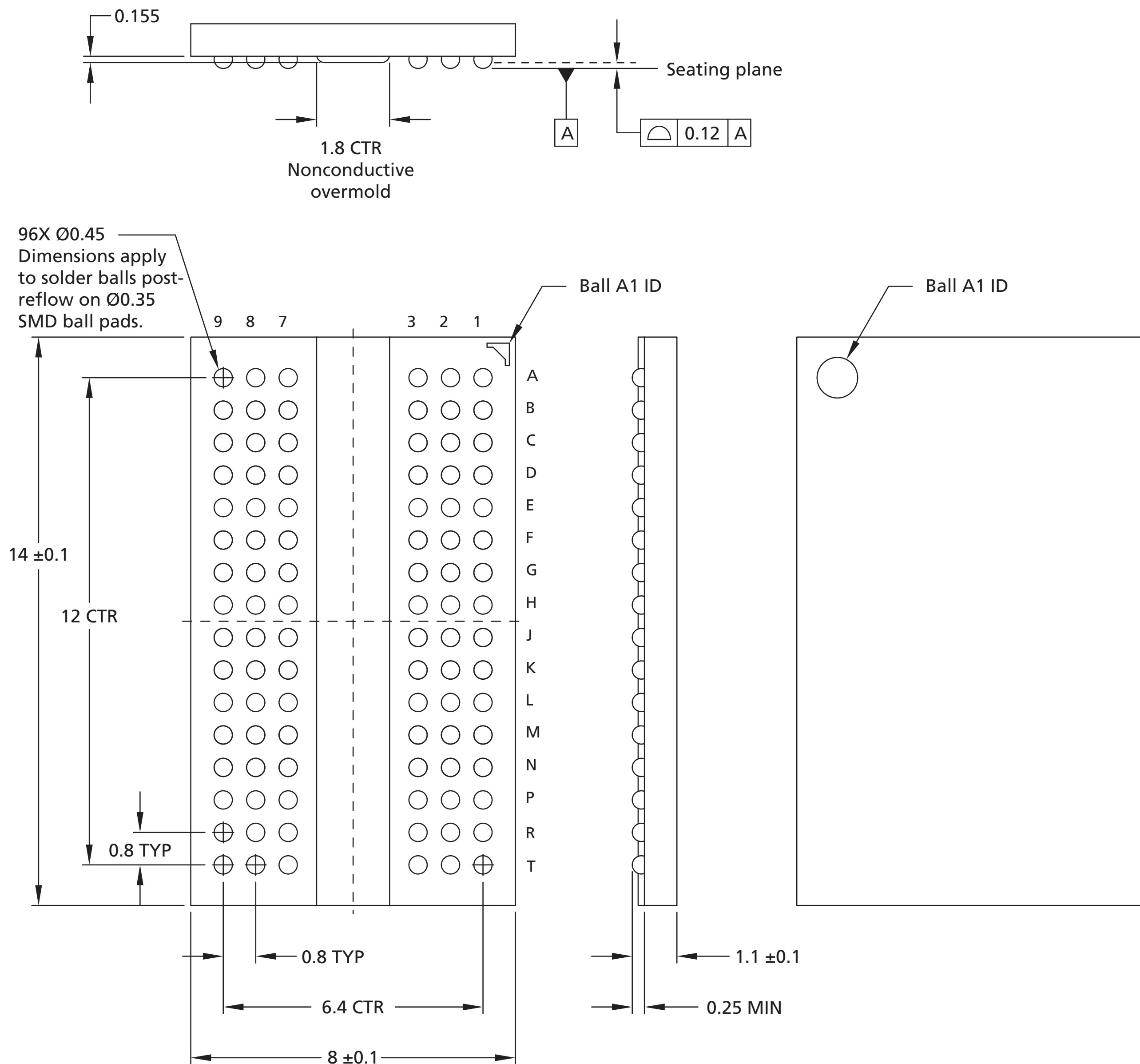
Figure 10: 96-Ball FBGA – x16 (JT)



Notes:
1. All dimensions are in millimeters.
2. Material composition: Pb-free SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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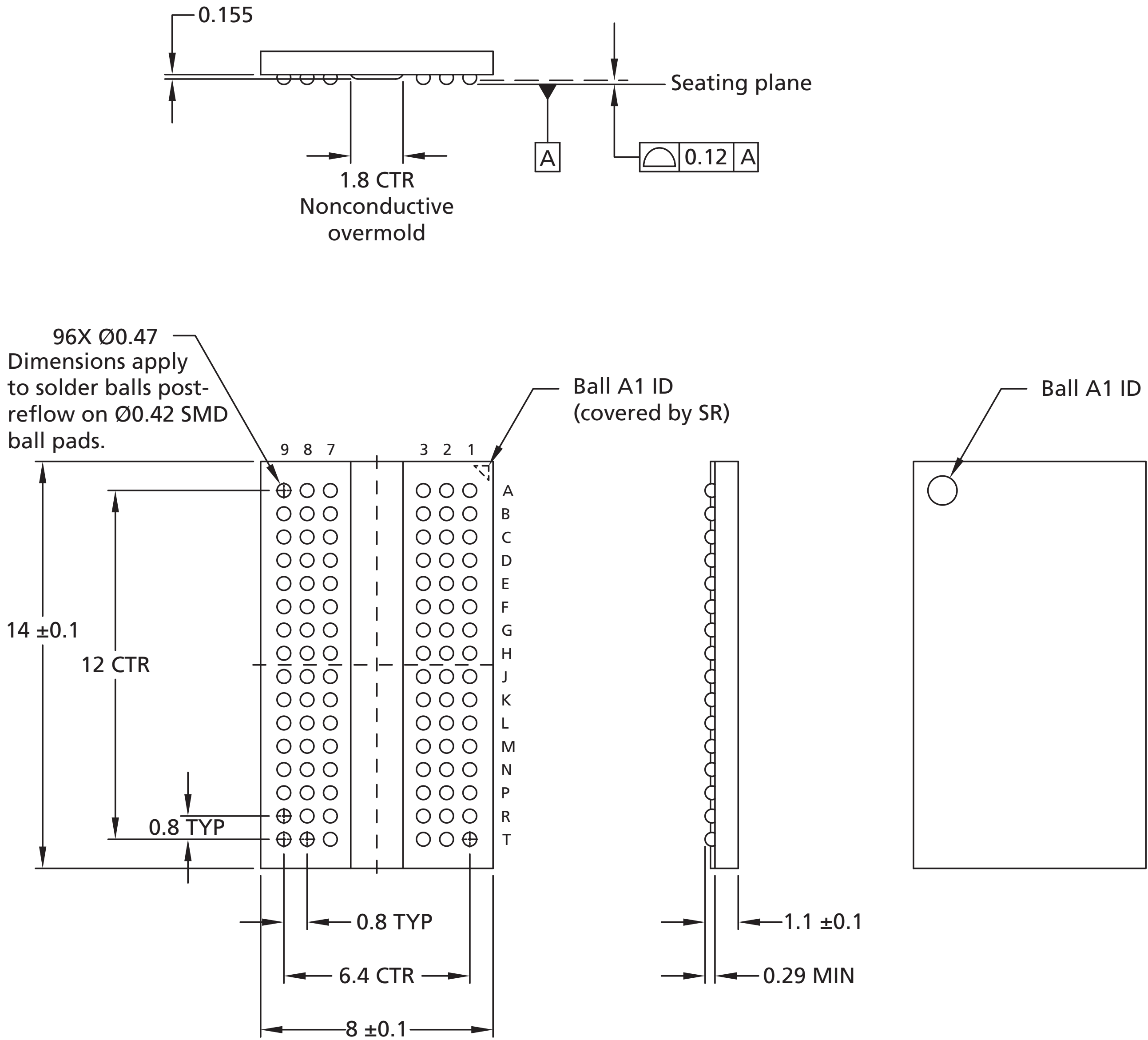
Figure 11: 96-Ball FBGA – x16 (TW)



Notes:
1. All dimensions are in millimeters.
2. Material composition: Pb-free SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

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