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Automotive DDR3L SDRAM

MT41K512M8 – 64 Meg x 8 x 8 banks
MT41K256M16 – 32 Meg x 16 x 8 banks

Description

DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 (1.5V) SDRAM. Refer to DDR3 (1.5V) SDRAM (Die Rev :E) data sheet specifications when running in 1.5V compatible mode.

Features

- $V_{DD} = V_{DDQ}$ = 1.35V (1.283–1.45V)
- Backward compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
  - Supports DDR3L devices to be backward compatible in 1.5V applications
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of -40°C to +125°C
  - 64ms, 8192-cycle refresh at 0°C to +85°C
  - 32ms at +85°C to +95°C
  - 16ms at +95°C to +105°C
  - 8ms at +105°C to +125°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration
- AEC-Q100
- PPAP submission
- 8D response time

Options	Marking
• Configuration	
– 512 Meg x 8	512M8
– 256 Meg x 16	256M16
• FBGA package (Pb-free) – x8	
– 78-ball (8mm x 10.5mm)	DA
• FBGA package (Pb-free) – x16	
– 96-ball (8mm x 14mm)	TW
• Timing – cycle time	
– 1.07ns @ CL = 13 (DDR3-1866)	-107
• Product certification	
– Automotive	A
• Operating temperature	
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
– Automotive (–40°C ≤ T_C ≤ +105°C)	AT
– Ultra-high (–40°C ≤ T_C ≤ +125°C)[3]	UT
• Revision	:P

Note:

1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

2. The datasheet does not support ×4 mode even though ×4 mode description exists in the following sections.

3. The UT option use based on automotive usage model. Please contact Micron sales representative if you have questions.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^tRCD-^tRP-CL	^tRCD (ns)	^tRP (ns)	CL (ns)
-107	1866	13-13-13	13.91	13.91	13.91

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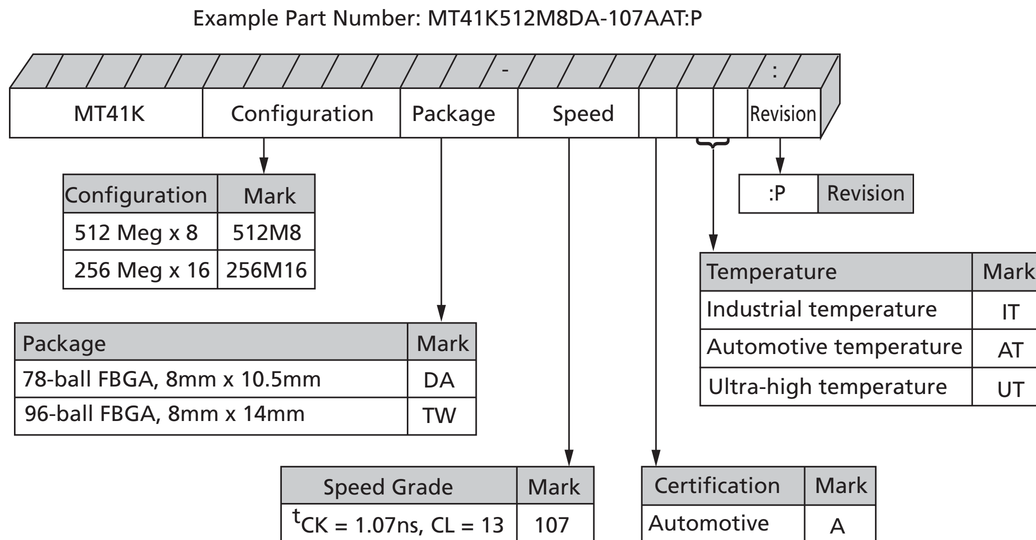
Table 2: Addressing

Parameter	512 Meg x 8	256 Meg x 16
Configuration	64 Meg x 8 x 8 banks	32 Meg x 16 x 8 banks
Refresh count	8K	8K
Row address	64K (A[15:0])	32K (A[14:0])
Bank address	8 (BA[2:0])	8 (BA[2:0])
Column address	1K (A[9:0])	1K (A[9:0])
Page size	1KB	2KB

Figure 1: DDR3L Part Numbers



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

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Contents

State Diagram 11
Functional Description 12
Industrial Temperature 12
Automotive Temperature 12
Utra-high Temperature 13
General Notes 13
Functional Block Diagrams 14
Ball Assignments and Descriptions 16
Package Dimensions 22
Electrical Specifications 24
Absolute Ratings 24
Input/Output Capacitance 25
Thermal Characteristics 26
Electrical Specifications – I_{DD} Specifications and Conditions 28
Electrical Characteristics – Operating I_{DD} Specifications 39
Electrical Specifications – DC and AC 41
DC Operating Conditions 41
Input Operating Conditions 42
DDR3L 1.35V AC Overshoot/Undershoot Specification 46
DDR3L 1.35V Slew Rate Definitions for Single-Ended Input Signals 49
DDR3L 1.35V Slew Rate Definitions for Differential Input Signals 51
ODT Characteristics 52
1.35V ODT Resistors 53
ODT Sensitivity 54
ODT Timing Definitions 54
Output Driver Impedance 58
34 Ohm Output Driver Impedance 59
DDR3L 34 Ohm Driver 60
DDR3L 34 Ohm Output Driver Sensitivity 61
DDR3L Alternative 40 Ohm Driver 62
DDR3L 40 Ohm Output Driver Sensitivity 62
Output Characteristics and Operating Conditions 64
Reference Output Load 67
Slew Rate Definitions for Single-Ended Output Signals 67
Slew Rate Definitions for Differential Output Signals 69
Speed Bin Tables 70
Electrical Characteristics and AC Operating Conditions 75
Command and Address Setup, Hold, and Derating 84
Data Setup, Hold, and Derating 91
Commands – Truth Tables 99
Commands 102
DESELECT 102
NO OPERATION 102
ZQ CALIBRATION LONG 102
ZQ CALIBRATION SHORT 102
ACTIVATE 102
READ 102
WRITE 103
PRECHARGE 104
REFRESH 104

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SELF REFRESH ... 105
DLL Disable Mode ... 106
Input Clock Frequency Change ... 110
Write Leveling ... 112
Write Leveling Procedure ... 114
Write Leveling Mode Exit Procedure ... 116
Initialization ... 117
Voltage Initialization / Change ... 119
V_{DD} Voltage Switching ... 120
Mode Registers ... 121
Mode Register 0 (MR0) ... 122
Burst Length ... 122
Burst Type ... 123
DLL RESET ... 124
Write Recovery ... 125
Precharge Power-Down (Precharge PD) ... 125
CAS Latency (CL) ... 125
Mode Register 1 (MR1) ... 127
DLL Enable/DLL Disable ... 127
Output Drive Strength ... 128
OUTPUT ENABLE/DISABLE ... 128
TDQS Enable ... 128
On-Die Termination ... 129
WRITE LEVELING ... 129
POSTED CAS ADDITIVE Latency ... 129
Mode Register 2 (MR2) ... 130
CAS WRITE Latency (CWL) ... 131
AUTO SELF REFRESH (ASR) ... 131
SELF REFRESH TEMPERATURE (SRT) ... 132
SRT vs. ASR ... 132
DYNAMIC ODT ... 132
Mode Register 3 (MR3) ... 133
MULTIPURPOSE REGISTER (MPR) ... 133
MPR Functional Description ... 134
MPR Register Address Definitions and Bursting Order ... 135
MPR Read Predefined Pattern ... 141
MODE REGISTER SET (MRS) Command ... 141
ZQ CALIBRATION Operation ... 142
ACTIVATE Operation ... 143
READ Operation ... 145
WRITE Operation ... 156
DQ Input Timing ... 164
PRECHARGE Operation ... 166
SELF REFRESH Operation ... 166
Extended Temperature Usage ... 167
Power-Down Mode ... 169
RESET Operation ... 177
On-Die Termination (ODT) ... 179
Functional Representation of ODT ... 179
Nominal ODT ... 179
Dynamic ODT ... 181
Dynamic ODT Special Use Case ... 181

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Functional Description 181
Synchronous ODT Mode 187
ODT Latency and Posted ODT 187
Timing Parameters 187
ODT Off During READs 190
Asynchronous ODT Mode 192
Synchronous to Asynchronous ODT Mode Transition (Power-Down Entry) 194
Asynchronous to Synchronous ODT Mode Transition (Power-Down Exit) 196
Asynchronous to Synchronous ODT Mode Transition (Short CKE Pulse) 198
Revision History 200
Rev. D – 02/17 200
Rev. C – 05/16 200
Rev. B – 04/16 200
Rev. A – 12/15 200

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List of Figures

Figure 1: DDR3L Part Numbers 2
Figure 2: Simplified State Diagram 11
Figure 3: 1 Gig x 4 Functional Block Diagram 14
Figure 4: 512 Meg x 8 Functional Block Diagram 15
Figure 5: 256 Meg x 16 Functional Block Diagram 15
Figure 6: 78-Ball FBGA – x4, x8 (Top View) 16
Figure 7: 96-Ball FBGA – x16 (Top View) 17
Figure 8: 78-Ball FBGA – x4, x8 (DA) 22
Figure 9: 96-Ball FBGA – x16 (TW) 23
Figure 10: Thermal Measurement Point 26
Figure 11: DDR3L 1.35V Input Signal 45
Figure 12: Overshoot 46
Figure 13: Undershoot 47
Figure 14: V_{IX} for Differential Signals 47
Figure 15: Single-Ended Requirements for Differential Signals 47
Figure 16: Definition of Differential AC-Swing and ^{t}DVAC 48
Figure 17: Nominal Slew Rate Definition for Single-Ended Input Signals 50
Figure 18: DDR3L 1.35V Nominal Differential Input Slew Rate Definition for DQS, DQS# and CK, CK# 51
Figure 19: ODT Levels and I-V Characteristics 52
Figure 20: ODT Timing Reference Load 55
Figure 21: ^{t}AON and ^{t}AOF Definitions 56
Figure 22: ^{t}AONPD and ^{t}AOFPD Definitions 56
Figure 23: ^{t}ADC Definition 57
Figure 24: Output Driver 58
Figure 25: DQ Output Signal 65
Figure 26: Differential Output Signal 66
Figure 27: Reference Output Load for AC Timing and Output Slew Rate 67
Figure 28: Nominal Slew Rate Definition for Single-Ended Output Signals 68
Figure 29: Nominal Differential Output Slew Rate Definition for DQS, DQS# 69
Figure 30: Nominal Slew Rate and ^{t}VAC for ^{t}IS (Command and Address – Clock) 87
Figure 31: Nominal Slew Rate for ^{t}IH (Command and Address – Clock) 88
Figure 32: Tangent Line for ^{t}IS (Command and Address – Clock) 89
Figure 33: Tangent Line for ^{t}IH (Command and Address – Clock) 90
Figure 34: Nominal Slew Rate and ^{t}VAC for ^{t}DS (DQ – Strobe) 95
Figure 35: Nominal Slew Rate for ^{t}DH (DQ – Strobe) 96
Figure 36: Tangent Line for ^{t}DS (DQ – Strobe) 97
Figure 37: Tangent Line for ^{t}DH (DQ – Strobe) 98
Figure 38: Refresh Mode 105
Figure 39: DLL Enable Mode to DLL Disable Mode 107
Figure 40: DLL Disable Mode to DLL Enable Mode 108
Figure 41: DLL Disable ^{t}DQSCK 109
Figure 42: Change Frequency During Precharge Power-Down 111
Figure 43: Write Leveling Concept 112
Figure 44: Write Leveling Sequence 115
Figure 45: Write Leveling Exit Procedure 116
Figure 46: Initialization Sequence 118
Figure 47: V_{DD} Voltage Switching 120
Figure 48: MRS to MRS Command Timing (^{t}MRD) 121
Figure 49: MRS to nonMRS Command Timing (^{t}MOD) 122
Figure 50: Mode Register 0 (MR0) Definitions 123

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Figure 51: READ Latency 126
Figure 52: Mode Register 1 (MR1) Definition 127
Figure 53: READ Latency (AL = 5, CL = 6) 130
Figure 54: Mode Register 2 (MR2) Definition 131
Figure 55: CAS WRITE Latency 131
Figure 56: Mode Register 3 (MR3) Definition 133
Figure 57: Multipurpose Register (MPR) Block Diagram 134
Figure 58: MPR System Read Calibration with BL8: Fixed Burst Order Single Readout 137
Figure 59: MPR System Read Calibration with BL8: Fixed Burst Order, Back-to-Back Readout 138
Figure 60: MPR System Read Calibration with BC4: Lower Nibble, Then Upper Nibble 139
Figure 61: MPR System Read Calibration with BC4: Upper Nibble, Then Lower Nibble 140
Figure 62: ZQ CALIBRATION Timing (ZQCL and ZQCS) 142
Figure 63: Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN) 143
Figure 64: Example: ^{t}FAW 144
Figure 65: READ Latency 145
Figure 66: Consecutive READ Bursts (BL8) 147
Figure 67: Consecutive READ Bursts (BC4) 147
Figure 68: Nonconsecutive READ Bursts 148
Figure 69: READ (BL8) to WRITE (BL8) 148
Figure 70: READ (BC4) to WRITE (BC4) OTF 149
Figure 71: READ to PRECHARGE (BL8) 149
Figure 72: READ to PRECHARGE (BC4) 150
Figure 73: READ to PRECHARGE (AL = 5, CL = 6) 150
Figure 74: READ with Auto Precharge (AL = 4, CL = 6) 150
Figure 75: Data Output Timing – ^{t}DQSQ and Data Valid Window 152
Figure 76: Data Strobe Timing – READs 153
Figure 77: Method for Calculating ^{t}LZ and ^{t}HZ 154
Figure 78: ^{t}RPRE Timing 154
Figure 79: ^{t}RPST Timing 155
Figure 80: ^{t}WPRE Timing 157
Figure 81: ^{t}WPST Timing 157
Figure 82: WRITE Burst 158
Figure 83: Consecutive WRITE (BL8) to WRITE (BL8) 159
Figure 84: Consecutive WRITE (BC4) to WRITE (BC4) via OTF 159
Figure 85: Nonconsecutive WRITE to WRITE 160
Figure 86: WRITE (BL8) to READ (BL8) 160
Figure 87: WRITE to READ (BC4 Mode Register Setting) 161
Figure 88: WRITE (BC4 OTF) to READ (BC4 OTF) 162
Figure 89: WRITE (BL8) to PRECHARGE 163
Figure 90: WRITE (BC4 Mode Register Setting) to PRECHARGE 163
Figure 91: WRITE (BC4 OTF) to PRECHARGE 164
Figure 92: Data Input Timing 165
Figure 93: Self Refresh Entry/Exit Timing 167
Figure 94: Active Power-Down Entry and Exit 171
Figure 95: Precharge Power-Down (Fast-Exit Mode) Entry and Exit 171
Figure 96: Precharge Power-Down (Slow-Exit Mode) Entry and Exit 172
Figure 97: Power-Down Entry After READ or READ with Auto Precharge (RDAP) 172
Figure 98: Power-Down Entry After WRITE 173
Figure 99: Power-Down Entry After WRITE with Auto Precharge (WRAP) 173
Figure 100: REFRESH to Power-Down Entry 174
Figure 101: ACTIVATE to Power-Down Entry 174
Figure 102: PRECHARGE to Power-Down Entry 175

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Figure 103: MRS Command to Power-Down Entry ... 175
Figure 104: Power-Down Exit to Refresh to Power-Down Entry ... 176
Figure 105: RESET Sequence ... 178
Figure 106: On-Die Termination ... 179
Figure 107: Dynamic ODT: ODT Asserted Before and After the WRITE, BC4 ... 184
Figure 108: Dynamic ODT: Without WRITE Command ... 184
Figure 109: Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8 ... 185
Figure 110: Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4 ... 186
Figure 111: Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4 ... 186
Figure 112: Synchronous ODT ... 188
Figure 113: Synchronous ODT (BC4) ... 189
Figure 114: ODT During READs ... 191
Figure 115: Asynchronous ODT Timing with Fast ODT Transition ... 193
Figure 116: Synchronous to Asynchronous Transition During Precharge Power-Down (DLL Off) Entry ... 195
Figure 117: Asynchronous to Synchronous Transition During Precharge Power-Down (DLL Off) Exit ... 197
Figure 118: Transition Period for Short CKE LOW Cycles with Entry and Exit Period Overlapping ... 199
Figure 119: Transition Period for Short CKE HIGH Cycles with Entry and Exit Period Overlapping ... 199

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List of Tables

Table 1: Key Timing Parameters 1
Table 2: Addressing 2
Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions 18
Table 4: 96-Ball FBGA – x16 Ball Descriptions 20
Table 5: Absolute Maximum Ratings 24
Table 6: DDR3L Input/Output Capacitance 25
Table 7: Thermal Characteristics 26
Table 8: Thermal Impedance 27
Table 9: Timing Parameters Used for I_{DD} Measurements – Clock Units 28
Table 10: I_{DD0} Measurement Loop 29
Table 11: I_{DD1} Measurement Loop 30
Table 12: I_{DD} Measurement Conditions for Power-Down Currents 31
Table 13: I_{DD2N} and I_{DD3N} Measurement Loop 32
Table 14: I_{DD2NT} Measurement Loop 32
Table 15: I_{DD4R} Measurement Loop 33
Table 16: I_{DD4W} Measurement Loop 34
Table 17: I_{DD5B} Measurement Loop 35
Table 18: I_{DD} Measurement Conditions for I_{DD6}, I_{DD6ET}, and I_{DD8} 36
Table 19: I_{DD7} Measurement Loop 37
Table 20: I_{DD} Maximum Limits Die Rev. P for 1.35V/1.5V Operation 39
Table 21: DDR3L 1.35V DC Electrical Characteristics and Operating Conditions 41
Table 22: DDR3L 1.35V DC Electrical Characteristics and Input Conditions 42
Table 23: DDR3L 1.35V Input Switching Conditions – Command and Address 43
Table 24: DDR3L 1.35V Differential Input Operating Conditions (CK, CK# and DQS, DQS#) 44
Table 25: DDR3L Control and Address Pins 46
Table 26: DDR3L 1.35V Clock, Data, Strobe, and Mask Pins 46
Table 27: DDR3L 1.35V – Minimum Required Time ^{t}DVAC for CK/CK#, DQS/DQS# Differential for AC Ringback .. 48
Table 28: Single-Ended Input Slew Rate Definition 49
Table 29: DDR3L 1.35V Differential Input Slew Rate Definition 51
Table 30: On-Die Termination DC Electrical Characteristics 52
Table 31: 1.35V R_{TT} Effective Impedance 53
Table 32: ODT Sensitivity Definition 54
Table 33: ODT Temperature and Voltage Sensitivity 54
Table 34: ODT Timing Definitions 55
Table 35: DDR3L(1.35V) Reference Settings for ODT Timing Measurements 55
Table 36: DDR3L 34 Ohm Driver Impedance Characteristics 59
Table 37: DDR3L 34 Ohm Driver Pull-Up and Pull-Down Impedance Calculations 60
Table 38: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ}$ = DDR3L@1.35V 60
Table 39: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ}$ = DDR3L@1.45V 60
Table 40: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ}$ = DDR3L@1.283 61
Table 41: DDR3L 34 Ohm Output Driver Sensitivity Definition 61
Table 42: DDR3L 34 Ohm Output Driver Voltage and Temperature Sensitivity 61
Table 43: DDR3L 40 Ohm Driver Impedance Characteristics 62
Table 44: DDR3L 40 Ohm Output Driver Sensitivity Definition 62
Table 45: 40 Ohm Output Driver Voltage and Temperature Sensitivity 63
Table 46: DDR3L Single-Ended Output Driver Characteristics 64
Table 47: DDR3L Differential Output Driver Characteristics 65
Table 48: DDR3L Differential Output Driver Characteristics $V_{OX(AC)}$ 66
Table 49: Single-Ended Output Slew Rate Definition 67
Table 50: Differential Output Slew Rate Definition 69

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Table 51: DDR3L-1066 Speed Bins 70
Table 52: DDR3L-1333 Speed Bins 71
Table 53: DDR3L-1600 Speed Bins 72
Table 54: DDR3L-1866 Speed Bins 73
Table 55: DDR3L-2133 Speed Bins 74
Table 56: Electrical Characteristics and AC Operating Conditions for Speed Extensions 75
Table 57: DDR3L Command and Address Setup and Hold Values 1 V/ns Referenced – AC/DC-Based 84
Table 58: DDR3L-800/1066 Derating Values ^{t}IS/^{t}IH – AC160/DC90-Based 85
Table 59: DDR3L-800/1066/1333/1600 Derating Values for ^{t}IS/^{t}IH – AC135/DC90-Based 85
Table 60: DDR3L-1866/2133 Derating Values for ^{t}IS/^{t}IH – AC125/DC90-Based 85
Table 61: DDR3L Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL[AC]}$) for Valid ADD/CMD Transition .. 86
Table 62: DDR3L Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based 91
Table 63: DDR3L Derating Values for ^{t}DS/^{t}DH – AC160/DC90-Based 92
Table 64: DDR3L Derating Values for ^{t}DS/^{t}DH – AC135/DC90-Based 92
Table 65: DDR3L Derating Values for ^{t}DS/^{t}DH – AC130/DC90-Based at 2V/ns 93
Table 66: DDR3L Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQ Transition 94
Table 67: Truth Table – Command 99
Table 68: Truth Table – CKE 101
Table 69: READ Command Summary 103
Table 70: WRITE Command Summary 103
Table 71: READ Electrical Characteristics, DLL Disable Mode 109
Table 72: Write Leveling Matrix 113
Table 73: Burst Order 124
Table 74: MPR Functional Description of MR3 Bits 134
Table 75: MPR Readouts and Burst Order Bit Mapping 135
Table 76: Self Refresh Temperature and Auto Self Refresh Description 168
Table 77: Self Refresh Mode Summary 168
Table 78: Command to Power-Down Entry Parameters 169
Table 79: Power-Down Modes 170
Table 80: Truth Table – ODT (Nominal) 180
Table 81: ODT Parameters 180
Table 82: Write Leveling with Dynamic ODT Special Case 181
Table 83: Dynamic ODT Specific Parameters 182
Table 84: Mode Registers for $R_{TT,nom}$ 182
Table 85: Mode Registers for $R_{TT(WR)}$ 183
Table 86: Timing Diagrams for Dynamic ODT 183
Table 87: Synchronous ODT Parameters 188
Table 88: Asynchronous ODT Timing Parameters for All Speed Bins 193
Table 89: ODT Parameters for Power-Down (DLL Off) Entry and Exit Transition Period 195

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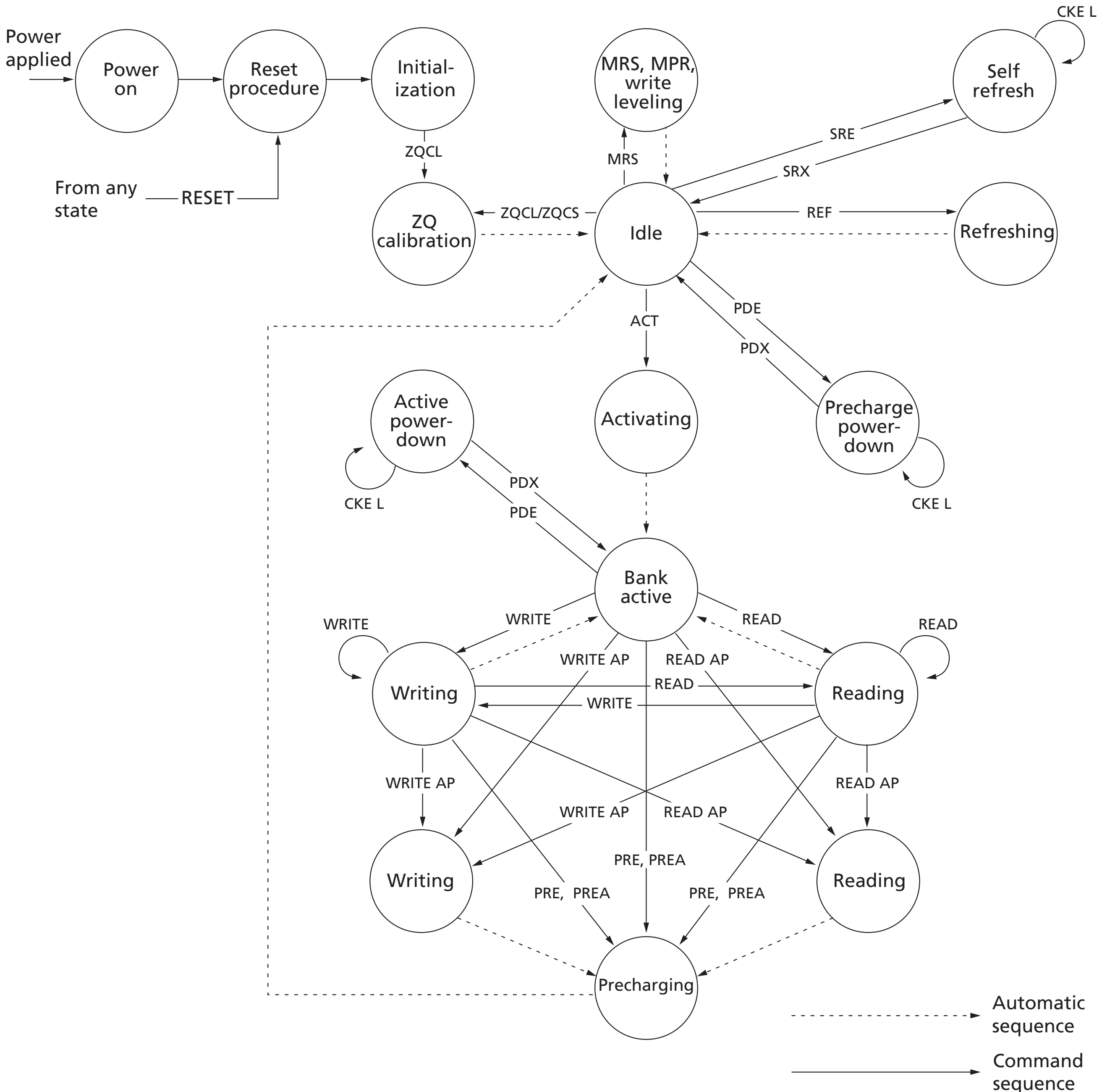
State Diagram

Figure 2: Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

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Functional Description

DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Industrial Temperature

The industrial temperature (IT) device requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is < 0°C or >85°C.

Automotive Temperature

The automotive temperature (AT) device requires that the case temperature not exceed –40°C or 105°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is < 0°C or >85°C.

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Ultra-high Temperature

The Utra-high temperature (UT) device requires that the case temperature not exceed –40°C or 125°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature auto refresh option. When Tc > +105C, the refresh rate must be increased to 8X. Self-refresh mode is not available for Tc >+105°C. Additionally, ODT resistance and the input/output impedance must be derated when T_C is < 0°C or >85°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout this data sheet, various figures and text refer to DQs as "DQ." DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "DQS" and "CK" found throughout this data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Row addressing is denoted as A[*n*:0]. *For example,* 1Gb: *n* = 12 (x16); 1Gb: *n* = 13 (x4, x8); 2Gb: *n* = 13 (x16) and 2Gb: *n* = 14 (x4, x8); 4Gb: *n* = 14 (x16); and 4Gb: *n* = 15 (x4, x8).
- Dynamic ODT has a special use case: when DDR3 devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed. Refer to the Dynamic ODT Special Use Case section.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:

  – Connect UDQS to ground via 1kΩ* resistor.
  – Connect UDQS# to V_{DD} via 1kΩ* resistor.
  – Connect UDM to V_{DD} via 1kΩ* resistor.
  – Connect DQ[15:8] individually to either V_{SS}, V_{DD}, or V_{REF} via 1kΩ resistors,* or float DQ[15:8].

  *If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.

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Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

Figure 3: 1 Gig x 4 Functional Block Diagram

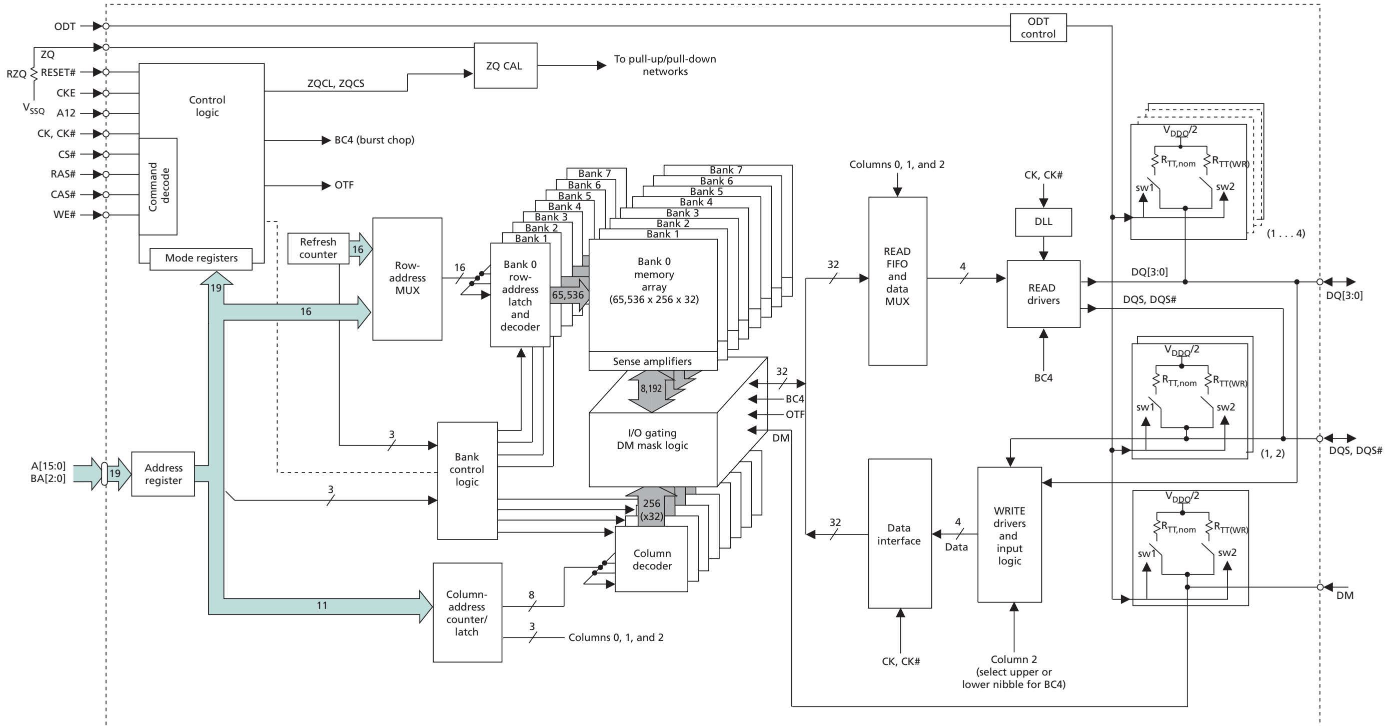


Figure 4: 512 Meg x 8 Functional Block Diagram

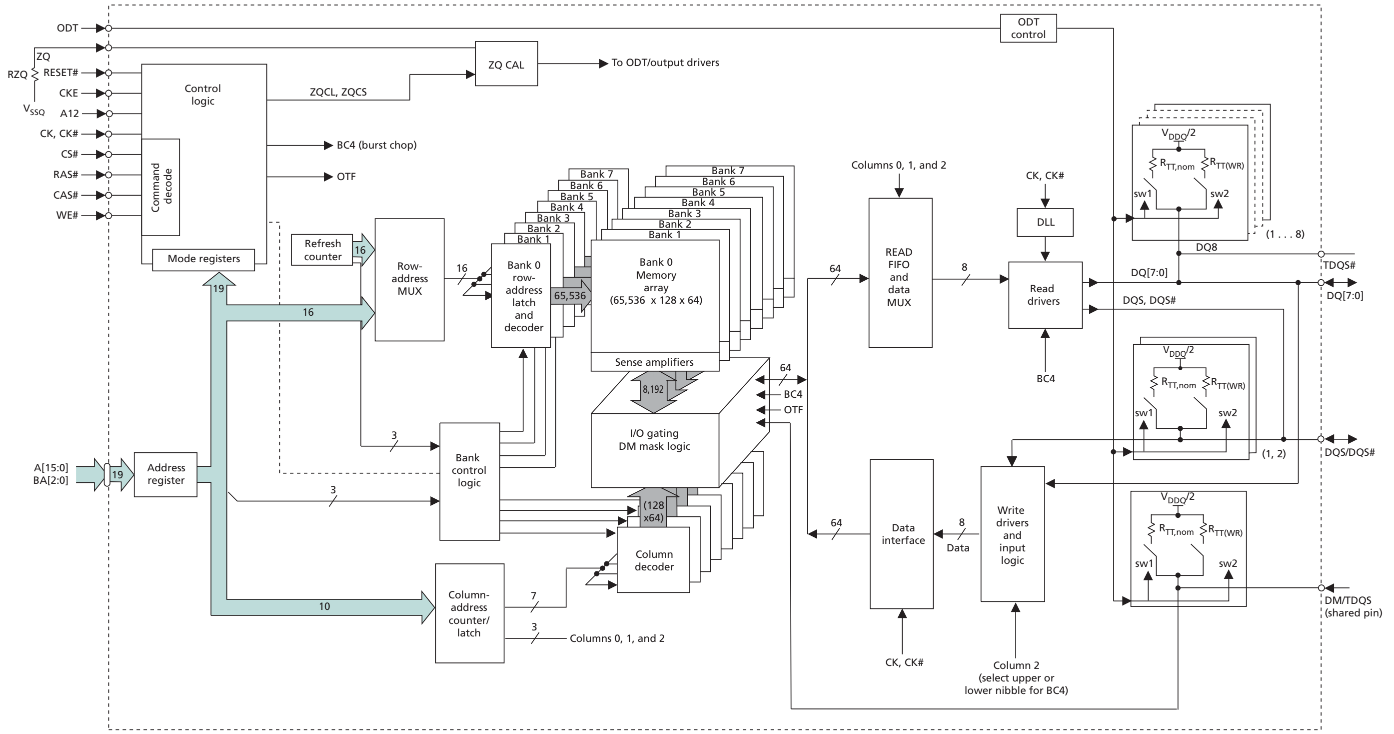
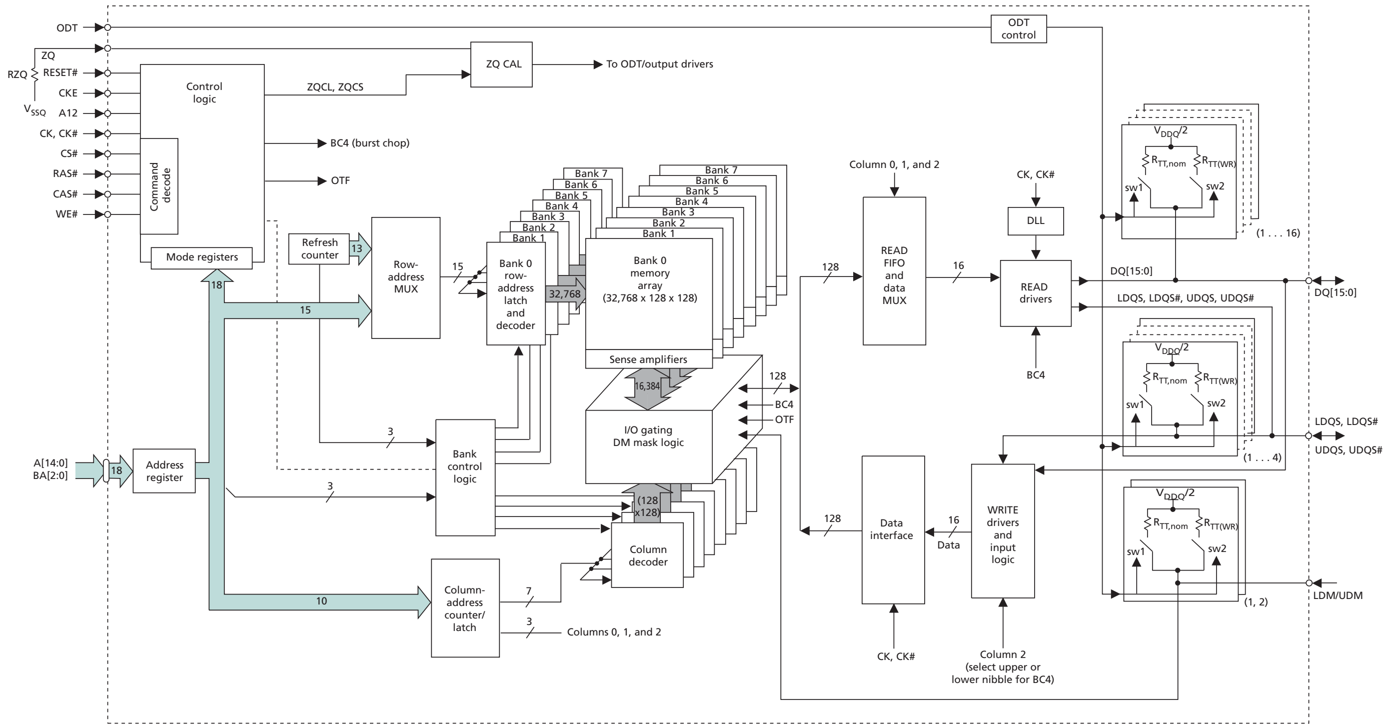


Figure 5: 256 Meg x 16 Functional Block Diagram



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Ball Assignments and Descriptions

Figure 6: 78-Ball FBGA – x4, x8 (Top View)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DD}	NC				NF, NF/TDQS#	V_{SS}	V_{DD}
B	V_{SS}	V_{SSQ}	DQ0				DM, DM/TDQS	V_{SSQ}	V_{DDQ}
C	V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}
D	V_{SSQ}	NF, DQ6	DQS#				V_{DD}	V_{SS}	V_{SSQ}
E	V_{REFDQ}	V_{DDQ}	NF, DQ4				NF, DQ7	NF, DQ5	V_{DDQ}
F	NC	V_{SS}	RAS#				CK	V_{SS}	NC
G	ODT	V_{DD}	CAS#				CK#	V_{DD}	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	V_{SS}	BA0	BA2				A15	V_{REFCA}	V_{SS}
K	V_{DD}	A3	A0				A12/BC#	BA1	V_{DD}
L	V_{SS}	A5	A2				A1	A4	V_{SS}
M	V_{DD}	A7	A9				A11	A6	V_{DD}
N	V_{SS}	RESET#	A13				A14	A8	V_{SS}

Notes: 1. Ball descriptions listed in Table 3 (page 18) are listed as "x4, x8" if unique; otherwise, x4 and x8 are the same.

2. A comma separates the configuration; a slash defines a selectable function. Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

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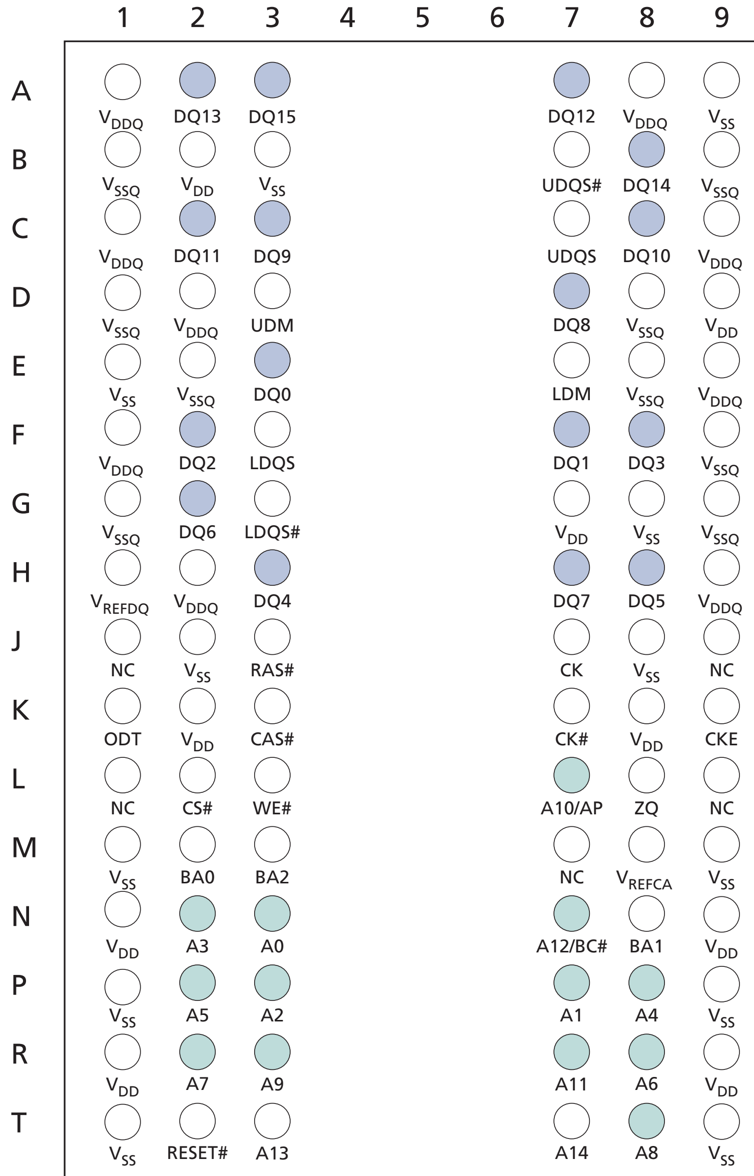
Figure 7: 96-Ball FBGA – x16 (Top View)



Notes:
1. Ball descriptions listed in Table 4 (page 20) are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function. Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

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Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Symbol	Type	Description
A[15:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Table 67 (page 99).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/ disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. DM has an optional use as TDQS on the x8.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.

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Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	Output	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

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Table 4: 96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Table 67 (page 99).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.

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Table 4: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

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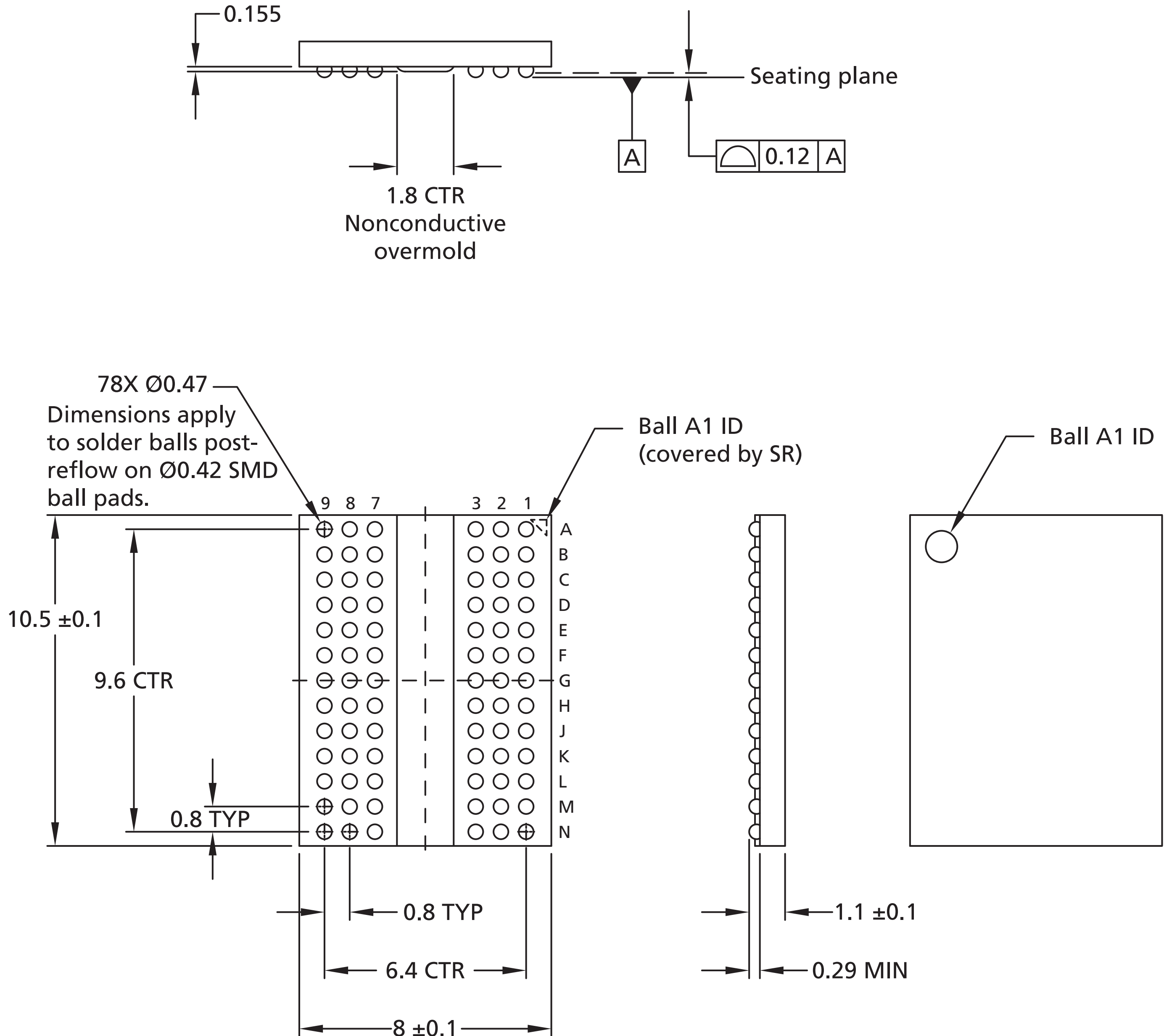
Package Dimensions

Figure 8: 78-Ball FBGA – x4, x8 (DA)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

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Figure 9: 96-Ball FBGA – x16 (TW)

0.155
Seating plane
1.8 CTR
Nonconductive
overmold
A
0.12 A

96X Ø0.47
Dimensions apply
to solder balls post-
reflow on Ø0.42 SMD
ball pads.

Ball A1 ID
(covered by SR)

Ball A1 ID

9 8 7 3 2 1
A B C D E F G H J K L M N P R T

14 ±0.1
12 CTR
0.8 TYP
0.8 TYP
6.4 CTR
8 ±0.1
1.1 ±0.1
0.34 ±0.05

Notes:
1. All dimensions are in millimeters.
2. Material composition: Pb-free SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

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Electrical Specifications

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}	–0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V	
T_C	Operating case temperature – Commercial	0	95	°C	2, 3
	Operating case temperature – Industrial	–40	95	°C	2, 3
	Operating case temperature – Automotive	–40	105	°C	2, 3
	Operating case temperature – Ultra-high	–40	125	°C	2, 3
T_{STG}	Storage temperature	–55	150	°C	

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.
2. MAX operating case temperature. T_C is measured in the center of the package.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. Ultra-high temperature use based on automotive usage model. Please contact Micron sales representative if you have questions.

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Input/Output Capacitance

Table 6: DDR3L Input/Output Capacitance

Note 1 applies to the entire table

Capacitance Parameters	Sym	DDR3L -800		DDR3L -1066		DDR3L -1333		DDR3L -1600		DDR3L -1866		DDR3L -2133		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CK and CK#	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	0.8	1.3	pF	
ΔC: CK to CK#	C_{DCK}	0.0	0.15	0.0	0.15	0.0	0.15	0.0	0.15	0.0	0.15	0.0	0.15	pF	
Single-end I/O: DQ, DM	C_{IO}	1.4	2.5	1.4	2.5	1.4	2.3	1.4	2.2	1.4	2.1	1.4	2.1	pF	2
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.4	2.5	1.4	2.5	1.4	2.3	1.4	2.2	1.4	2.1	1.4	2.1	pF	3
ΔC: DQS to DQS#, TDQS, TDQS#	C_{DDQS}	0.0	0.2	0.0	0.2	0.0	0.15	0.0	0.15	0.0	0.15	0.0	0.15	pF	3
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	4
Inputs (CTRL, CMD, ADDR)	C_I	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	0.75	1.2	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	–0.5	0.3	–0.5	0.3	–0.4	0.2	–0.4	0.2	–0.4	0.2	–0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	$C_{DI_CMD_ADDR}$	–0.5	0.5	–0.5	0.5	–0.4	0.4	–0.4	0.4	–0.4	0.4	–0.4	0.4	pF	7
ZQ pin capacitance	C_{ZQ}	–	3.0	–	3.0	–	3.0	–	3.0	–	3.0	–	3.0	pF	
Reset pin capacitance	C_{RE}	–	3.0	–	3.0	–	3.0	–	3.0	–	3.0	–	3.0	pF	

Notes:
1. V_{DD} = 1.35V (1.283–1.45V), $V_{DDQ} = V_{DD}$, $V_{REF} = V_{SS}$, f = 100 MHz, T_C = 25°C. $V_{OUT(DC)} = 0.5 \times V_{DDQ}$, V_{OUT} = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes TDQS, TDQS#. C_{DDQS} is for DQS vs. DQS# and TDQS vs. TDQS# separately.
4. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO(DQS)} + C_{IO(DQS\#)})$.
5. Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR = A[*n*:0], BA[2:0].
6. $C_{DI_CTRL} = C_{I(CTRL)} - 0.5 \times (C_{CK(CK)} + C_{CK(CK\#)})$.
7. $C_{DI_CMD_ADDR} = C_{I(CMD_ADDR)} - 0.5 \times (C_{CK(CK)} + C_{CK(CK\#)})$.

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