Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Mobile LPDDR2 SDRAM

MT42L256M16D1, MT42L128M32D1, MT42L256M32D2, MT42L128M64D2, MT42L512M32D4, MT42L192M64D3, MT42L256M64D4, MT42L384M32D3

Features

- Ultra low-voltage core and I/O power supplies
  - V_{DD2} = 1.14–1.30V
  - V_{DDCA}/V_{DDQ} = 1.14–1.30V
  - V_{DD1} = 1.70–1.95V
- Clock frequency range
  - 533–10 MHz (data rate range: 1066–20 Mb/s/pin)
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Per-bank refresh for concurrent operation
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- RoHS-compliant, "green" packaging

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL	$^tRCD/^tRP$[1]
-18	533	1066	8	4	Typical
-25	400	800	6	3	Typical
-3	333	667	5	2	Typical

Options

Options	Marking
• V_{DD2}: 1.2V	L
• Configuration	
– 32 Meg x 16 x 8 banks x 1 die	256M16
– 16 Meg x 32 x 8 banks x 1 die	128M32
– 16 Meg x 32 x 8 banks x 2 die	256M32
– 1 (16 Meg x 32 x 8 banks) + 2 (32 Meg x 16 x 8 banks)	384M32
– 32 Meg x 16 x 8 banks x 4 die	512M32
– 16 Meg x 32 x 8 banks x 2 die	128M64
– 16 Meg x 32 x 8 banks x 3 die	192M64
– 16 Meg x 32 x 8 banks x 4 die	256M64
• Device type	
– LPDDR2-S4, 1 die in package	D1
– LPDDR2-S4, 2 die in package	D2
– LPDDR2-S4, 3 die in package	D3
– LPDDR2-S4, 4 die in package	D4
• FBGA "green" package	
– 134-ball FBGA (10mm x 11.5mm)	GU, GV
– 168-ball FBGA (12mm x 12mm)	LF, LG
– 216-ball FBGA (12mm x 12mm)	LH, LK, LL, LM, LP
– 220-ball FBGA (14mm x 14mm)	LD, MP
– 240-ball FBGA (14mm x 14mm)	MC
– 253-ball FBGA (11mm x 11mm)	EU, EV
• Timing – cycle time	
– 1.875ns @ RL = 8	-18
– 2.5ns @ RL = 6	-25
– 3.0ns @ RL = 5	-3
• Operating temperature range	
– From –30°C to +85°C	WT
– From –40°C to +105°C	AT
• Revision	:A

Note: 1. For Fast $^tRCD/^tRP$, contact factory.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.
Products and specifications discussed herein are subject to change by Micron without notice.

Table 2: Single Channel S4 Configuration Addressing

Architecture		256 Meg x 16	128 Meg x 32	256 Meg x 32	384 Meg x 32	512 Meg x 32
Die configuration	CS0#	32 Meg x 16 x 8 banks	16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks	32 Meg x 16 x 8 banks
	CS1#	n/a	n/a	16 Meg x 32 x 8 banks	32 Meg x 32 x 8 banks	32 Meg x 16 x 8 banks
Row addressing		16K (A[13:0])	16K (A[13:0])	16K (A[13:0])	16K (A[13:0])	16K (A[13:0])
Column addressing	CS0#	2K (A[10:0])	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])	2K (A[10:0])
	CS1#	n/a	n/a	1K (A[9:0])	2K (A[10:0])	2K (A[10:0])
Number of die		1	1	2	3	4
Die per rank	CS0#	1	1	1	1	2
	CS1#	0	0	1	2	2
Ranks per channel [1]		1	1	2	2	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

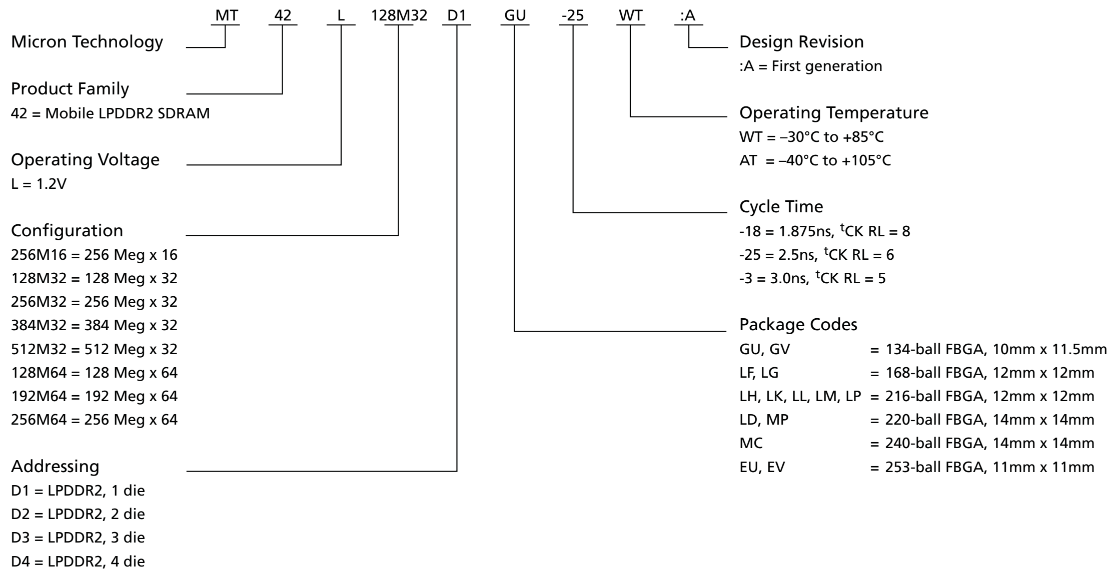
Table 3: Dual Channel S4 Configuration Addressing

Architecture		128 Meg x 64	192 Meg x 64	256 Meg x 64
Die configuration		16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks
Row addressing		16K (A[13:0])	16K (A[13:0])	16K (A[13:0])
Column addressing	CS0#	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
	CS1#	n/a	1K (A[9:0])	1K (A[9:0])
Number of die		2	3	4
Die per rank	CS0#	1	1	1
	CS1#	0	1 = Channel A 0 = Channel B	1
Ranks per channel [1]	Channel A	1	2	2
	Channel B	1	1	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 1: 4Gb LPDDR2 Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Table 4: Package Codes and Descriptions

Package Code	Ball Count	# Ranks	# Channels	Size (mm)	Die per Package	Solder Ball Composition
GU	134	1	1	10 x 11.5 x 0.7, 0.65 pitch	SDP	LF35 (w/OSP)
GV	134	2	1	10 x 11.5 x 0.85, 0.65 pitch	DDP	LF35 (w/OSP)
LF	168	1	1	12 x 12 x 0.75, 0.5 pitch	SDP	SAC305
LG	168	2	1	12 x 12 x 0.8, 0.5 pitch	DDP	SAC305
LH	216	1	1 (Chan B only)	12 x 12 x 0.65, 0.4 pitch	SDP	SAC305
LL	216	1	2	12 x 12 x 0.8, 0.4 pitch	DDP	SAC305
LM	216	2	2	12 x 12 x 1.0, 0.4 pitch	QDP	SAC305
LK	216	2	1 (Chan B only)	12 x 12 x 0.8, 0.4 pitch	DDP	SAC305
LP	216	2	1 (Chan B only)	12 x 12 x 0.82, 0.4 pitch	3DP	SAC305
MP	220	1	2	14 x 14 x 0.8, 0.5 pitch	DDP	SAC305
LD	220	2	2	14 x 14 x 1.0, 0.5 pitch	QDP	SAC305
MC	240	1	2	14 x 14 x 0.8, 0.5 pitch	DDP	SAC305
EU	253	1	2	11 x 11 x 0.9, 0.5 pitch	DDP	LF35 (w/OSP)
EV	253	2	2	11 x 11 x 1.2, 0.5 pitch	QDP	LF35 (w/OSP)

Notes:
1. SDP = single-die package, DDP = dual-die package, 3DP = triple-die package, QDP = quad-die package
2. Solder ball material: LF35 with Cu OSP ball pads (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni),

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Contents

General Description 12
General Notes 12
I_{DD} Specifications 13
Package Block Diagrams 18
Package Dimensions 24
Ball Assignments and Descriptions 37
Functional Description 46
Power-Up 47
Initialization After RESET (Without Voltage Ramp) 49
Power-Off 49
Uncontrolled Power-Off 50
Mode Register Definition 50
Mode Register Assignments and Definitions 50
ACTIVATE Command 61
8-Bank Device Operation 61
Read and Write Access Modes 62
Burst READ Command 62
READs Interrupted by a READ 69
Burst WRITE Command 69
WRITEs Interrupted by a WRITE 72
BURST TERMINATE Command 72
Write Data Mask 74
PRECHARGE Command 75
READ Burst Followed by PRECHARGE 76
WRITE Burst Followed by PRECHARGE 77
Auto Precharge 78
READ Burst with Auto Precharge 78
WRITE Burst with Auto Precharge 79
REFRESH Command 81
REFRESH Requirements 87
SELF REFRESH Operation 89
Partial-Array Self Refresh – Bank Masking 90
Partial-Array Self Refresh – Segment Masking 91
MODE REGISTER READ 92
Temperature Sensor 94
DQ Calibration 96
MODE REGISTER WRITE Command 98
MRW RESET Command 98
MRW ZQ Calibration Commands 99
ZQ External Resistor Value, Tolerance, and Capacitive Loading 101
Power-Down 101
Deep Power-Down 108
Input Clock Frequency Changes and Stop Events 109
Input Clock Frequency Changes and Clock Stop with CKE LOW 109
Input Clock Frequency Changes and Clock Stop with CKE HIGH 110
NO OPERATION Command 110
Simplified Bus Interface State Diagram 110
Truth Tables 112
Electrical Specifications 120
Absolute Maximum Ratings 120

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Input/Output Capacitance 120
Electrical Specifications – I_{DD} Specifications and Conditions 121
AC and DC Operating Conditions 124
AC and DC Logic Input Measurement Levels for Single-Ended Signals 127
V_{REF} Tolerances 128
Input Signal 128
AC and DC Logic Input Measurement Levels for Differential Signals 131
Single-Ended Requirements for Differential Signals 132
Differential Input Crosspoint Voltage 134
Input Slew Rate 134
Output Characteristics and Operating Conditions 135
Single-Ended Output Slew Rate 136
Differential Output Slew Rate 137
HSUL_12 Driver Output Timing Reference Load 140
Output Driver Impedance 140
Output Driver Impedance Characteristics with ZQ Calibration 141
Output Driver Temperature and Voltage Sensitivity 142
Output Impedance Characteristics Without ZQ Calibration 142
Clock Specification 146
^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) 147
Clock Period Jitter 147
Clock Period Jitter Effects on Core Timing Parameters 147
Cycle Time Derating for Core Timing Parameters 148
Clock Cycle Derating for Core Timing Parameters 148
Clock Jitter Effects on Command/Address Timing Parameters 148
Clock Jitter Effects on READ Timing Parameters 148
Clock Jitter Effects on WRITE Timing Parameters 149
Refresh Requirements 150
AC Timing 151
CA and CS# Setup, Hold, and Derating 157
Data Setup, Hold, and Slew Rate Derating 164
Revision History 171
Rev. O – 08/13 171
Rev. N – 05/13 171
Rev. M – 10/12 171
Rev. L – 08/12 171
Rev. K – 07/12 171
Rev. J – 07/12 171
Rev. I – 05/12 171
Rev. H – 04/12 171
Rev. G – 04/12 172
Rev. F – 03/12 172
Rev. E – 02/12 172
Rev. D – 12/11 172
Rev. C – 12/11 172
Rev. B – 05/11 172
Rev. A – 02/11 172

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

List of Figures

Figure 1: 4Gb LPDDR2 Part Numbering ... 3
Figure 2: V_{DD1} Typical Self Refresh Current vs. Temperature ... 17
Figure 3: V_{DD2} Typical Self Refresh Current vs. Temperature ... 17
Figure 4: Single Rank, Single Channel Package Block Diagram ... 18
Figure 5: Dual Rank, Single Channel Package Block Diagram ... 18
Figure 6: Dual Rank, Single Channel (3 Die) Package Block Diagram ... 19
Figure 7: Single Rank, Dual Channel Package Block Diagram ... 20
Figure 8: Dual Rank, Dual Channel Package Block Diagram ... 21
Figure 9: Dual Rank, Dual Channel (3 Die) Package Block Diagram ... 22
Figure 10: Dual Rank, Single Channel (4 Die) Package Block Diagram ... 23
Figure 11: 134-Ball FBGA – 10mm x 11.5mm Single-Die (Package Code GU) ... 24
Figure 12: 134-Ball FBGA – 10mm x 11.5mm Dual-Die (Package Code GV) ... 25
Figure 13: 168-Ball FBGA – 12mm x 12mm Single-Die (Package Code LF) ... 26
Figure 14: 168-Ball FBGA – 12mm x 12mm Dual-Die (Package Code LG) ... 27
Figure 15: 216-Ball FBGA – 12mm x 12mm (Package Codes LK, LL) ... 28
Figure 16: 216-Ball FBGA – 12mm x 12mm (Package Code LM) ... 29
Figure 17: 216-Ball FBGA – 12mm x 12mm (Package Code LH) ... 30
Figure 18: 216-Ball FBGA – 12mm x 12mm (Package Code LP) ... 31
Figure 19: 220-Ball FBGA – 14mm x 14mm Dual-Die (Package Code MP) ... 32
Figure 20: 220-Ball FBGA – 14mm x 14mm Quad-Die (Package Code LD) ... 33
Figure 21: 240-Ball FBGA – 14mm x 14mm Dual-Die (Package Code MC) ... 34
Figure 22: 253-Ball FBGA – 11mm x 11mm Dual-Die (Package Code EU) ... 35
Figure 23: 253-Ball FBGA – 11mm x 11mm Quad-Die (Package Code EV) ... 36
Figure 24: 134-Ball FBGA (x16) ... 37
Figure 25: 134-Ball FBGA (x32) ... 38
Figure 26: 168-Ball FBGA – 12mm x 12mm ... 39
Figure 27: 216-Ball 2-Channel FBGA – 12mm x 12mm ... 40
Figure 28: 216-Ball 1-Channel (B) FBGA – 12mm x 12mm ... 41
Figure 29: 220-Ball 2-Channel FBGA – 14mm x 14mm ... 42
Figure 30: 240-Ball 2-Channel FBGA – 14mm x 14mm ... 43
Figure 31: 253-Ball 2-Channel FBGA – 11mm x 11mm ... 44
Figure 32: Functional Block Diagram ... 46
Figure 33: Voltage Ramp and Initialization Sequence ... 49
Figure 34: ACTIVATE Command ... 61
Figure 35: ^{t}FAW Timing (8-Bank Devices) ... 62
Figure 36: READ Output Timing – ^{t}DQSCK (MAX) ... 63
Figure 37: READ Output Timing – ^{t}DQSCK (MIN) ... 63
Figure 38: Burst READ – RL = 5, BL = 4, ^{t}DQSCK > ^{t}CK ... 64
Figure 39: Burst READ – RL = 3, BL = 8, ^{t}DQSCK < ^{t}CK ... 64
Figure 40: ^{t}DQSCKDL Timing ... 65
Figure 41: ^{t}DQSCKDM Timing ... 66
Figure 42: ^{t}DQSCKDS Timing ... 67
Figure 43: Burst READ Followed by Burst WRITE – RL = 3, WL = 1, BL = 4 ... 68
Figure 44: Seamless Burst READ – RL = 3, BL = 4, ^{t}CCD = 2 ... 68
Figure 45: READ Burst Interrupt Example – RL = 3, BL = 8, ^{t}CCD = 2 ... 69
Figure 46: Data Input (WRITE) Timing ... 70
Figure 47: Burst WRITE – WL = 1, BL = 4 ... 70
Figure 48: Burst WRITE Followed by Burst READ – RL = 3, WL = 1, BL = 4 ... 71
Figure 49: Seamless Burst WRITE – WL = 1, BL = 4, ^{t}CCD = 2 ... 71
Figure 50: WRITE Burst Interrupt Timing – WL = 1, BL = 8, ^{t}CCD = 2 ... 72

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 51: Burst WRITE Truncated by BST – WL = 1, BL = 16 73
Figure 52: Burst READ Truncated by BST – RL = 3, BL = 16 74
Figure 53: Data Mask Timing 74
Figure 54: Write Data Mask – Second Data Bit Masked 75
Figure 55: READ Burst Followed by PRECHARGE – RL = 3, BL = 8, RU(^{t}RTP(MIN)/^{t}CK) = 2 76
Figure 56: READ Burst Followed by PRECHARGE – RL = 3, BL = 4, RU(^{t}RTP(MIN)/^{t}CK) = 3 77
Figure 57: WRITE Burst Followed by PRECHARGE – WL = 1, BL = 4 78
Figure 58: READ Burst with Auto Precharge – RL = 3, BL = 4, RU(^{t}RTP(MIN)/^{t}CK) = 2 79
Figure 59: WRITE Burst with Auto Precharge – WL = 1, BL = 4 80
Figure 60: Regular Distributed Refresh Pattern 84
Figure 61: Supported Transition from Repetitive REFRESH Burst 85
Figure 62: Nonsupported Transition from Repetitive REFRESH Burst 86
Figure 63: Recommended Self Refresh Entry and Exit 87
Figure 64: ^{t}SRF Definition 88
Figure 65: All-Bank REFRESH Operation 88
Figure 66: Per-Bank REFRESH Operation 89
Figure 67: SELF REFRESH Operation 90
Figure 68: MRR Timing – RL = 3, ^{t}MRR = 2 92
Figure 69: READ to MRR Timing – RL = 3, ^{t}MRR = 2 93
Figure 70: Burst WRITE Followed by MRR – RL = 3, WL = 1, BL = 4 94
Figure 71: Temperature Sensor Timing 96
Figure 72: MR32 and MR40 DQ Calibration Timing – RL = 3, ^{t}MRR = 2 97
Figure 73: MODE REGISTER WRITE Timing – RL = 3, ^{t}MRW = 5 98
Figure 74: ZQ Timings 100
Figure 75: Power-Down Entry and Exit Timing 102
Figure 76: CKE Intensive Environment 102
Figure 77: REFRESH-to-REFRESH Timing in CKE Intensive Environments 102
Figure 78: READ to Power-Down Entry 103
Figure 79: READ with Auto Precharge to Power-Down Entry 104
Figure 80: WRITE to Power-Down Entry 105
Figure 81: WRITE with Auto Precharge to Power-Down Entry 106
Figure 82: REFRESH Command to Power-Down Entry 107
Figure 83: ACTIVATE Command to Power-Down Entry 107
Figure 84: PRECHARGE Command to Power-Down Entry 107
Figure 85: MRR Command to Power-Down Entry 108
Figure 86: MRW Command to Power-Down Entry 108
Figure 87: Deep Power-Down Entry and Exit Timing 109
Figure 88: Simplified Bus Interface State Diagram 111
Figure 89: V_{REF} DC Tolerance and V_{REF} AC Noise Limits 128
Figure 90: LPDDR2-466 to LPDDR2-1066 Input Signal 129
Figure 91: LPDDR2-200 to LPDDR2-400 Input Signal 130
Figure 92: Differential AC Swing Time and ^{t}DVAC 131
Figure 93: Single-Ended Requirements for Differential Signals 133
Figure 94: V_{IX} Definition 134
Figure 95: Differential Input Slew Rate Definition for CK, CK#, DQS, and DQS# 135
Figure 96: Single-Ended Output Slew Rate Definition 136
Figure 97: Differential Output Slew Rate Definition 138
Figure 98: Overshoot and Undershoot Definition 139
Figure 99: HSUL_12 Driver Output Reference Load for Timing and Slew Rate 140
Figure 100: Output Driver 141
Figure 101: Output Impedance = 240 Ohms, I-V Curves After ZQRESET 144
Figure 102: Output Impedance = 240 Ohms, I-V Curves After Calibration 145

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 103: Command Input Setup and Hold Timing 157
Figure 104: Typical Slew Rate and ^{t}VAC – ^{t}IS for CA and CS# Relative to Clock 160
Figure 105: Typical Slew Rate – ^{t}IH for CA and CS# Relative to Clock 161
Figure 106: Tangent Line – ^{t}IS for CA and CS# Relative to Clock 162
Figure 107: Tangent Line – ^{t}IH for CA and CS# Relative to Clock 163
Figure 108: Typical Slew Rate and ^{t}VAC – ^{t}DS for DQ Relative to Strobe 167
Figure 109: Typical Slew Rate – ^{t}DH for DQ Relative to Strobe 168
Figure 110: Tangent Line – ^{t}DS for DQ with Respect to Strobe 169
Figure 111: Tangent Line – ^{t}DH for DQ with Respect to Strobe 170

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

List of Tables

Table 1: Key Timing Parameters ... 1
Table 2: Single Channel S4 Configuration Addressing ... 2
Table 3: Dual Channel S4 Configuration Addressing ... 2
Table 4: Package Codes and Descriptions ... 3
Table 5: 256 Meg x 16 I_{DD} Specifications ... 13
Table 6: 128 Meg x 32 I_{DD} Specifications ... 14
Table 7: I_{DD6} Partial-Array Self Refresh Current ... 16
Table 8: Ball/Pad Descriptions ... 45
Table 9: Initialization Timing Parameters ... 49
Table 10: Power-Off Timing ... 50
Table 11: Mode Register Assignments ... 51
Table 12: MR0 Device Information (MA[7:0] = 00h) ... 52
Table 13: MR0 Op-Code Bit Definitions ... 52
Table 14: MR1 Device Feature 1 (MA[7:0] = 01h) ... 52
Table 15: MR1 Op-Code Bit Definitions ... 53
Table 16: Burst Sequence by Burst Length (BL), Burst Type (BT), and Wrap Control (WC) ... 53
Table 17: No-Wrap Restrictions ... 54
Table 18: MR2 Device Feature 2 (MA[7:0] = 02h) ... 54
Table 19: MR2 Op-Code Bit Definitions ... 55
Table 20: MR3 I/O Configuration 1 (MA[7:0] = 03h) ... 55
Table 21: MR3 Op-Code Bit Definitions ... 55
Table 22: MR4 Device Temperature (MA[7:0] = 04h) ... 55
Table 23: MR4 Op-Code Bit Definitions ... 56
Table 24: MR5 Basic Configuration 1 (MA[7:0] = 05h) ... 56
Table 25: MR5 Op-Code Bit Definitions ... 56
Table 26: MR6 Basic Configuration 2 (MA[7:0] = 06h) ... 57
Table 27: MR6 Op-Code Bit Definitions ... 57
Table 28: MR7 Basic Configuration 3 (MA[7:0] = 07h) ... 57
Table 29: MR7 Op-Code Bit Definitions ... 57
Table 30: MR8 Basic Configuration 4 (MA[7:0] = 08h) ... 57
Table 31: MR8 Op-Code Bit Definitions ... 57
Table 32: MR9 Test Mode (MA[7:0] = 09h) ... 58
Table 33: MR10 Calibration (MA[7:0] = 0Ah) ... 58
Table 34: MR10 Op-Code Bit Definitions ... 58
Table 35: MR[11:15] Reserved (MA[7:0] = 0Bh–0Fh) ... 59
Table 36: MR16 PASR Bank Mask (MA[7:0] = 010h) ... 59
Table 37: MR16 Op-Code Bit Definitions ... 59
Table 38: MR17 PASR Segment Mask (MA[7:0] = 011h) ... 59
Table 39: MR17 PASR Segment Mask Definitions ... 59
Table 40: MR17 PASR Row Address Ranges in Masked Segments ... 59
Table 41: Reserved Mode Registers ... 60
Table 42: MR63 RESET (MA[7:0] = 3Fh) – MRW Only ... 60
Table 43: Bank Selection for PRECHARGE by Address Bits ... 76
Table 44: PRECHARGE and Auto Precharge Clarification ... 80
Table 45: REFRESH Command Scheduling Separation Requirements ... 82
Table 46: Bank and Segment Masking Example ... 91
Table 47: Temperature Sensor Definitions and Operating Conditions ... 95
Table 48: Data Calibration Pattern Description ... 97
Table 49: Truth Table for MRR and MRW ... 98
Table 50: Command Truth Table ... 112

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Table 51: CKE Truth Table 113
Table 52: Current State Bank *n* to Command to Bank *n* Truth Table 114
Table 53: Current State Bank *n* to Command to Bank *m* Truth Table 116
Table 54: DM Truth Table 119
Table 55: Absolute Maximum DC Ratings 120
Table 56: Input/Output Capacitance 120
Table 57: Switching for CA Input Signals 121
Table 58: Switching for I_{DD4R} 122
Table 59: Switching for I_{DD4W} 122
Table 60: I_{DD} Specification Parameters and Operating Conditions 123
Table 61: Recommended DC Operating Conditions 125
Table 62: Input Leakage Current 126
Table 63: Operating Temperature Range 126
Table 64: Single-Ended AC and DC Input Levels for CA and CS# Inputs 127
Table 65: Single-Ended AC and DC Input Levels for CKE 127
Table 66: Single-Ended AC and DC Input Levels for DQ and DM 127
Table 67: Differential AC and DC Input Levels 131
Table 68: CK/CK# and DQS/DQS# Time Requirements Before Ringback (^{t}DVAC) 132
Table 69: Single-Ended Levels for CK, CK#, DQS, DQS# 133
Table 70: Crosspoint Voltage for Differential Input Signals (CK, CK#, DQS, DQS#) 134
Table 71: Differential Input Slew Rate Definition 135
Table 72: Single-Ended AC and DC Output Levels 135
Table 73: Differential AC and DC Output Levels 136
Table 74: Single-Ended Output Slew Rate Definition 136
Table 75: Single-Ended Output Slew Rate 136
Table 76: Differential Output Slew Rate Definition 137
Table 77: Differential Output Slew Rate 138
Table 78: AC Overshoot/Undershoot Specification 138
Table 79: Output Driver DC Electrical Characteristics with ZQ Calibration 141
Table 80: Output Driver Sensitivity Definition 142
Table 81: Output Driver Temperature and Voltage Sensitivity 142
Table 82: Output Driver DC Electrical Characteristics Without ZQ Calibration 142
Table 83: I-V Curves 143
Table 84: Definitions and Calculations 146
Table 85: ^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) Definitions 147
Table 86: Refresh Requirement Parameters (Per Density) 150
Table 87: AC Timing 151
Table 88: CA and CS# Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate) 158
Table 89: CA and CS# Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate) 158
Table 90: Derating Values for AC/DC-Based ^{t}IS/^{t}IH (AC220) 159
Table 91: Derating Values for AC/DC-Based ^{t}IS/^{t}IH (AC300) 159
Table 92: Required Time for Valid Transition – ^{t}VAC > $V_{IH(AC)}$ and < $V_{IL(AC)}$ 159
Table 93: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate) 164
Table 94: Data Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate) 165
Table 95: Derating Values for AC/DC-Based ^{t}DS/^{t}DH (AC220) 165
Table 96: Derating Values for AC/DC-Based ^{t}DS/^{t}DH (AC300) 166
Table 97: Required Time for Valid Transition – ^{t}VAC > $V_{IH(AC)}$ or < $V_{IL(AC)}$ 166

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

General Description

The 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296-bits. The LPDDR2-S4 device is internally configured as an eight-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

I_{DD} Specifications

Table 5: 256 Meg x 16 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD01}	V_{DD1}	15	15	15	mA
I_{DD02}	V_{DD2}	70	70	70	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	7	6	6	
I_{DD2P1}	V_{DD1}	600	600	600	µA
I_{DD2P2}	V_{DD2}	800	800	800	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	50	50	50	
I_{DD2PS1}	V_{DD1}	600	600	600	µA
I_{DD2PS2}	V_{DD2}	800	800	800	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	50	50	50	
I_{DD2N1}	V_{DD1}	2	2	2	mA
I_{DD2N2}	V_{DD2}	30	30	30	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	7	6	6	
I_{DD2NS1}	V_{DD1}	1.7	1.7	1.7	mA
I_{DD2NS2}	V_{DD2}	27	27	27	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD3P1}	V_{DD1}	1200	1200	1200	µA
I_{DD3P2}	V_{DD2}	8	8	8	mA
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	150	150	150	µA
I_{DD3PS1}	V_{DD1}	1200	1200	1200	µA
I_{DD3PS2}	V_{DD2}	8	8	8	mA
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	150	150	150	µA
I_{DD3N1}	V_{DD1}	2.5	2.5	2.5	mA
I_{DD3N2}	V_{DD2}	30	30	30	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	7	6	6	
I_{DD3NS1}	V_{DD1}	2	2	2	mA
I_{DD3NS2}	V_{DD2}	27	27	27	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD4R1}	V_{DD1}	3	3	3	mA
I_{DD4R2}	V_{DD2}	220	194	178	
$I_{DD4R,in}$	V_{DDCA}	6	6	6	
I_{DD4W1}	V_{DD1}	10	10	10	mA
I_{DD4W2}	V_{DD2}	190	185	170	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	25	25	25	

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Table 5: 256 Meg x 16 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD51}	V_{DD1}	40	40	40	mA
I_{DD52}	V_{DD2}	150	150	150	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	8	6	6	
I_{DD5PB1}	V_{DD1}	5	5	5	mA
I_{DD5PB2}	V_{DD2}	50	50	50	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	8	8	8	
$I_{DD5PBET1}$	V_{DD1}	10.5	10.5	10.5	mA
$I_{DD5PBET2}$	V_{DD2}	80	80	80	
$I_{DD5PB,ETin}$	V_{DDCA} + V_{DDQ}	8	8	8	
I_{DD5AB1}	V_{DD1}	5	5	5	mA
I_{DD5AB2}	V_{DD2}	50	50	50	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	8	8	8	
$I_{DD5ABET1}$	V_{DD1}	10.5	10.5	10.5	mA
$I_{DD5ABET2}$	V_{DD2}	80	80	80	
$I_{DD5AB,ETin}$	V_{DDCA} + V_{DDQ}	8	8	8	
I_{DD61}	V_{DD1}	1000	1000	1000	µA
I_{DD62}	V_{DD2}	3200	3200	3200	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	50	50	50	
I_{DD6ET1}	V_{DD1}	3100	3100	3100	µA
I_{DD6ET2}	V_{DD2}	13.7	13.7	13.7	mA
$I_{DD6,ETin}$	V_{DDCA} + V_{DDQ}	90	90	90	µA
I_{DD81}	V_{DD1}	25	25	25	µA
I_{DD82}	V_{DD2}	100	100	100	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	100	100	100	

Table 6: 128 Meg x 32 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD01}	V_{DD1}	15	15	15	mA
I_{DD02}	V_{DD2}	70	70	70	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	7	6	6	
I_{DD2P1}	V_{DD1}	600	600	600	µA
I_{DD2P2}	V_{DD2}	800	800	800	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	50	50	50	

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Table 6: 128 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD2PS1}	V_{DD1}	600	600	600	µA
I_{DD2PS2}	V_{DD2}	800	800	800	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	50	50	50	
I_{DD2N1}	V_{DD1}	2	2	2	mA
I_{DD2N2}	V_{DD2}	30	30	30	mA
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	7	6	6	
I_{DD2NS1}	V_{DD1}	1.7	1.7	1.7	mA
I_{DD2NS2}	V_{DD2}	27	27	27	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD3P1}	V_{DD1}	1200	1200	1200	µA
I_{DD3P2}	V_{DD2}	8	8	8	mA
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	150	150	150	µA
I_{DD3PS1}	V_{DD1}	1200	1200	1200	µA
I_{DD3PS2}	V_{DD2}	8	8	8	mA
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	150	150	150	µA
I_{DD3N1}	V_{DD1}	2.5	2.5	2.5	mA
I_{DD3N2}	V_{DD2}	30	30	30	mA
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	7	6	6	
I_{DD3NS1}	V_{DD1}	2	2	2	mA
I_{DD3NS2}	V_{DD2}	27	27	27	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD4R1}	V_{DD1}	3	3	3	mA
I_{DD4R2}	V_{DD2}	220	194	178	
$I_{DD4R,in}$	V_{DDCA}	6	6	6	
I_{DD4W1}	V_{DD1}	10	10	10	mA
I_{DD4W2}	V_{DD2}	190	185	170	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	25	25	25	
I_{DD51}	V_{DD1}	40	40	40	mA
I_{DD52}	V_{DD2}	150	150	150	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	8	6	6	
I_{DD5PB1}	V_{DD1}	5	5	5	mA
I_{DD5PB2}	V_{DD2}	50	50	50	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	8	8	8	
$I_{DD5PBET1}$	V_{DD1}	10.5	10.5	10.5	mA
$I_{DD5PBET2}$	V_{DD2}	80	80	80	
$I_{DD5PB,ETin}$	V_{DDCA} + V_{DDQ}	8	8	8	

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Table 6: 128 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DDAB1}	V_{DD1}	5	5	5	mA
I_{DD5AB2}	V_{DD2}	50	50	50	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	8	8	8	
$I_{DDABET1}$	V_{DD1}	10.5	10.5	10.5	mA
$I_{DD5ABET2}$	V_{DD2}	80	80	80	
$I_{DD5AB,ETin}$	V_{DDCA} + V_{DDQ}	8	8	8	
I_{DD61}	V_{DD1}	1000	1000	1000	µA
I_{DD62}	V_{DD2}	3200	3200	3200	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	50	50	50	
I_{DD6ET1}	V_{DD1}	3100	3100	3100	µA
I_{DD6ET2}	V_{DD2}	13.7	13.7	13.7	mA
$I_{DD6,ETin}$	V_{DDCA} + V_{DDQ}	90	90	90	µA
I_{DD81}	V_{DD1}	25	25	25	µA
I_{DD82}	V_{DD2}	100	100	100	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	100	100	100	

Table 7: I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value (–30˚C to +85˚C)	Value (+85˚C to +105˚C)	Unit
Full array	V_{DD1}	1000	3100	µA
	V_{DD2}	3.2	13.7	mA
	V_{DDi}	50	90	µA
1/2 array	V_{DD1}	950	2200	
	V_{DD2}	2700	7300	
	V_{DDi}	50	90	
1/4 array	V_{DD1}	900	1600	
	V_{DD2}	2400	4300	
	V_{DDi}	50	90	
1/8 array	V_{DD1}	850	1300	
	V_{DD2}	2000	2800	
	V_{DDi}	50	90	

Note: 1. LPDDR2-S4 SDRAM devices support both bank masking and segment masking. I_{DD6} PASR currents are measured using bank masking only.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 2: V_{DD1} Typical Self Refresh Current vs. Temperature

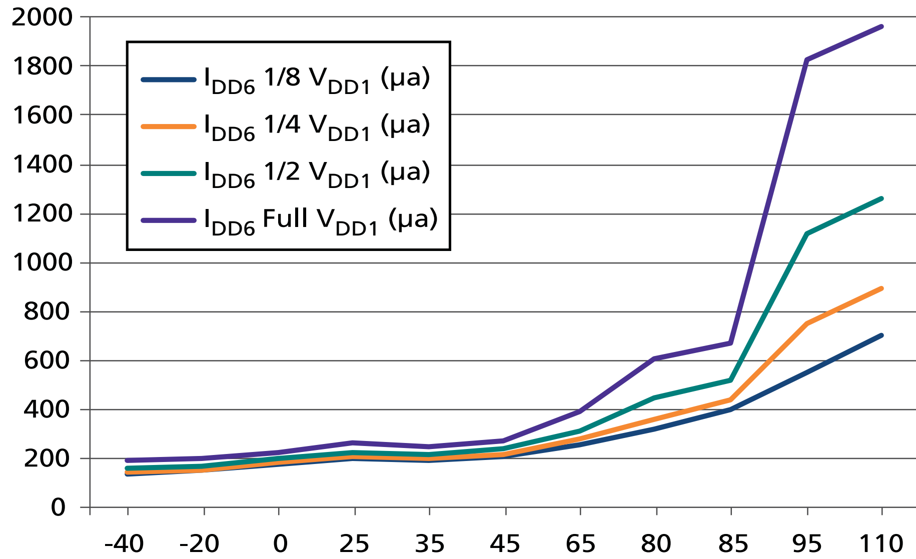
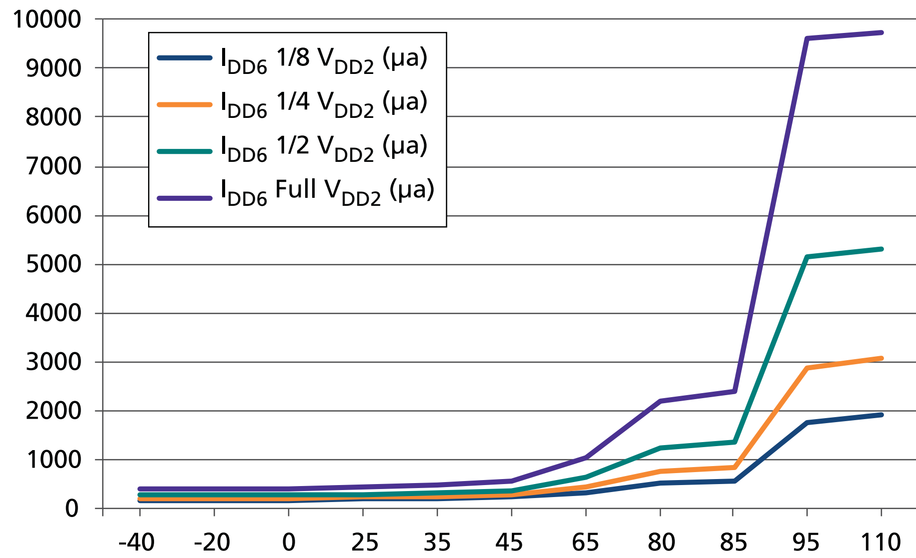


Figure 3: V_{DD2} Typical Self Refresh Current vs. Temperature



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Package Block Diagrams

Figure 4: Single Rank, Single Channel Package Block Diagram

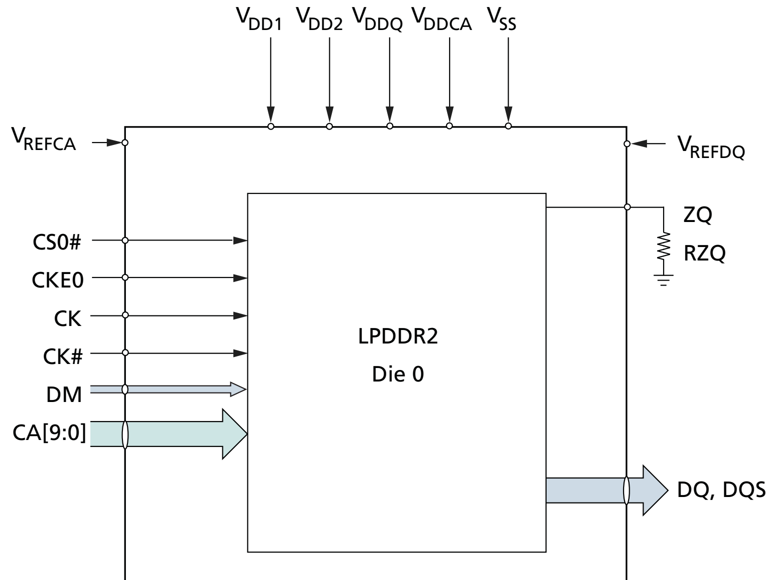
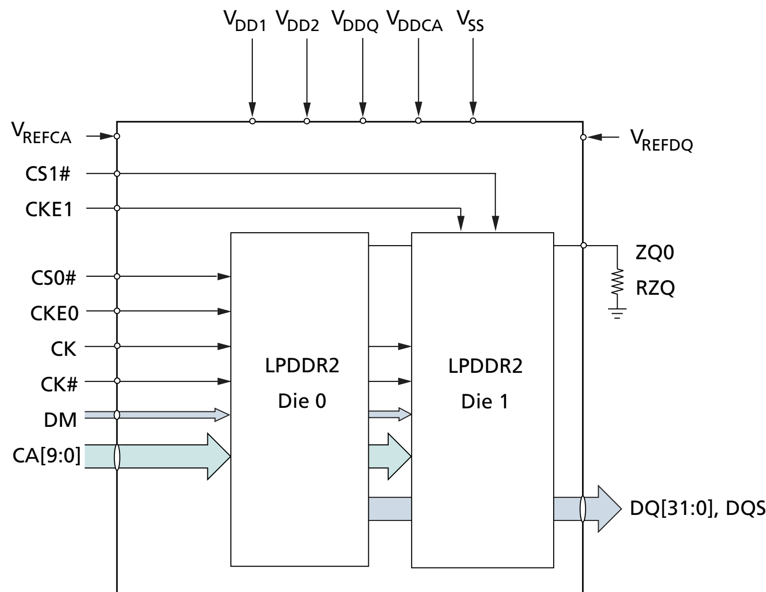


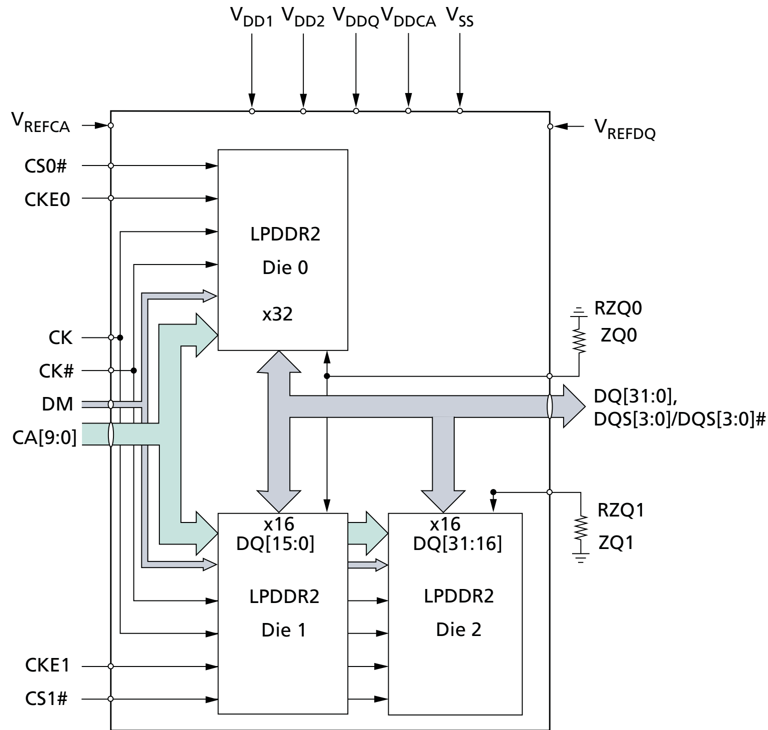
Figure 5: Dual Rank, Single Channel Package Block Diagram



Note: 1. For the 168-ball JEDEC PoP ballout employing only a single ZQ connection, the RZQ resistor is connected to ZQ.

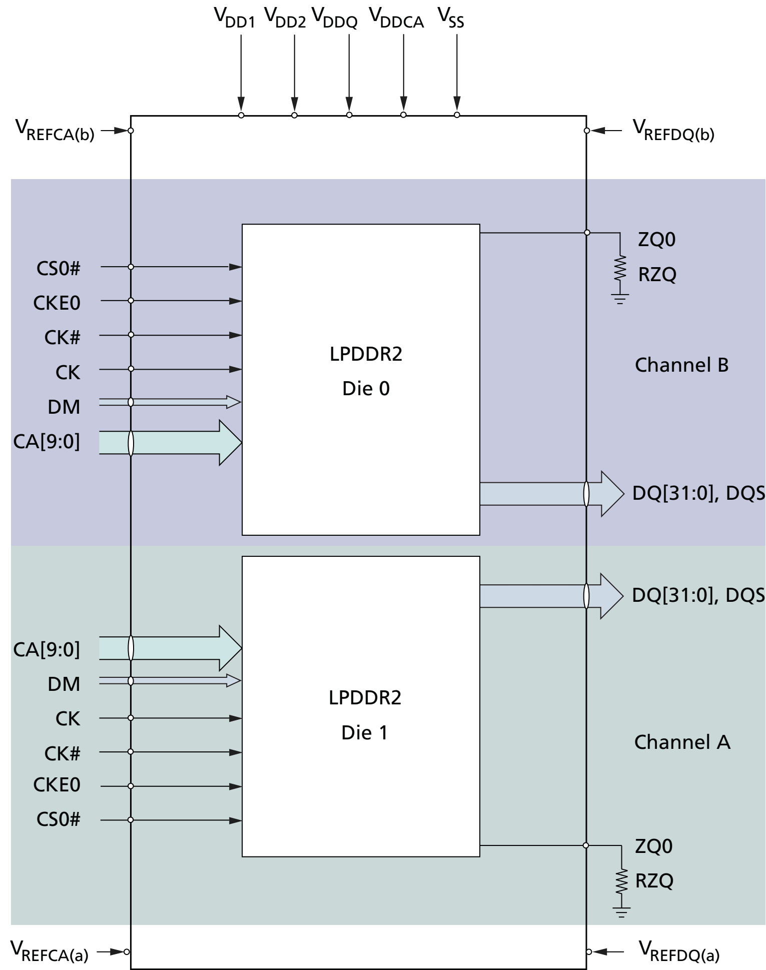
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 6: Dual Rank, Single Channel (3 Die) Package Block Diagram



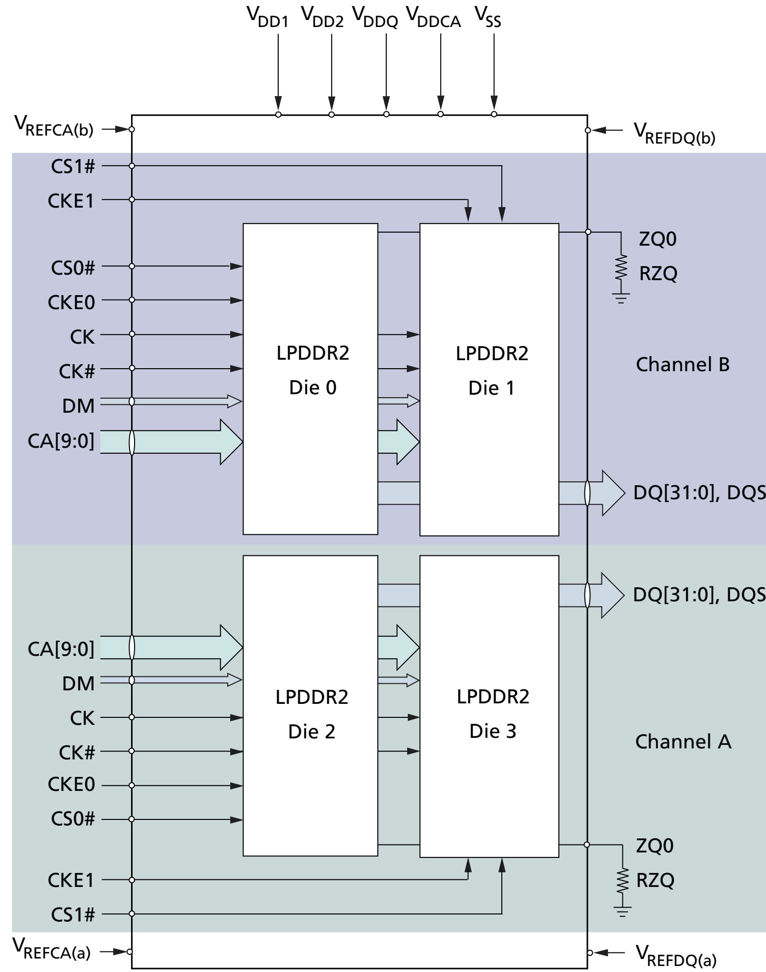
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 7: Single Rank, Dual Channel Package Block Diagram



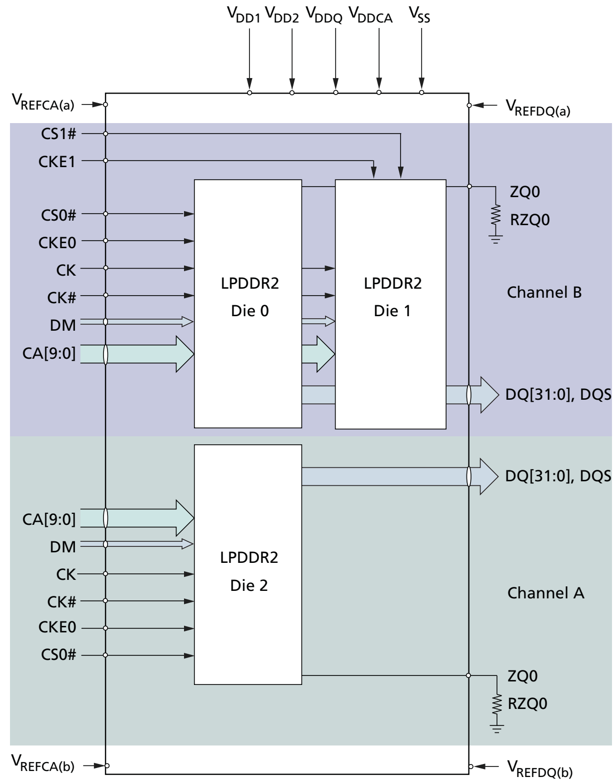
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 8: Dual Rank, Dual Channel Package Block Diagram



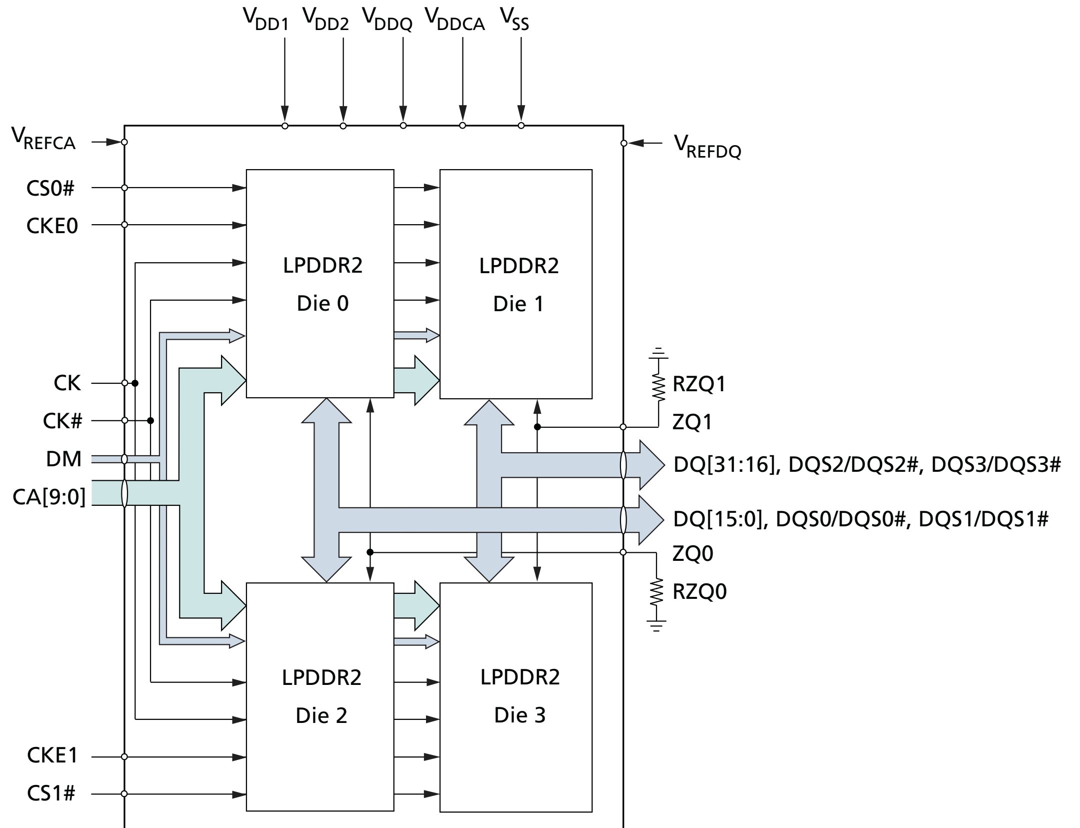
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 9: Dual Rank, Dual Channel (3 Die) Package Block Diagram



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

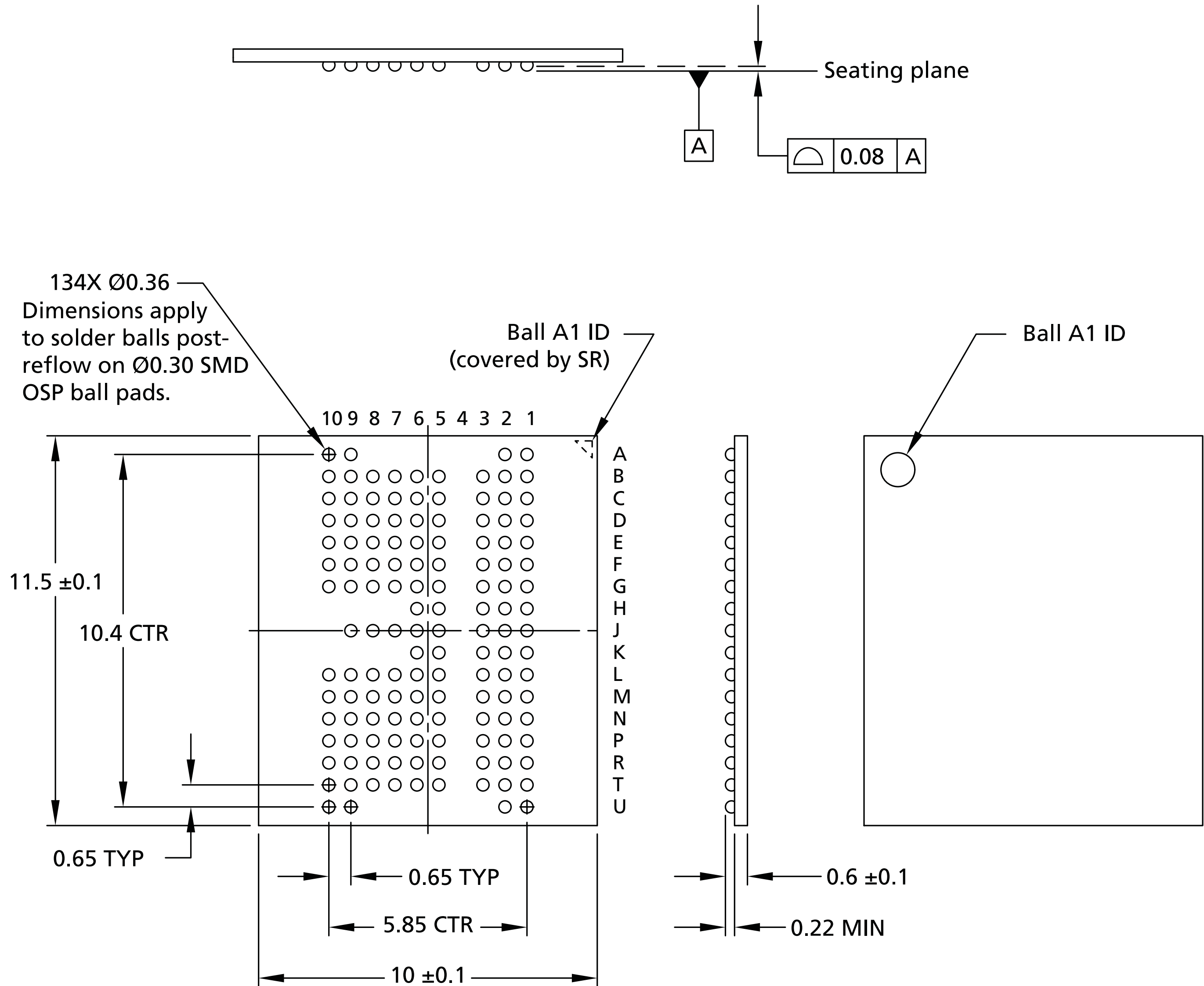
Figure 10: Dual Rank, Single Channel (4 Die) Package Block Diagram



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Package Dimensions

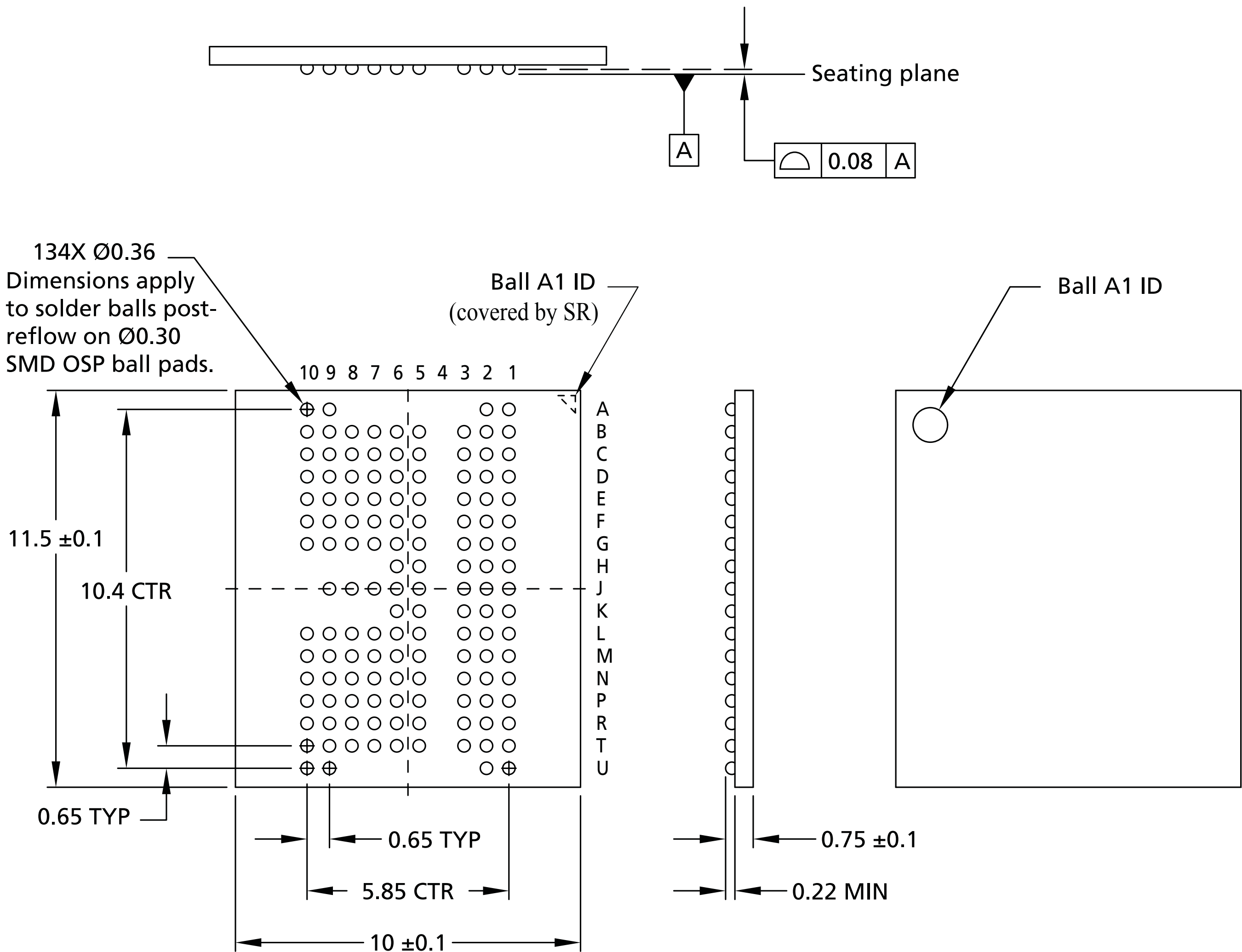
Figure 11: 134-Ball FBGA – 10mm x 11.5mm Single-Die (Package Code GU)



Note: 1. All dimensions are in millimeters.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.

Figure 12: 134-Ball FBGA – 10mm x 11.5mm Dual-Die (Package Code GV)



Note: 1. All dimensions are in millimeters.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2011 Micron Technology, Inc. All rights reserved.