Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Mobile LPDDR2 SDRAM

MT42L128M16D1, MT42L64M32D1, MT42L64M64D2, MT42L128M32D2, MT42L256M32D4, MT42L128M64D4 MT42L96M64D3, MT42L192M32D3

Features

- Ultra low-voltage core and I/O power supplies
  - V_{DD2} = 1.14–1.30V
  - V_{DDCA}/V_{DDQ} = 1.14–1.30V
  - V_{DD1} = 1.70–1.95V
- Clock frequency range
  - 533–10 MHz (data rate range: 1066–20 Mb/s/pin)
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Per-bank refresh for concurrent operation
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- RoHS-compliant, "green" packaging

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL	^{t}RCD/^{t}RP[1]
-18[2]	533	1066	8	4	Typical
-25	400	800	6	3	Typical
-3	333	667	5	2	Typical

Options	Marking
• V_{DD2}: 1.2V	L
• Configuration	
– 16 Meg x 16 x 8 banks x 1 die	128M16
– 8 Meg x 32 x 8 banks x 1 die	64M32
– 8 Meg x 32 x 8 banks x 2 die	128M32
– 16 Meg x 16 x 8 banks x 4 die	256M32
– 8 Meg x 32 x 8 banks x 2 die	64M64
– 8 Meg x 32 x 8 banks x 3 die	96M64
– 8 Meg x 32 x 8 banks x 4 die	128M64
– 16 Meg x 16 x 8 banks x 2 die + 8 Meg x 32 x 8 banks x 1 die	192M32
• Device type	
– LPDDR2-S4, 1 die in package	D1
– LPDDR2-S4, 2 die in package	D2
– LPDDR2-S4, 3 die in package	D3
– LPDDR2-S4, 4 die in package	D4
• FBGA"green" package	
– 134-ball FBGA (11mm x 11.5mm)	MH
– 134-ball FBGA (11.5mm x 11.5mm)	MG
– 168-ball FBGA (12mm x 12mm)	KL
– 168-ball FBGA (12mm x 12mm)	LE
– 168-ball FBGA (12mm x 12mm)	KP
– 216-ball FBGA (12mm x 12mm)	KH
– 216-ball FBGA (12mm x 12mm)	KJ
– 216-ball FBGA (12mm x 12mm)	KU
– 220-ball FBGA (14mm x 14mm)	MP
– 220-ball FBGA (14mm x 14mm)	LD
• Timing – cycle time	
– 1.875ns @ RL = 8	-18[2]
– 2.5ns @ RL = 6	-25
– 3.0ns @ RL = 5	-3
• Operating temperature range	
– From –25°C to +85°C	IT
– From –40°C to +105°C	AT
• Revision	:A

Notes: 1. For fast ^{t}RCD/^{t}RP, contact factory.
2. For -18 speed grade, contact factory.

Table 2: Single Channel S4 Configuration Addressing

Architecture		128 Meg x 16 Figure 3 (page 16)	64 Meg x 32 Figure 3 (page 16)	128 Meg x 32 Figure 4 (page 17)	192 Meg x 32 Figure 6 (page 19)	256 Meg x 32 Figure 9 (page 22)
Die configuration	CS0#	16 Meg x 16 x 8 banks	8 Meg x 32 x 8 banks	8 Meg x 32 x 8 banks	16 Meg x 16 x 8 banks x 2	16 Meg x 16 x 8 banks x 2
	CS1#	na	na	8 Meg x 32 x 8 banks	8 Meg x 32 x 8 banks	16 Meg x 16 x 8 banks x 2
Row addressing		16K (A[13:0])	16K (A[13:0])	16K (A[13:0])	16K (A[13:0])	16K (A[13:0])
Column addressing	CS0#	1K (A[9:0])	512 (A[8:0])	512 (A[8:0])	1K (A[9:0])	1K (A[9:0])
	CS1#	na	na	512 (A[8:0])	512 (A[8:0])	1K (A[9:0])
Number of die		1	1	2	3	4
Die per rank (CS#)	CS0#	1	1	1	2	2
	CS1#	0	0	1	1	2
Ranks per channel [1]		1	1	2	2	2

Table 3: Dual Channel S4 Configuration Addressing

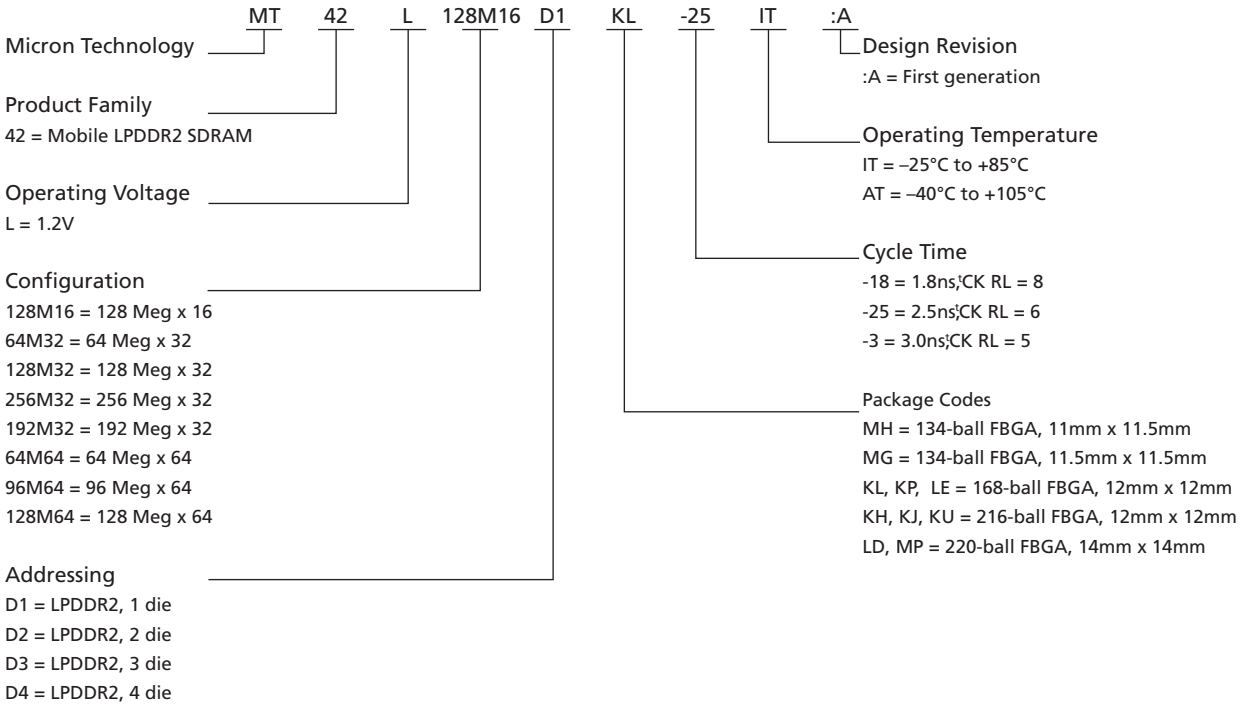
Architecture		64 Meg x 64 Figure 5 (page 18)	96 Meg x 64 Figure 8 (page 21)	128 Meg x 64 Figure 7 (page 20)
Die configuration		8 Meg x 32 x 8 banks	8 Meg x 32 x 8 banks	8 Meg x 32 x 8 banks
Row addressing		16K (A[13:0])	16K (A[13:0])	16K (A[13:0])
Column addressing	CS0#	512 (A[8:0])	512 (A[8:0])	512 (A[8:0])
	CS1#	na	512 (A[8:0])	512 (A[8:0])
Number of die		2	3	4
Die per rank (CS#)	CS0#	1	1	1
	CS1#	0	1-chan A, 0-chan B	1
Ranks per channel [1]	Channel A	1	2	2
	Channel B	1	1	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

See Package Block Diagrams (page 16) for descriptions of signal connections and die configurations for each respective architecture.

Part Numbering

Figure 1: 2Gb LPDDR2 Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Contents

List of Figures

List of Tables

General Description

The 2Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 2,147,483,648 bits. The LPDDR2-S4 device is internally configured as an eight-bank DRAM. Each of the x16's 268,435,456-bit banks is organized as 16,384 rows by 1024 columns by 16 bits. Each of the x32's 268,435,456-bit banks is organized as 16,384 rows by 512 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

I_{DD} Specifications

Table 4: 128 Meg x 16 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD01}	V_{DD1}	20	20	20	mA
I_{DD02}	V_{DD2}	65	50	47	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD2P1}	V_{DD1}	500	500	500	µA
I_{DD2P2}	V_{DD2}	1600	1600	1600	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	100	100	100	
I_{DD2PS1}	V_{DD1}	500	500	500	µA
I_{DD2PS2}	V_{DD2}	1600	1600	1600	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	100	100	100	
I_{DD2N1}	V_{DD1}	1.7	1.7	1.7	mA
I_{DD2N2}	V_{DD2}	16	15	15	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD2NS1}	V_{DD1}	1.7	1.7	1.7	mA
I_{DD2NS2}	V_{DD2}	16	15	15	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD3P1}	V_{DD1}	1200	1200	1200	µA
I_{DD3P2}	V_{DD2}	4	4	4	mA
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	120	120	120	µA
I_{DD3PS1}	V_{DD1}	1200	1200	1200	µA
I_{DD3PS2}	V_{DD2}	4	4	4	mA
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	120	120	120	µA
I_{DD3N1}	V_{DD1}	1.2	1.2	1.2	mA
I_{DD3N2}	V_{DD2}	24	23	23	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD3NS1}	V_{DD1}	1.2	1.2	1.2	mA
I_{DD3NS2}	V_{DD2}	24	23	23	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD4R1}	V_{DD1}	5	5	5	mA
I_{DD4R2}	V_{DD2}	220	210	200	
$I_{DD4R,in}$	V_{DDCA}	6	6	6	
I_{DD4W1}	V_{DD1}	10	10	10	mA
I_{DD4W2}	V_{DD2}	180	175	175	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	28	28	28	

Table 4: 128 Meg x 16 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD51}	V_{DD1}	15	15	15	mA
I_{DD52}	V_{DD2}	130	130	130	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD5PB1}	V_{DD1}	5	5	5	mA
I_{DD5PB2}	V_{DD2}	18	18	18	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD5AB1}	V_{DD1}	5	5	5	mA
I_{DD5AB2}	V_{DD2}	18	18	18	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD61}	V_{DD1}	1200	1200	1200	µA
I_{DD62}	V_{DD2}	2500	2500	2500	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	100	100	100	
I_{DD81}	V_{DD1}	7.5	7.5	7.5	µA
I_{DD82}	V_{DD2}	30	30	30	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	15	15	15	

Table 5: 64 Meg x 32 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD01}	V_{DD1}	20	20	20	mA
I_{DD02}	V_{DD2}	65	50	47	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD2P1}	V_{DD1}	500	500	500	µA
I_{DD2P2}	V_{DD2}	1600	1600	1600	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	100	100	100	
I_{DD2PS1}	V_{DD1}	500	500	500	µA
I_{DD2PS2}	V_{DD2}	1600	1600	1600	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	100	100	100	
I_{DD2N1}	V_{DD1}	1.7	1.7	1.7	mA
I_{DD2N2}	V_{DD2}	16	15	15	mA
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD2NS1}	V_{DD1}	1.7	1.7	1.7	mA
I_{DD2NS2}	V_{DD2}	16	15	15	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD3P1}	V_{DD1}	1200	1200	1200	µA

Table 5: 64 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

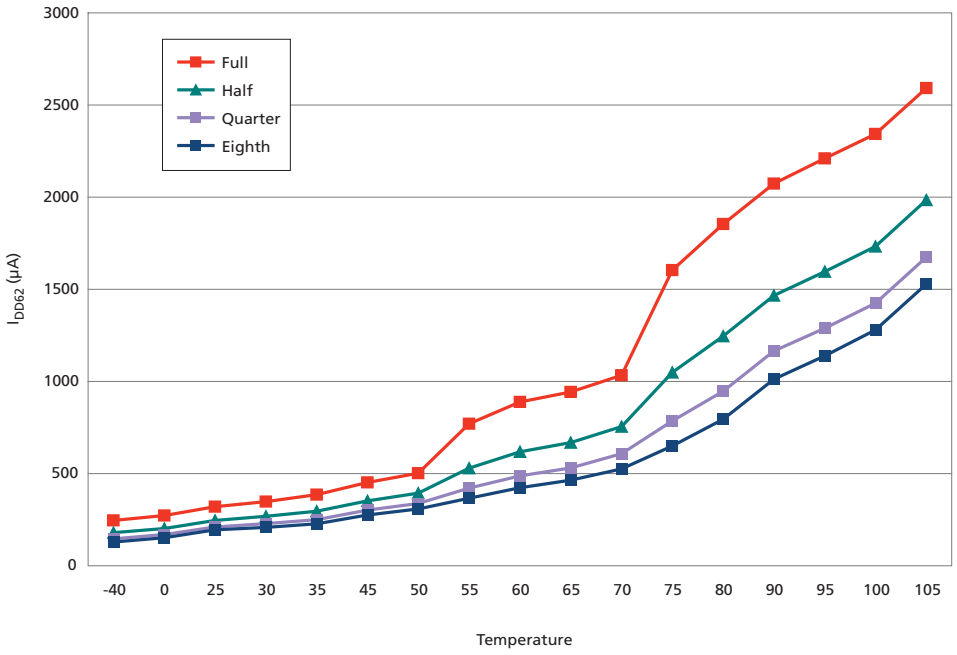
Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD3P2}	V_{DD2}	4	4	4	mA
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	120	120	120	µA
I_{DD3PS1}	V_{DD1}	1200	1200	1200	µA
I_{DD3PS2}	V_{DD2}	4	4	4	mA
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	120	120	120	µA
I_{DD3N1}	V_{DD1}	1.2	1.2	1.2	mA
I_{DD3N2}	V_{DD2}	24	23	23	mA
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD3NS1}	V_{DD1}	1.2	1.2	1.2	mA
I_{DD3NS2}	V_{DD2}	24	23	23	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD4R1}	V_{DD1}	5	5	5	mA
I_{DD4R2}	V_{DD2}	220	210	200	
$I_{DD4R,in}$	V_{DDCA}	6	6	6	
I_{DD4W1}	V_{DD1}	10	10	10	mA
I_{DD4W2}	V_{DD2}	185	175	175	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	28	28	28	
I_{DD51}	V_{DD1}	15	15	15	mA
I_{DD52}	V_{DD2}	130	130	130	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD5PB1}	V_{DD1}	5	5	5	mA
I_{DD5PB2}	V_{DD2}	18	18	18	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DDAB1}	V_{DD1}	5	5	5	mA
I_{DD5AB2}	V_{DD2}	18	18	18	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD61}	V_{DD1}	1200	1200	1200	µA
I_{DD62}	V_{DD2}	2500	2500	2500	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	100	100	100	
I_{DD81}	V_{DD1}	7.5	7.5	7.5	µA
I_{DD82}	V_{DD2}	30	30	30	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	15	15	15	

Table 6: I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit
Full array	V_{DD1}	1200	µA
	V_{DD2}	2500	
	V_{DDi}	75	
1/2 array	V_{DD1}	1000	
	V_{DD2}	2000	
	V_{DDi}	75	
1/4 array	V_{DD1}	900	
	V_{DD2}	1700	
	V_{DDi}	75	
1/8 array	V_{DD1}	900	
	V_{DD2}	1500	
	V_{DDi}	75	

Figure 2: Typical Self-Refresh Current vs. Temperature



Package Block Diagrams

Figure 3: Single Rank, Single Channel Package Block Diagram

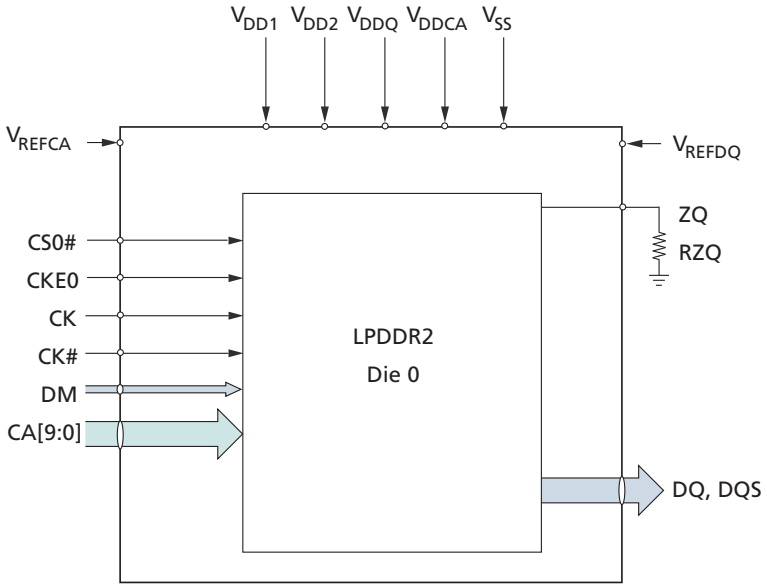
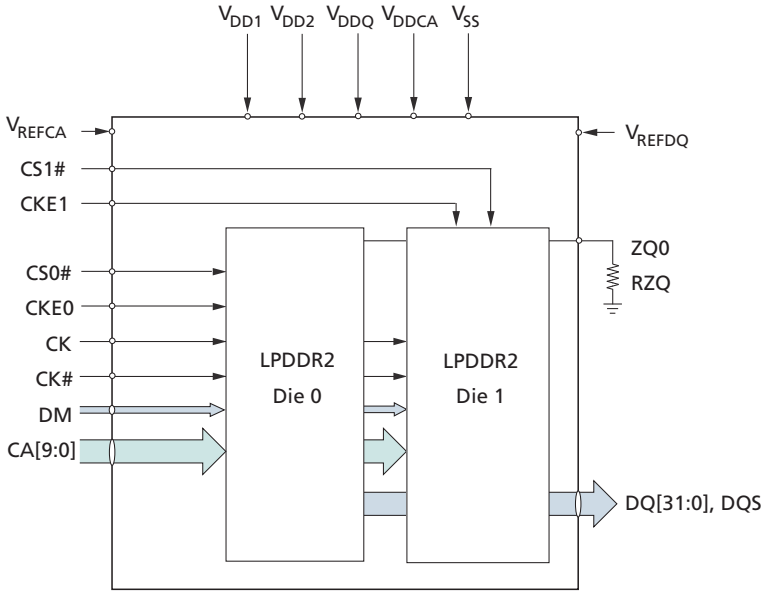


Figure 4: Dual Rank, Single Channel Package Block Diagram



Note: 1. For the 168-ball JEDEC PoP ballout employing only a single ZQ connection, the RZQ resistor is connected to ZQ.

Figure 5: Single Rank, Dual Channel Package Block Diagram

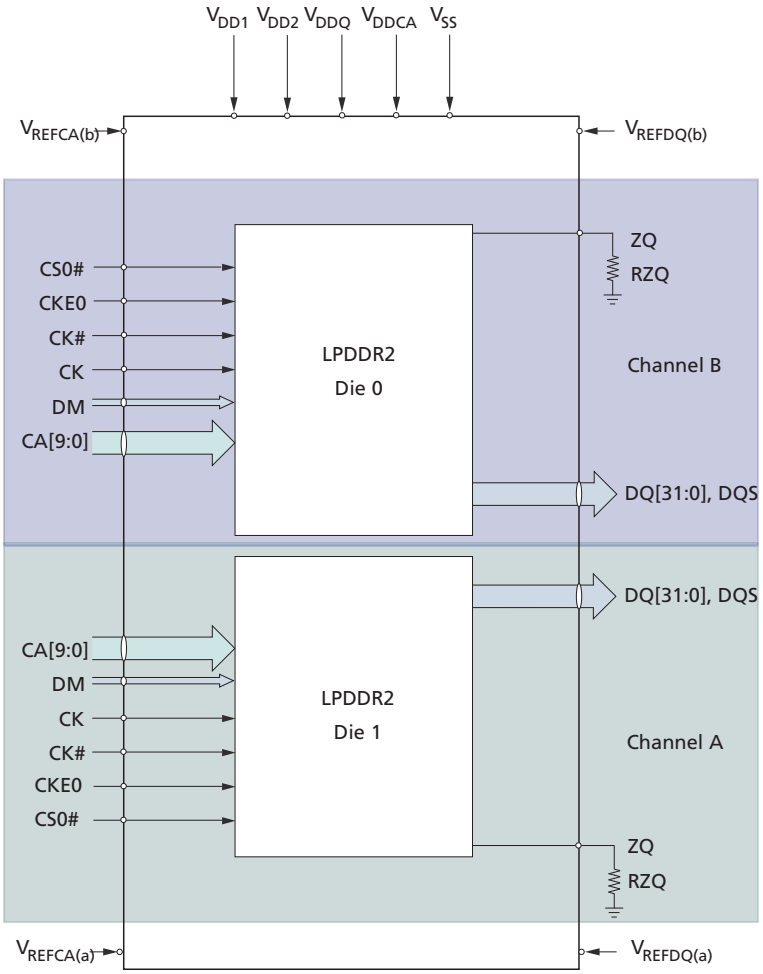


Figure 6: Dual Rank, Single Channel (3 Die) Package Block Diagram

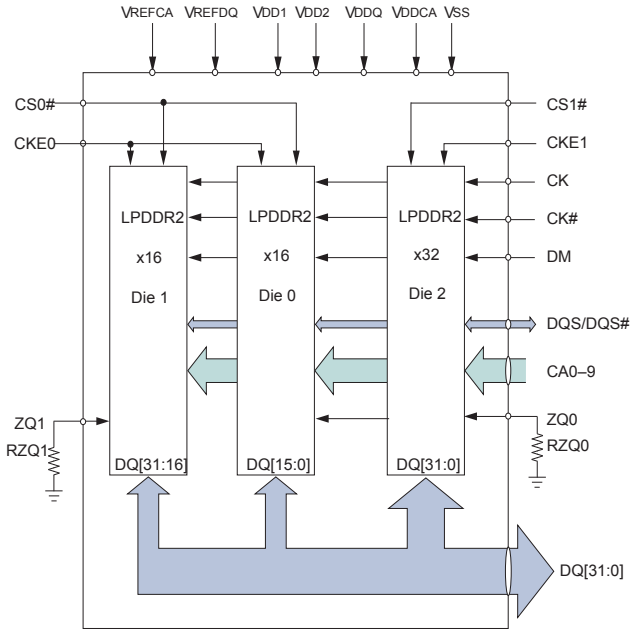


Figure 7: Dual Rank, Dual Channel Package Block Diagram

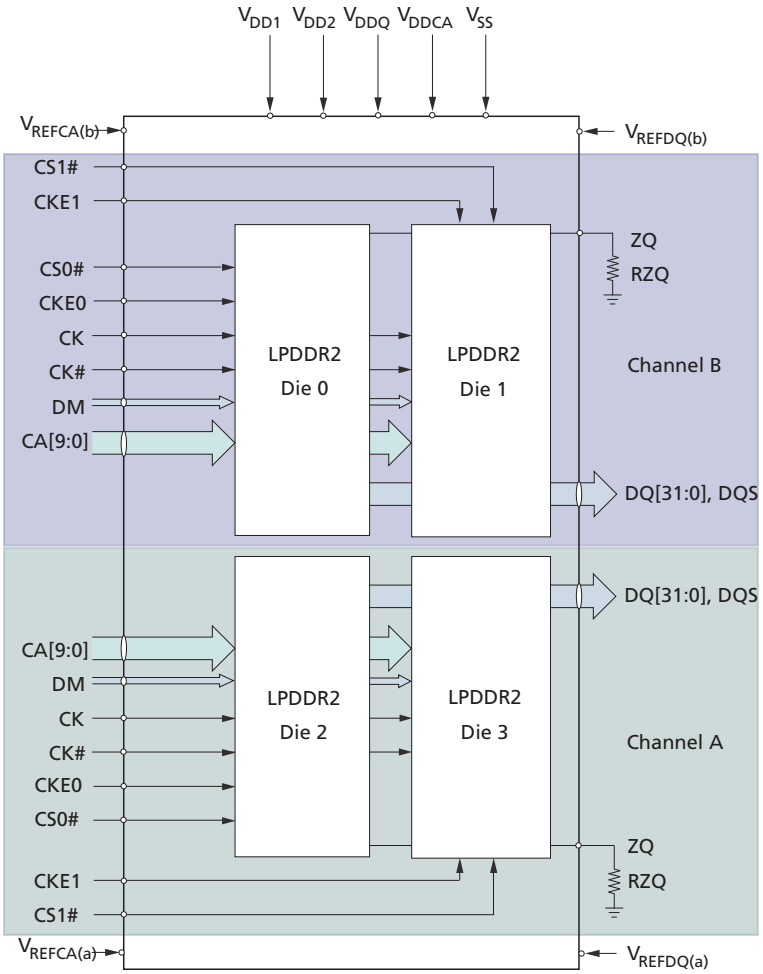


Figure 8: Dual Rank, Dual Channel (3 Die) Package Block Diagram

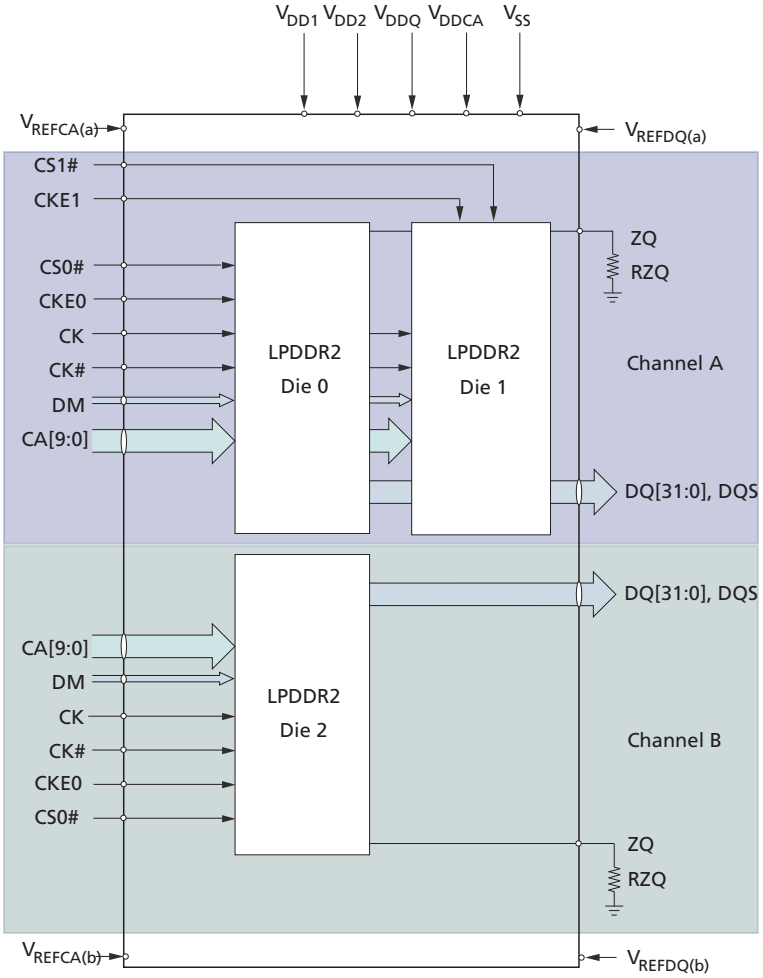
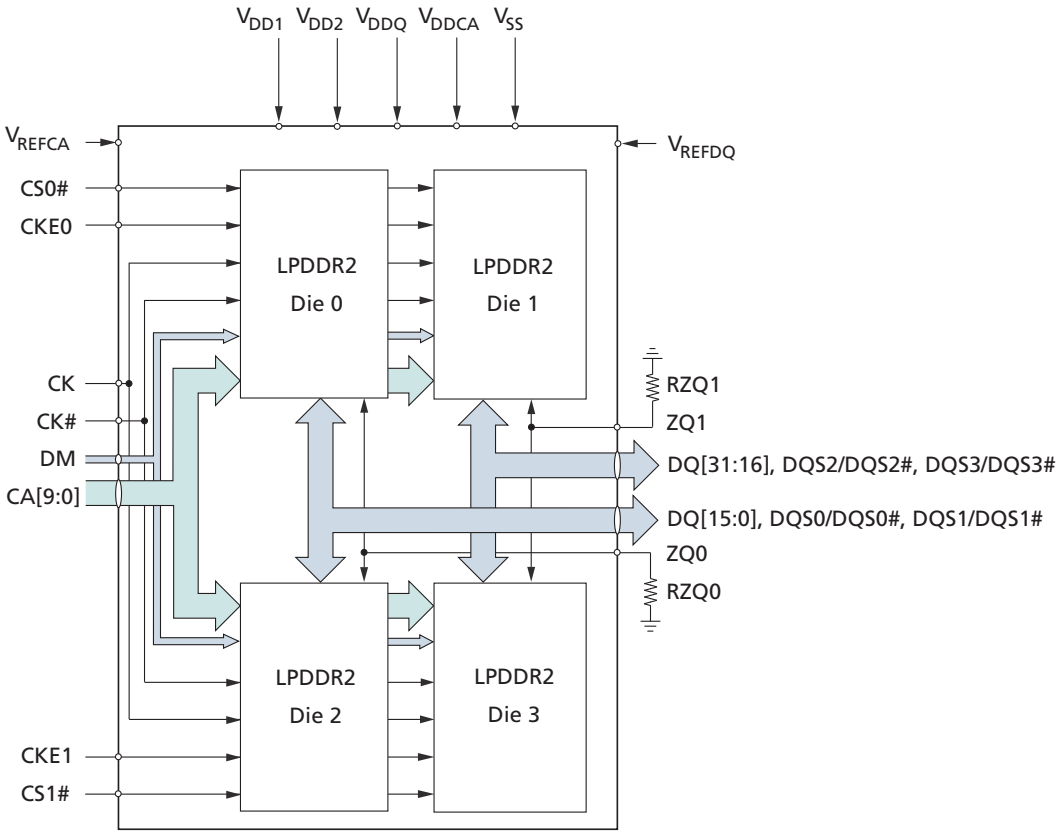
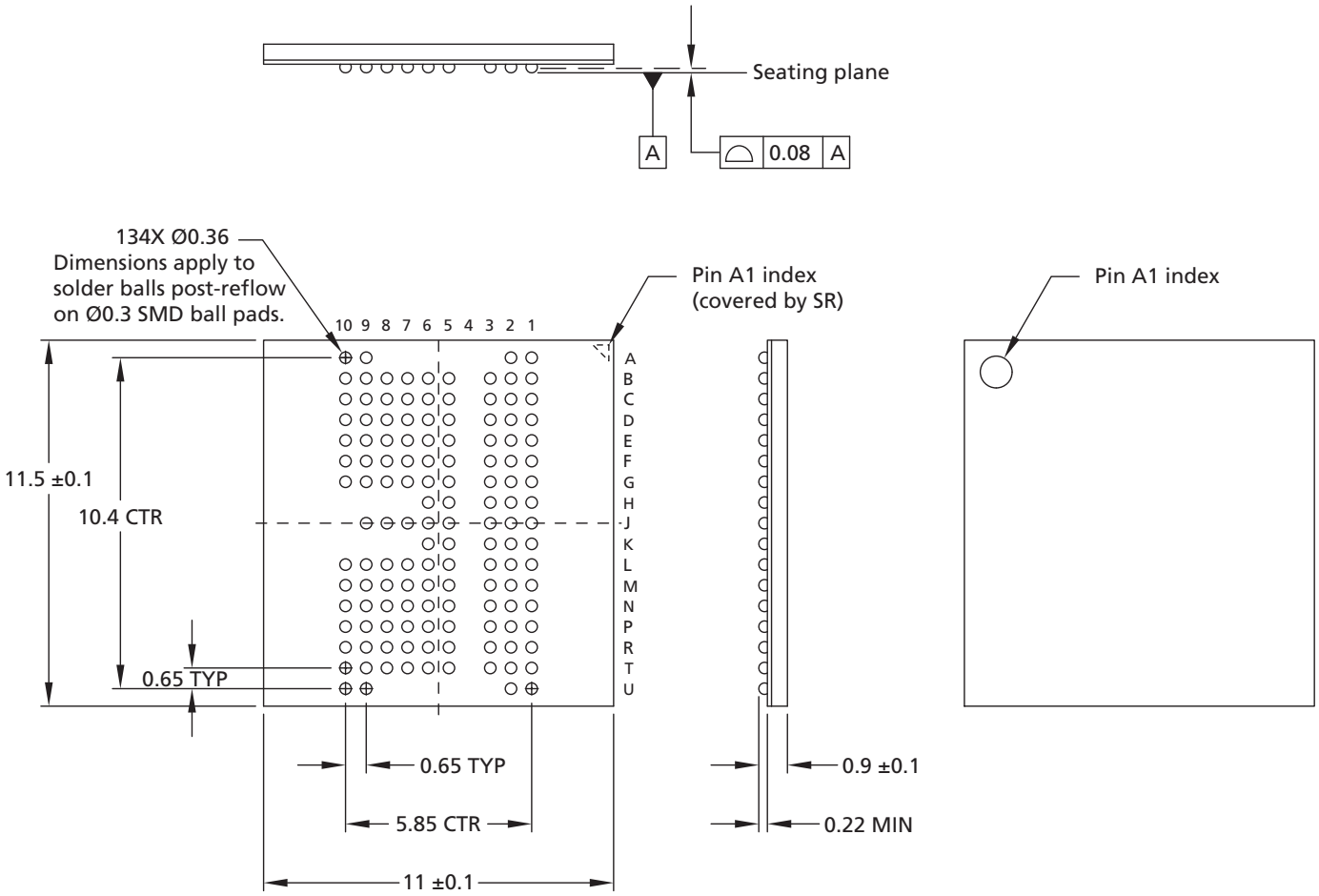


Figure 9: Dual Rank, Single Channel (4 Die) Package Block Diagram



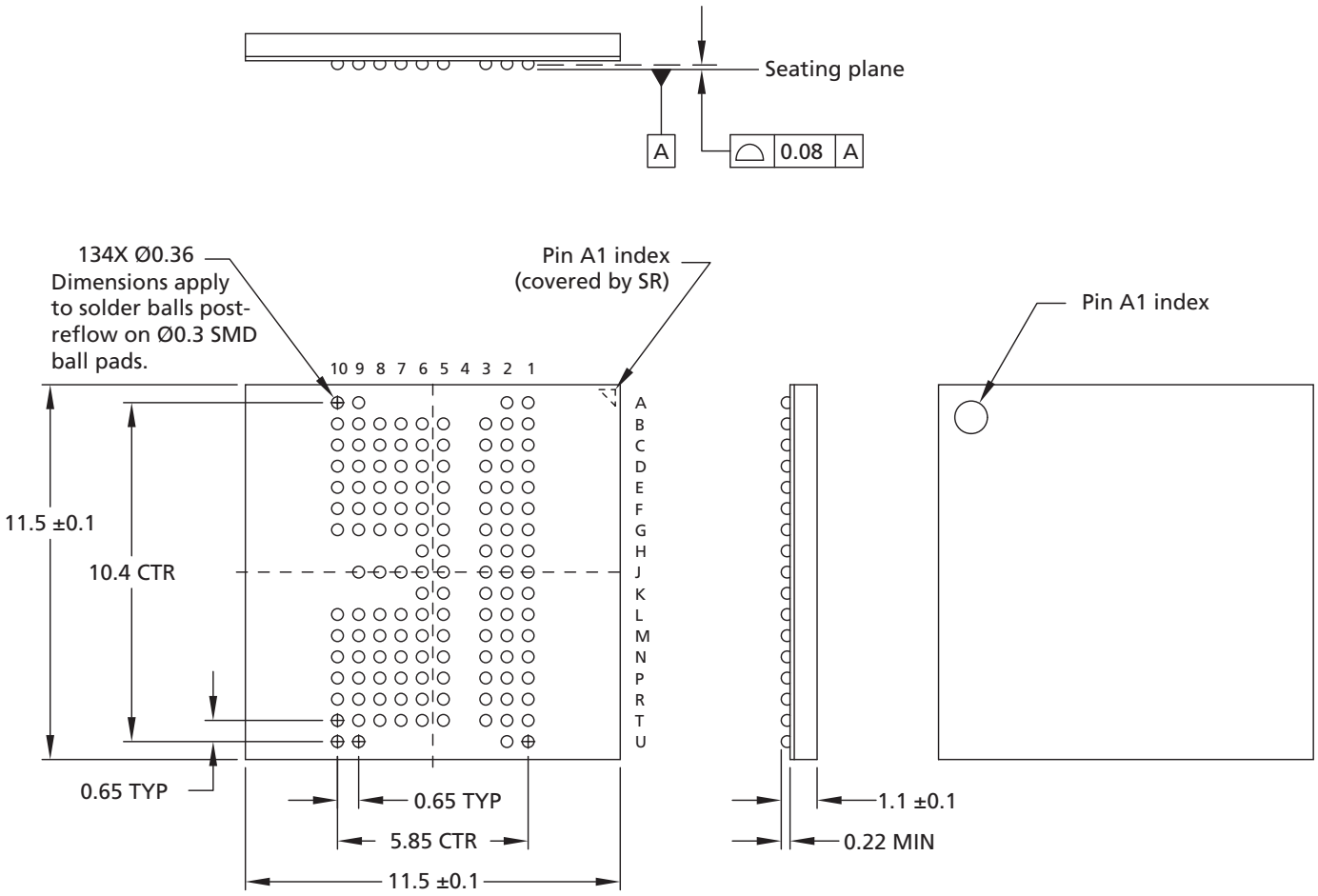
Package Dimensions

Figure 10: 134-Ball FBGA – 11mm x 11.5mm (Package Code MH)



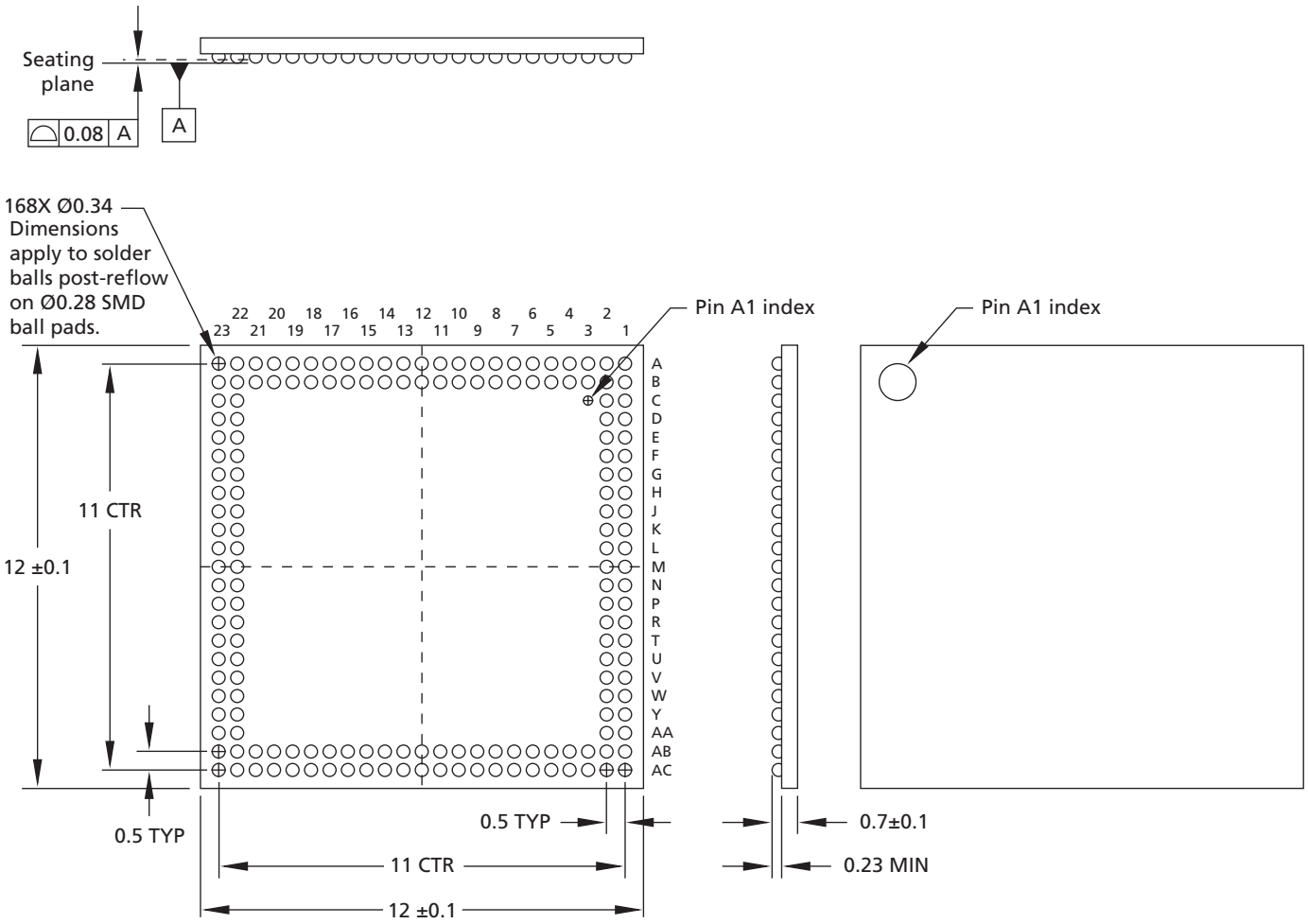
Notes:
1. All dimensions are in millimeters.
2. Solder ball material: LF35 (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).

Figure 11: 134-Ball FBGA – 11.5mm x 11.5mm (Package Code MG)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: LF35 (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).

Figure 12: 168-Ball FBGA – 12mm x 12mm (Package Code KL)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu).