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Automotive Mobile LPDDR2 SDRAM

MT42L32M16D1, MT42L32M32D2, MT42L16M32D1

Features

- Ultra low-voltage core and I/O power supplies
  - V_{DD2} = 1.14–1.30V
  - V_{DDCA}/V_{DDQ} = 1.14–1.30V
  - V_{DD1} = 1.70–1.95V
- Clock frequency range
  - 400–10 MHz (data rate range: 800–20 Mb/s/pin)
- Four-bit prefetch DDR architecture
- Four internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- RoHS-compliant, "green" packaging

Options	Marking
• V_{DD2}: 1.2V	L
• Configuration	
– 4 Meg x 32 x 4 banks	16M32
– 8 Meg x 16 x 4 banks	32M16
– 2 x 8 Meg x 16 x 4 banks	32M32
• Device type	
– LPDDR2-S4, 1 die in package	D1
– LPDDR2-S4, 2 die in package	D2
• FBGA "green" package	
– 121-ball FBGA (6.5mm x 8mm)	AB/FE
– 134-ball FBGA (10mm x 11.5mm)	AC
– 168-ball FBGA (12mm x 12mm)	LG
• Timing – cycle time	
– 2.5ns @ RL = 6	-25
– 3.0ns @ RL = 5	-3
• Automotive certified	
– Package-level burn-in	A
• Operating temperature range	
– From –40°C to +85°C	IT
– From –40°C to +105°C	AT
• Revision	:A

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL	^{t}RCD/^{t}RP
-25	400	800	6	3	Typical
-3	333	667	5	2	Typical

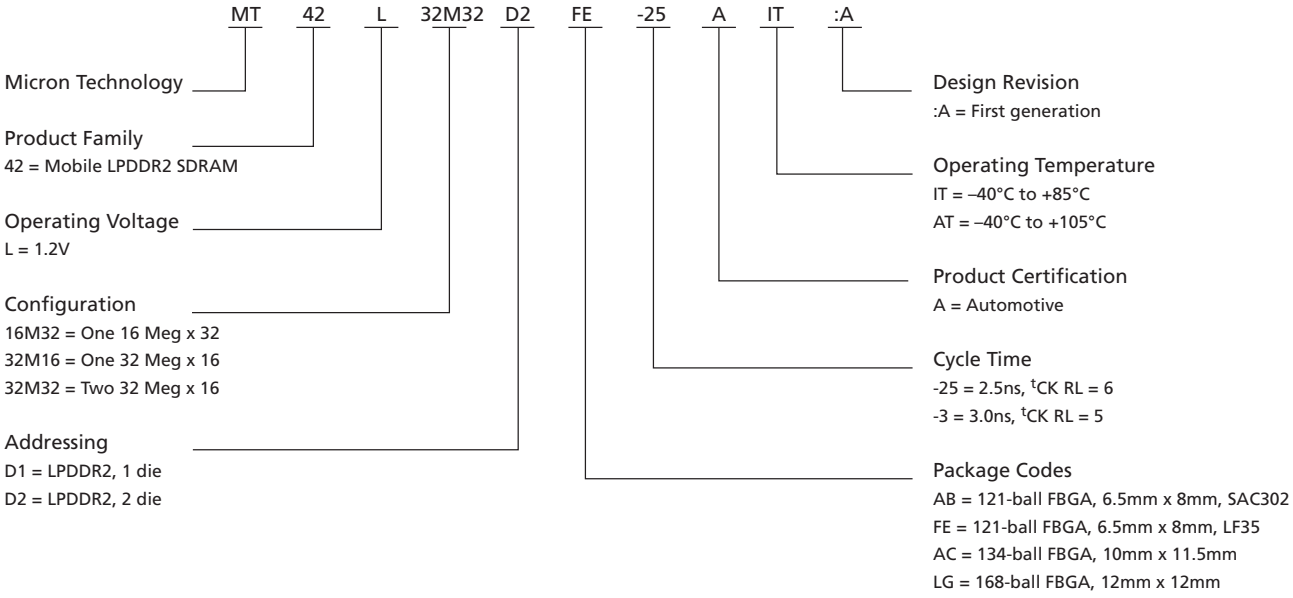
Table 2: S4 Configuration Addressing

Architecture	16 Meg x 32	32 Meg x 16	32 Meg x 32
Die configuration	4 Meg x 32 x 4 banks	8 Meg x 16 x 4 banks	2 x 8 Meg x 16 x 4 banks
Row addressing	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Column addressing	512 (A[8:0])	1K (A[9:0])	1K (A[9:0])
Number of die	1	1	2
Number of channels	1	1	1
Die per rank	1	1	2
Ranks per channel	1	1	1

See Package Block Diagrams for descriptions of signal connections and die configurations for each respective architecture.

Part Numbering

Figure 1: 512Mb LPDDR2 Part Numbering



Contents

List of Figures

List of Tables

General Description

The 512Mb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. The LPDDR2-S4 device is internally configured as an four-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

I_{DD} Specifications

Table 3: 16 Meg x 32 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I_{DD01}	V_{DD1}	9	9	mA
I_{DD02}	V_{DD2}	28	28	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD2P1}	V_{DD1}	200	200	µA
I_{DD2P2}	V_{DD2}	500	500	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	75	75	
I_{DD2PS1}	V_{DD1}	200	200	µA
I_{DD2PS2}	V_{DD2}	500	500	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	75	75	
I_{DD2N1}	V_{DD1}	2	2	mA
I_{DD2N2}	V_{DD2}	10	10	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD2NS1}	V_{DD1}	0.7	0.7	mA
I_{DD2NS2}	V_{DD2}	2.5	2.5	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	6	6	
I_{DD3P1}	V_{DD1}	750	750	µA
I_{DD3P2}	V_{DD2}	4	4	mA
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	240	240	µA
I_{DD3PS1}	V_{DD1}	750	750	µA
I_{DD3PS2}	V_{DD2}	4	4	mA
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	240	240	µA
I_{DD3N1}	V_{DD1}	0.7	0.7	mA
I_{DD3N2}	V_{DD2}	12	12	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD3NS1}	V_{DD1}	0.7	0.7	mA
I_{DD3NS2}	V_{DD2}	2.5	2.5	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	6	6	
I_{DD4R1}	V_{DD1}	2	2	mA
I_{DD4R2}	V_{DD2}	165	165	
$I_{DD4R,in}$	V_{DDCA}	10	10	
I_{DD4W1}	V_{DD1}	2	2	mA
I_{DD4W2}	V_{DD2}	130	130	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	50	50	

Table 3: 16 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I_{DD51}	V_{DD1}	22	22	mA
I_{DD52}	V_{DD2}	60	60	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD5AB1}	V_{DD1}	1.2	1.2	mA
I_{DD5AB2}	V_{DD2}	12	12	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD61}	V_{DD1}	500	500	µA
I_{DD62}	V_{DD2}	2000	2000	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	50	50	
I_{DD81}	V_{DD1}	25	25	µA
I_{DD82}	V_{DD2}	60	60	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	25	25	

Table 4: 32 Meg x 16 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I_{DD01}	V_{DD1}	9	9	mA
I_{DD02}	V_{DD2}	28	28	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD2P1}	V_{DD1}	200	200	µA
I_{DD2P2}	V_{DD2}	500	500	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	75	75	
I_{DD2PS1}	V_{DD1}	200	200	µA
I_{DD2PS2}	V_{DD2}	500	500	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	75	75	
I_{DD2N1}	V_{DD1}	2	2	mA
I_{DD2N2}	V_{DD2}	10	10	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD2NS1}	V_{DD1}	0.7	0.7	mA
I_{DD2NS2}	V_{DD2}	2.5	2.5	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	6	6	
I_{DD3P1}	V_{DD1}	750	750	µA
I_{DD3P2}	V_{DD2}	4	4	mA
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	240	240	µA

Table 4: 32 Meg x 16 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I_{DD3PS1}	V_{DD1}	750	750	µA
I_{DD3PS2}	V_{DD2}	4	4	mA
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	240	240	µA
I_{DD3N1}	V_{DD1}	0.7	0.7	mA
I_{DD3N2}	V_{DD2}	12	12	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD3NS1}	V_{DD1}	0.7	0.7	mA
I_{DD3NS2}	V_{DD2}	2.5	2.5	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	6	6	
I_{DD4R1}	V_{DD1}	2	2	mA
I_{DD4R2}	V_{DD2}	125	125	
$I_{DD4R,in}$	V_{DDCA}	10	10	
I_{DD4W1}	V_{DD1}	2	2	mA
I_{DD4W2}	V_{DD2}	90	90	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	30	30	
I_{DD51}	V_{DD1}	22	22	mA
I_{DD52}	V_{DD2}	60	60	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD5AB1}	V_{DD1}	1.2	1.2	mA
I_{DD5AB2}	V_{DD2}	12	12	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	10	10	
I_{DD61}	V_{DD1}	500	500	µA
I_{DD62}	V_{DD2}	2000	2000	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	50	50	
I_{DD81}	V_{DD1}	25	25	µA
I_{DD82}	V_{DD2}	60	60	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	25	25	

Table 5: 32 Meg x 32 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I_{DD01}	V_{DD1}	18	18	mA
I_{DD02}	V_{DD2}	56	56	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	20	20	

Table 5: 32 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I_{DD2P1}	V_{DD1}	400	400	µA
I_{DD2P2}	V_{DD2}	1000	1000	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	150	150	
I_{DD2PS1}	V_{DD1}	400	400	µA
I_{DD2PS2}	V_{DD2}	1000	1000	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	150	150	
I_{DD2N1}	V_{DD1}	4	4	mA
I_{DD2N2}	V_{DD2}	20	20	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	20	20	
I_{DD2NS1}	V_{DD1}	1.4	1.4	mA
I_{DD2NS2}	V_{DD2}	5	5	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	12	12	
I_{DD3P1}	V_{DD1}	1500	1500	µA
I_{DD3P2}	V_{DD2}	8	8	mA
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	480	480	µA
I_{DD3PS1}	V_{DD1}	1500	1500	µA
I_{DD3PS2}	V_{DD2}	8	8	mA
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	480	480	µA
I_{DD3N1}	V_{DD1}	1.4	1.4	mA
I_{DD3N2}	V_{DD2}	24	24	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	20	20	
I_{DD3NS1}	V_{DD1}	1.4	1.4	mA
I_{DD3NS2}	V_{DD2}	5	5	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	12	12	
I_{DD4R1}	V_{DD1}	4	4	mA
I_{DD4R2}	V_{DD2}	250	250	
$I_{DD4R,in}$	V_{DDCA}	20	20	
I_{DD4W1}	V_{DD1}	4	4	mA
I_{DD4W2}	V_{DD2}	180	180	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	60	60	
I_{DD51}	V_{DD1}	44	44	mA
I_{DD52}	V_{DD2}	120	120	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	20	20	
I_{DD5AB1}	V_{DD1}	2.4	2.4	mA
I_{DD5AB2}	V_{DD2}	24	24	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	20	20	

Table 5: 32 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I_{DD61}	V_{DD1}	1000	1000	µA
I_{DD62}	V_{DD2}	4000	4000	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	100	100	
I_{DD81}	V_{DD1}	50	50	µA
I_{DD82}	V_{DD2}	120	120	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	50	50	

Table 6: 32 Meg x 16 I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit
Full array	V_{DD1}	500	µA
	V_{DD2}	2000	
	V_{DDi}	50	
1/2 array	V_{DD1}	300	
	V_{DD2}	1200	
	V_{DDi}	50	
1/4 array	V_{DD1}	250	
	V_{DD2}	800	
	V_{DDi}	50	

Figure 2: 32 Meg x 16 I_{DD61} Typical Self Refresh Current vs. Temperature

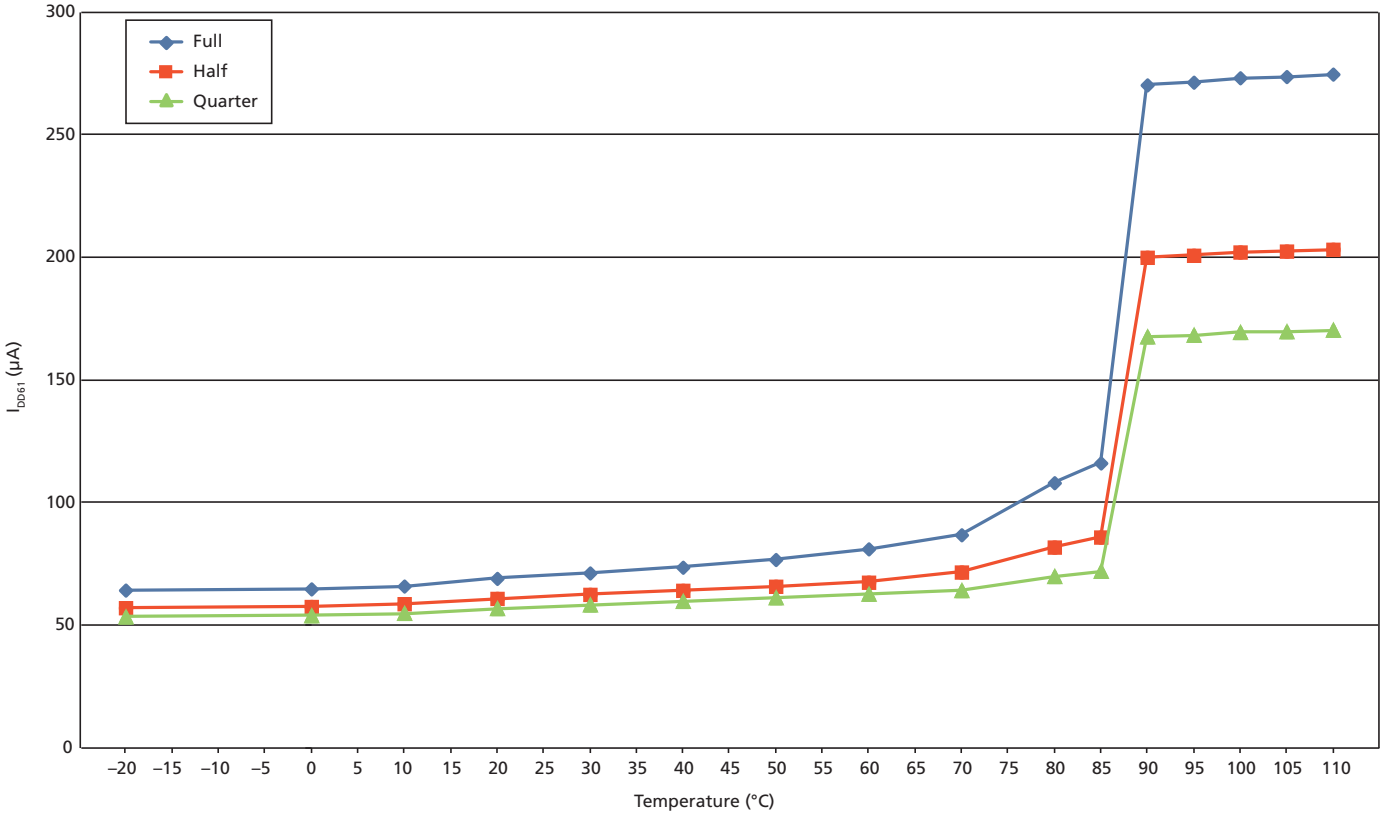


Table 7: 32 Meg x 32 DDP I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit
Full array	V_{DD1}	1000	µA
	V_{DD2}	4000	
	V_{DDi}	100	
1/2 array	V_{DD1}	600	
	V_{DD2}	2400	
	V_{DDi}	100	
1/4 array	V_{DD1}	500	
	V_{DD2}	1600	
	V_{DDi}	100	

Package Block Diagrams

Figure 3: LPDDR2 x 1 Die

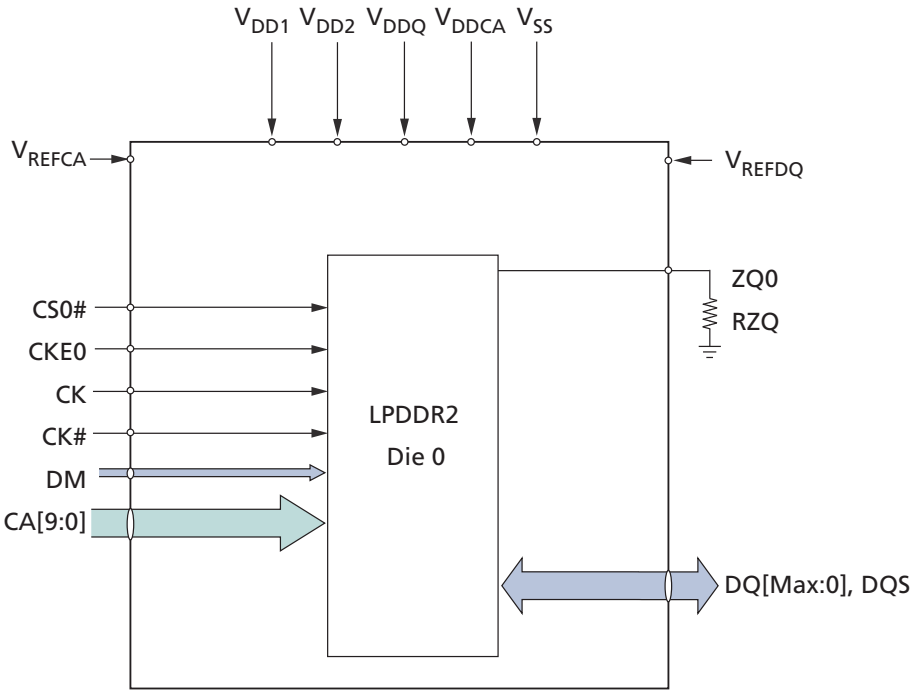
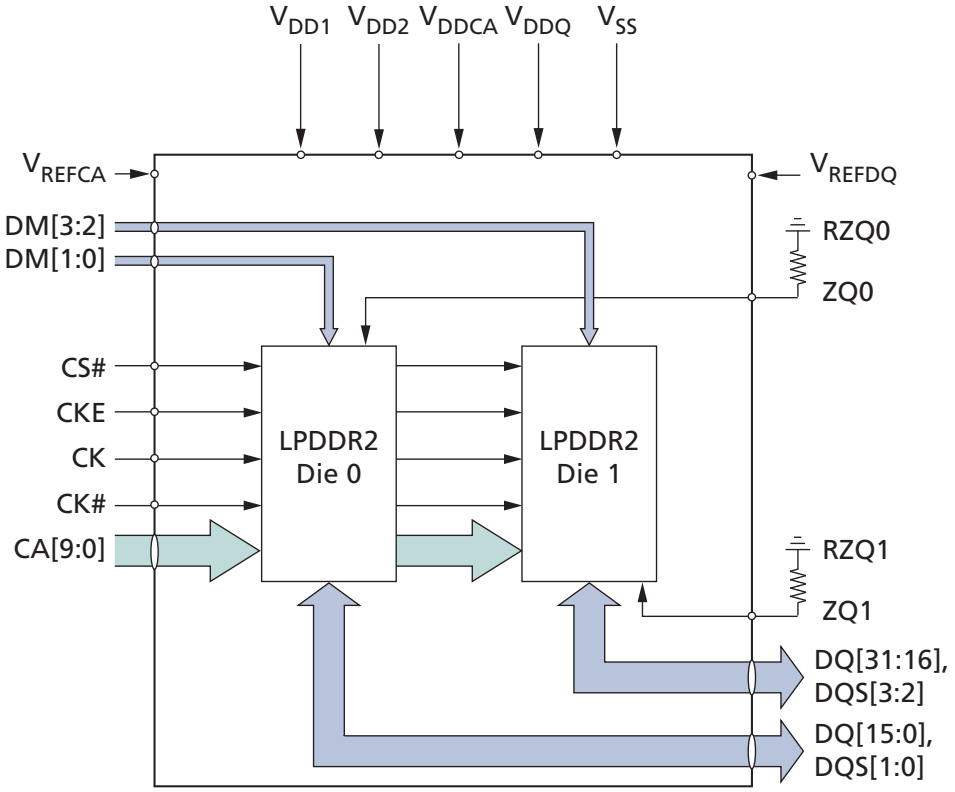
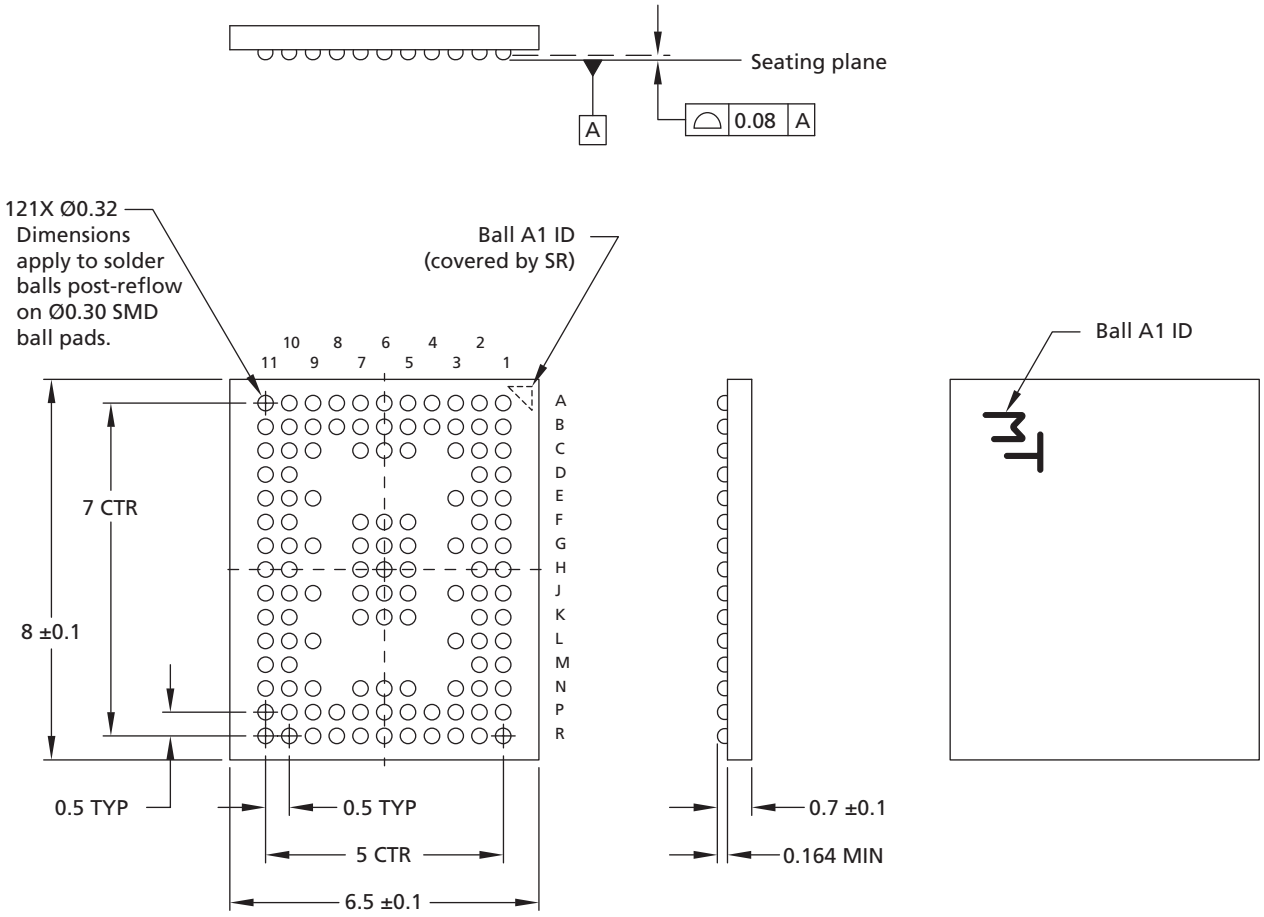


Figure 4: LPDDR2 x 2 Die



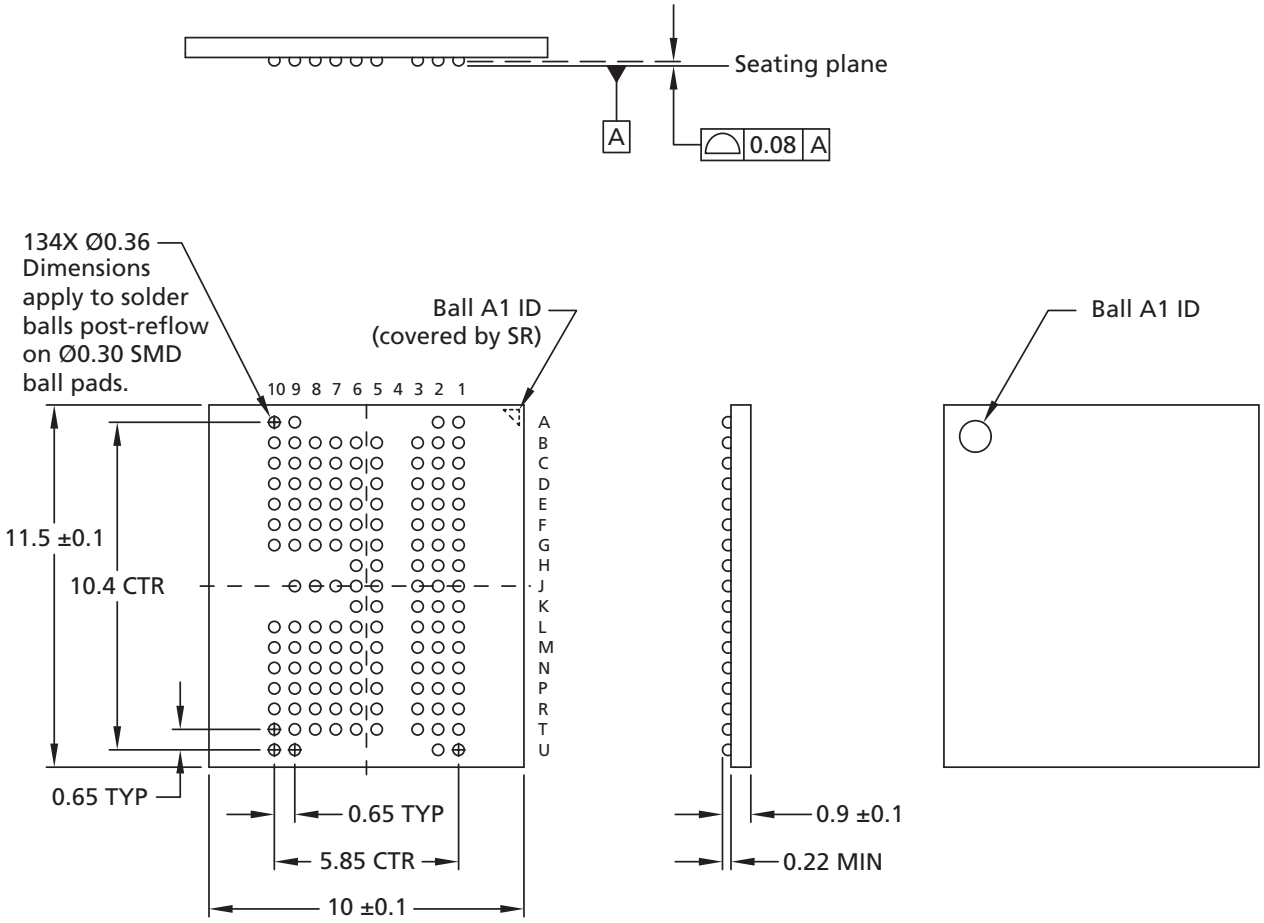
Package Dimensions

Figure 5: 121-Ball FBGA – 6.5mm x 8mm (Package Codes AB, FE)



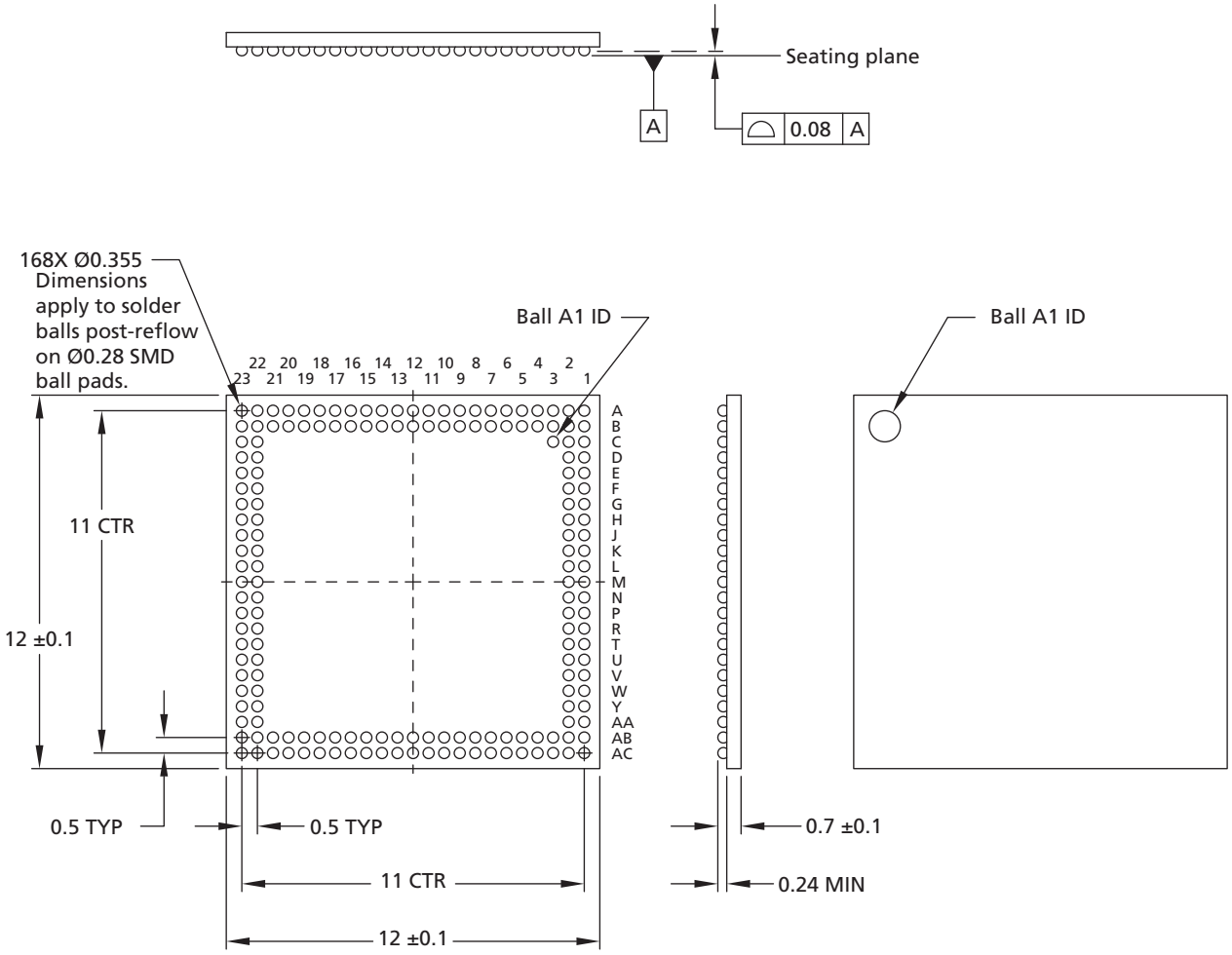
Notes:
1. All dimensions are in millimeters.
2. AB solder ball material: LF35 (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).
   FE solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Figure 6: 134-Ball FBGA – 10mm x 11.5mm (Package Code AC)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 7: 168-Ball PoP – 12mm x 12mm Single-Die (Package Code LG)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Ball Assignments and Descriptions

Figure 8: 121-Ball FBGA (x16) Ball Assignments

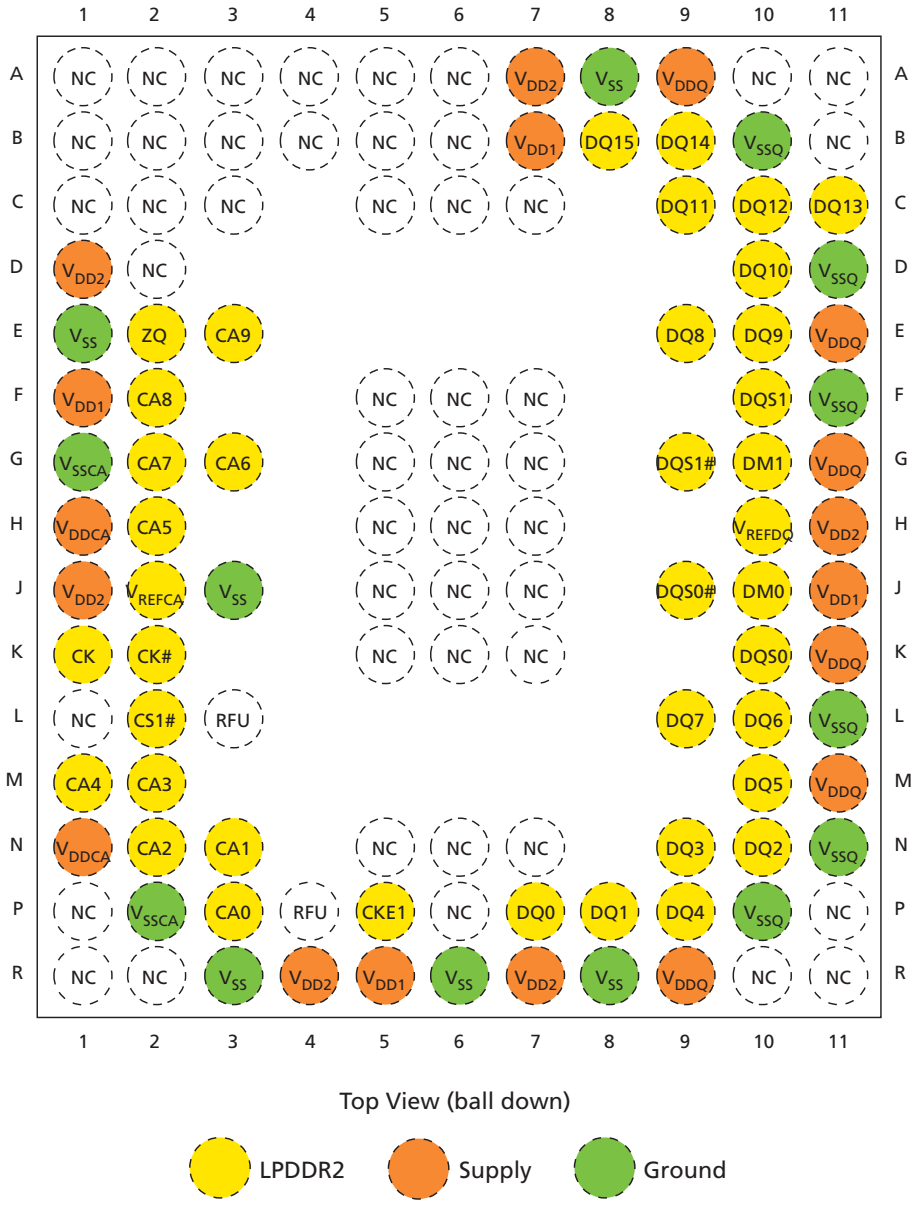


Figure 9: 134-Ball DDP FBGA (x32) Ball Assignments (Top View, Balls Down)

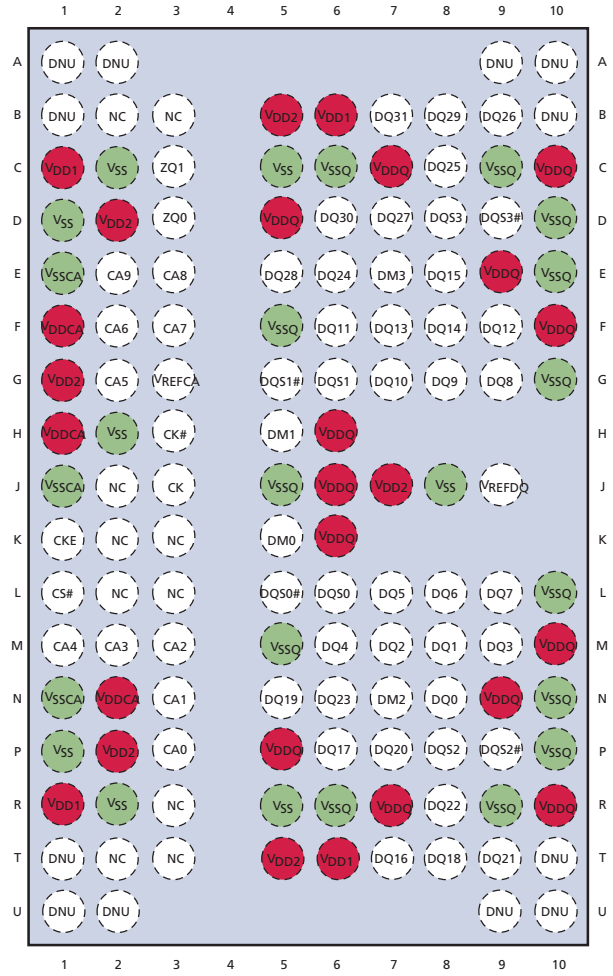
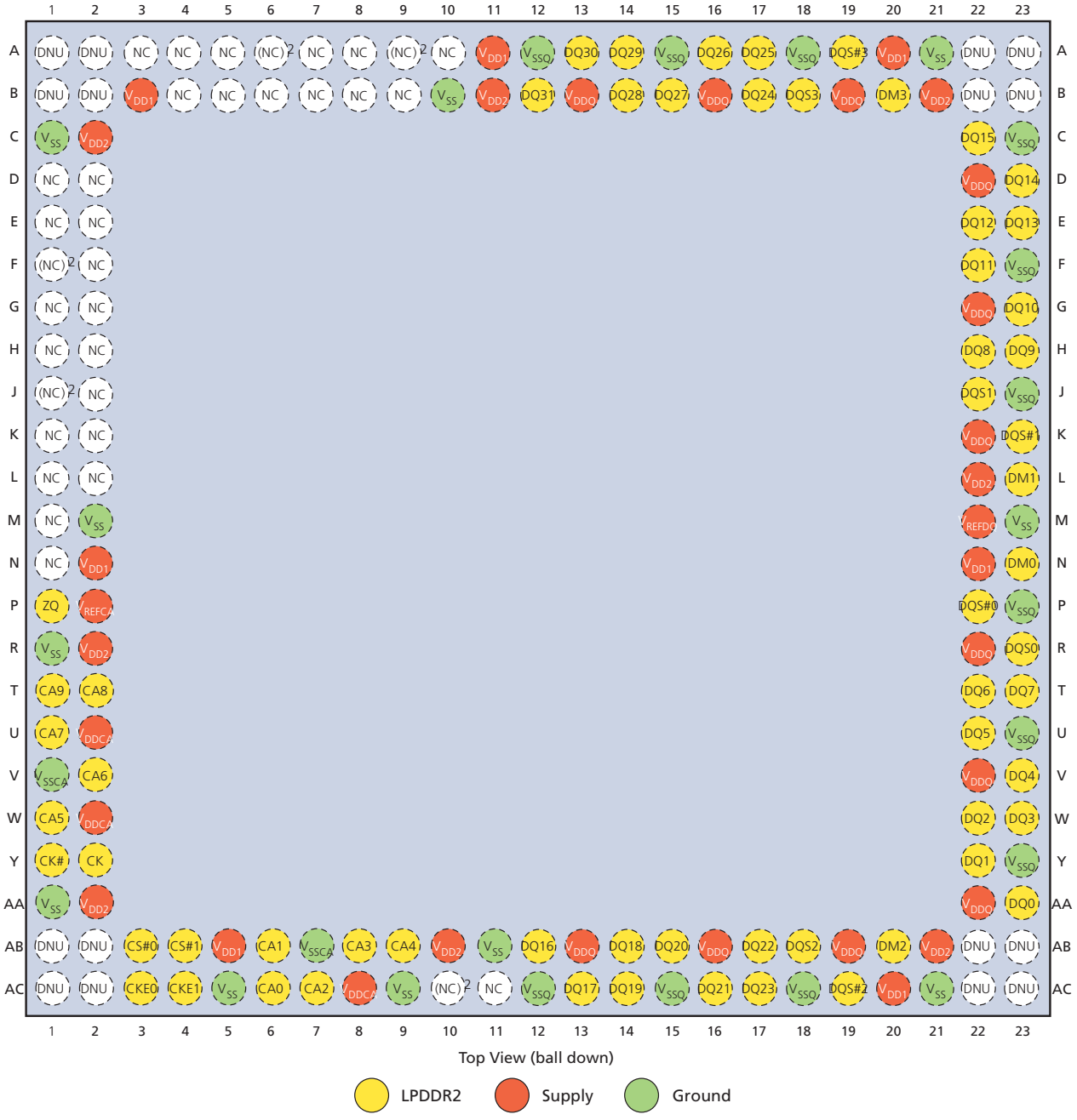


Figure 10: 168-Ball PoP (x32) Ball Assignments



Notes:
1. Ball AC9 may be V_{SS} or left unconnected.
2. Balls labeled NC = no connect; however, they can be connected together internally.

Table 8: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS[1:0]#	Input	**Chip select:** CS# is considered part of the command code and is sampled at the rising edge of CK.
DM[3:0]	Input	**Input data mask:** DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[15:0] (x16), DQ[31:0] (x32)	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0], DQS[3:0]#	I/O	**Data strobe:** The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/DQS[3:0]# is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{SSCA}	Supply	**Command/address ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ	Reference	**External impedance (240 ohm):** This signal is used to calibrate the device output impedance.
NC	–	**No connect:** Not internally connected.

Functional Description

Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4- or 8-bank memory device. LPDDR2 devices use a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a 4*n* prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Figure 11: Functional Block Diagram