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RLDRAM 3

MT44K32M18 – 2 Meg x 18 x 16 Banks
MT44K16M36 – 1 Meg x 36 x 16 Banks

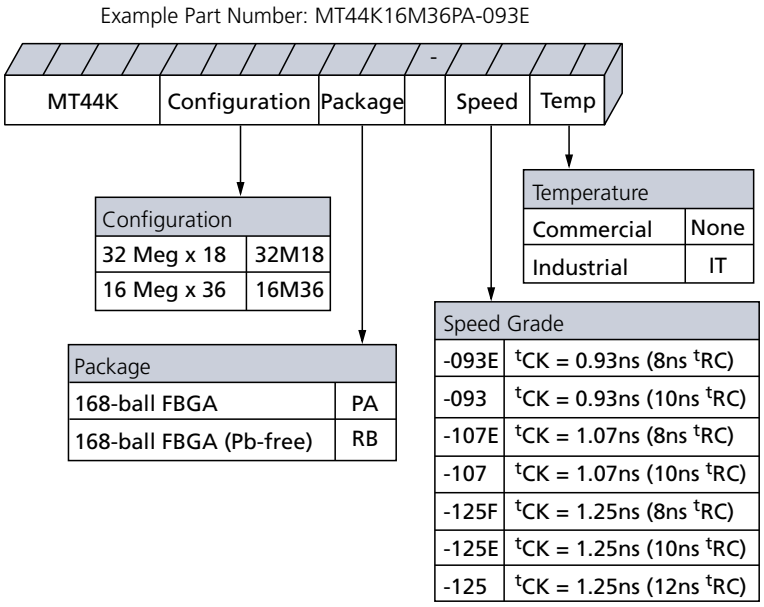
Features

- 1066 MHz DDR operation (2133 Mb/s/ball data rate)
- 76.8 Gb/s peak bandwidth (x36 at 1066 MHz clock frequency)
- Organization
  - 32 Meg x 18, and 16 Meg x 36 common I/O (CIO)
  - 16 banks
- 1.2V center-terminated push/pull I/O
- 2.5V V_{EXT}, 1.35V V_{DD}, 1.2V V_{DDQ} I/O
- Reduced cycle time (^{t}RC (MIN) = 8 - 12ns)
- SDR addressing
- Programmable READ/WRITE latency (RL/WL) and burst length
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Free-running differential input data clocks (DK*x*, DK*x*#) and output data clocks (QK*x*, QK*x*#)
- On-die DLL generates CK edge-aligned data and differential output data clock signals
- 64ms refresh (128K refresh per 64ms)
- 168-ball FBGA package
- 40Ω or 60Ω matched impedance outputs
- Integrated on-die termination (ODT)
- Single or multibank writes
- Extended operating range (200–1066 MHz)
- READ training register
- Multiplexed and non-multiplexed addressing capabilities
- Mirror function
- Output driver and ODT calibration
- JTAG interface (IEEE 1149.1-2001)

Options[1]	Marking
• Clock cycle and ^{t}RC timing	
– 0.93ns and ^{t}RC (MIN) = 8ns (RL3-2133)	-093E
– 0.93ns and ^{t}RC (MIN) = 10ns (RL3-2133)	-093
– 1.07ns and ^{t}RC (MIN) = 8ns (RL3-1866)	-107E
– 1.07ns and ^{t}RC (MIN) = 10ns (RL3-1866)	-107
– 1.25ns and ^{t}RC (MIN) = 8ns (RL3-1600)	-125F
– 1.25ns and ^{t}RC (MIN) = 10ns (RL3-1600)	-125E
– 1.25ns and ^{t}RC (MIN) = 12ns (RL3-1600)	-125
• Configuration	
– 32 Meg x 18	32M18
– 16 Meg x 36	16M36
• Operating temperature	
– Commercial (T_C = 0° to +95°C)	None
– Industrial (T_C = –40°C to +95°C)	IT
• Package	
– 168-ball FBGA	PA[2]
– 168-ball FBGA (Pb-free)	RB
• Revision	:A

Notes:
1. Not all options listed can be combined to define an offered product. Use the part catalog search on www.micron.com for available offerings.
2. Consult factory.

Figure 1: 576Mb RLDRAM® 3 Part Numbers



BGA Part Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. Micron's BGA Part Marking Decoder is available on Micron's Web site at www.micron.com.

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General Description

The Micron® RLDRAM® 3 is a high-speed memory device designed for high-bandwidth data storage—telecommunications, networking, cache applications, etc. The chip's 16-bank architecture is optimized for sustainable high-speed operation.

The DDR I/O interface transfers two data bits per clock cycle at the I/O balls. Output data is referenced to the READ strobes.

Commands, addresses, and control signals are also registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data strobes.

Read and write accesses to the RL3 device are burst-oriented. The burst length (BL) is programmable to 2, 4, or 8 by a setting in the mode register.

The device is supplied with 1.35V for the core and 1.2V for the output drivers. The 2.5V supply is used for an internal supply.

Bank-scheduled refresh is supported with the row address generated internally.

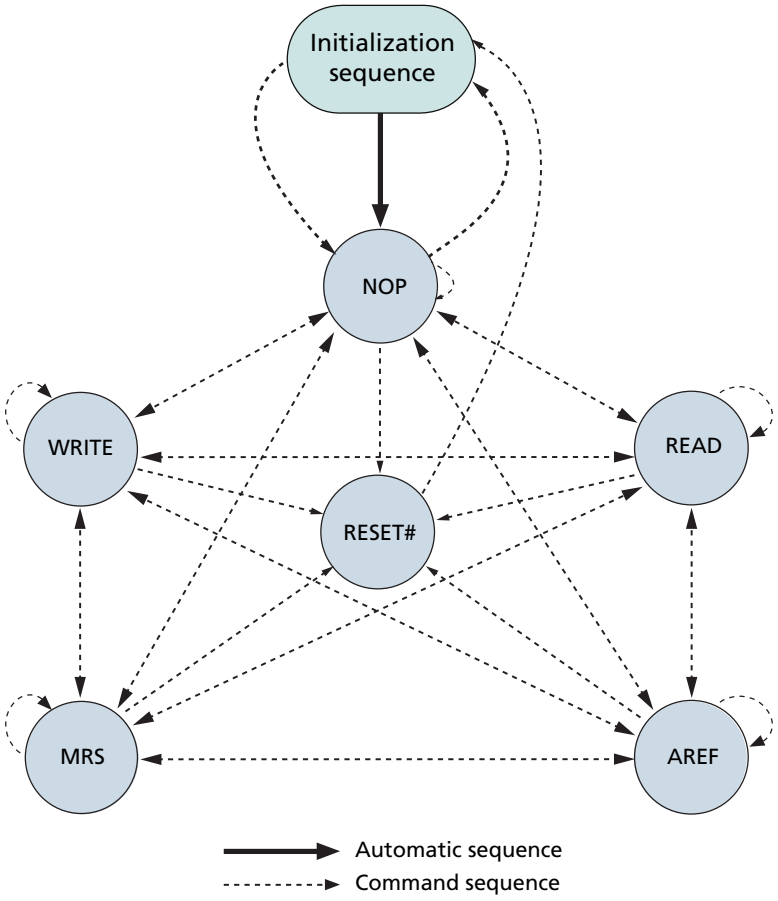
The 168-ball FBGA package is used to enable ultra-high-speed data transfer rates.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Nominal conditions are assumed for specifications not defined within the figures shown in this data sheet.
- Throughout this data sheet, the terms "RLDRAM," "DRAM," and "RLDRAM 3" are all used interchangeably and refer to the RLDRAM 3 SDRAM device.
- References to DQ, DK, QK, DM, and QVLD are to be interpeted as each group collectively, unless specifically stated otherwise. This includes true and complement signals of differential signals.
- Non-multiplexed operation is assumed if not specified as multiplexed.
- A X36 Device supplies four QK/QK# sets. One per 9 DQs. If a user only wants to use two QK/QK# sets, this is allowed. The user needs to use QK0/QK0# and QK1/QK1#. QK0/QK0# will control DQ[8:0] & DQ[26:18]. QK1/QK1# will control DQ[17:9] & DQ[35:27]. The QK to DQ timing parameter to be used would be ^{t}QKQ02, ^{t}QKQ13. The unused QK/QK# pins should be left floating.

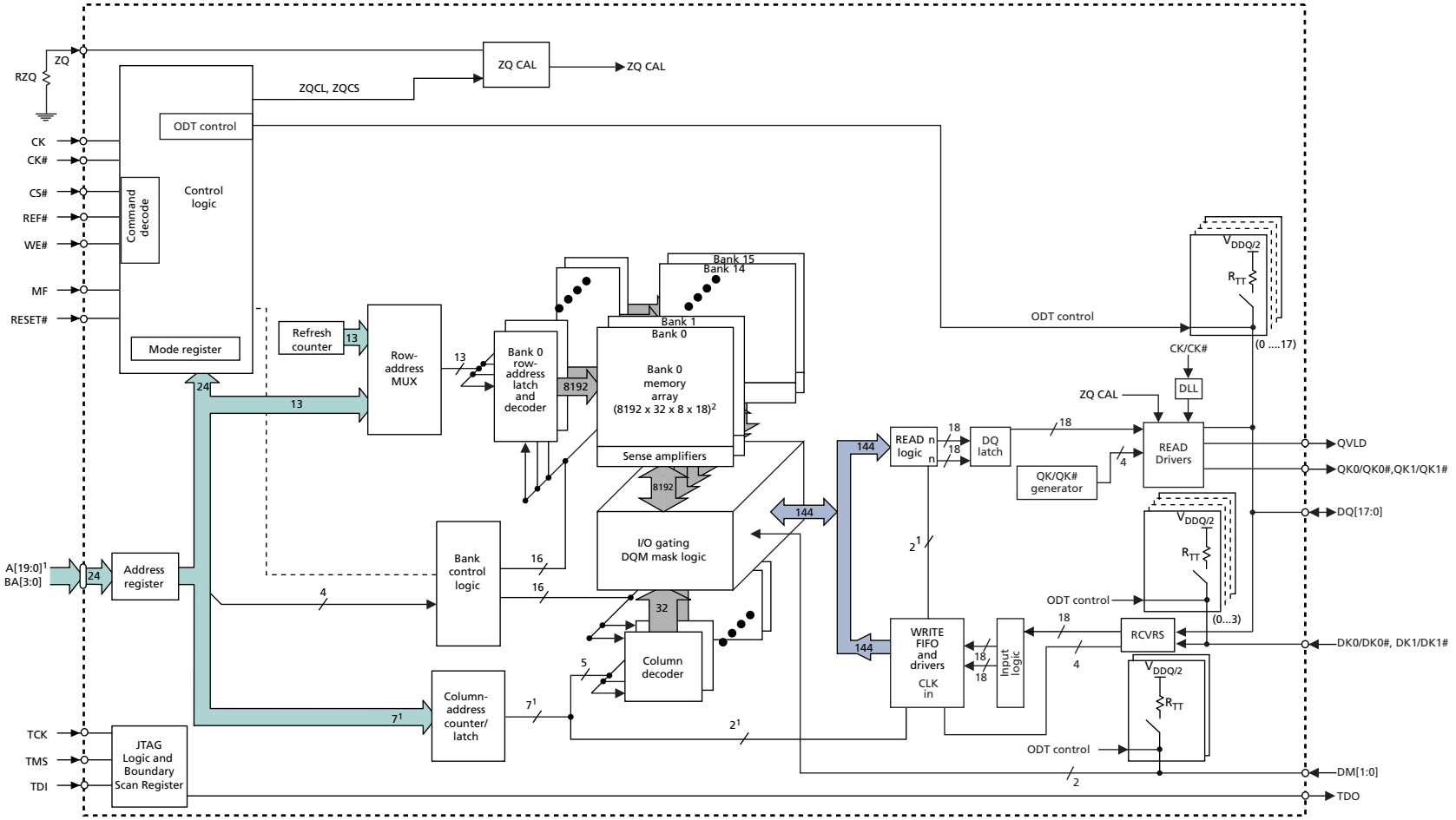
State Diagram

Figure 2: Simplified State Diagram



Functional Block Diagrams

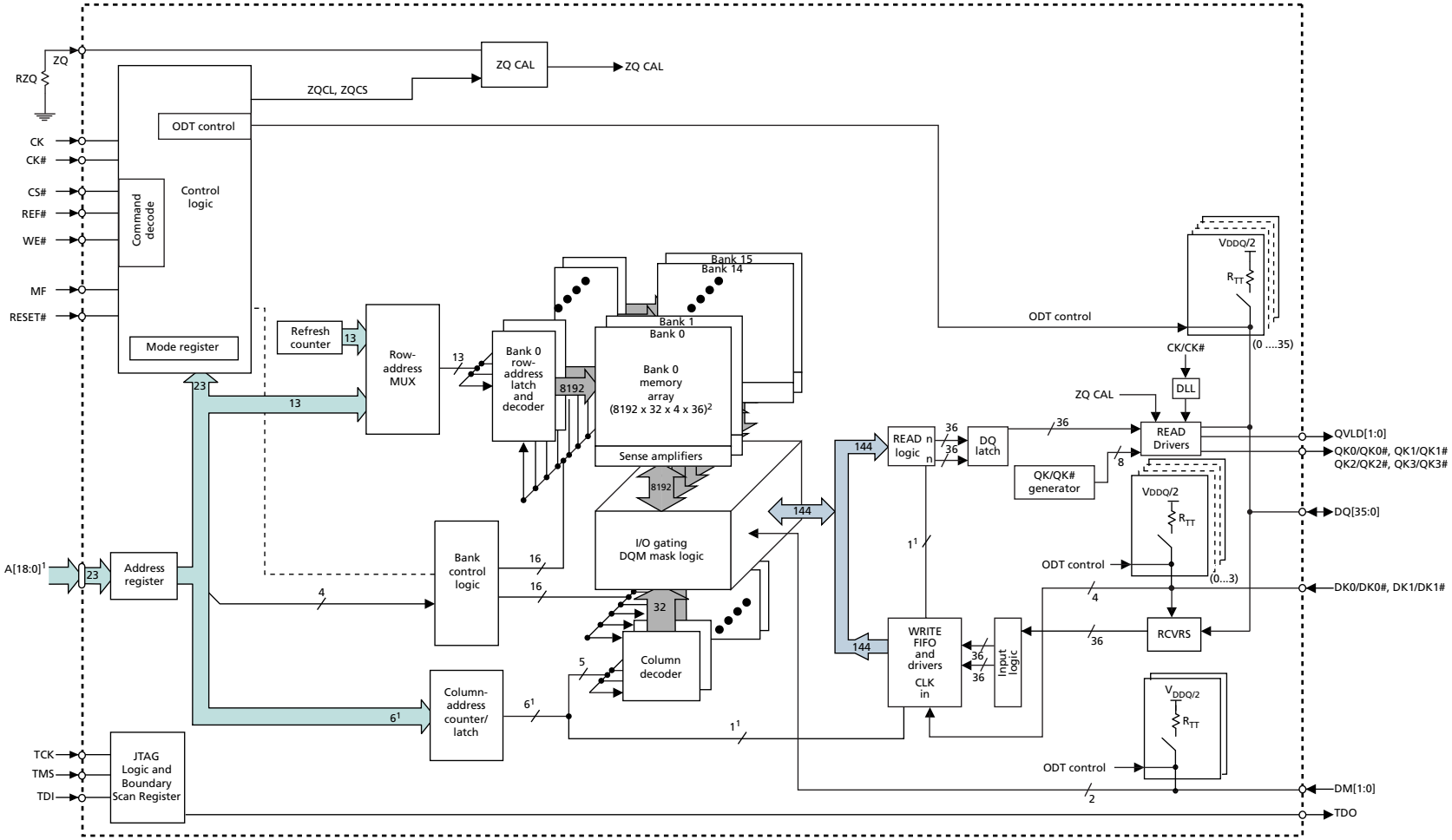
Figure 3: 32 Meg x 18 Functional Block Diagram



Notes: 1. Example for BL = 2; column address will be reduced with an increase in burst length.
2. 8 = (length of burst) x 2^ (number of column addresses to WRITE FIFO and READ logic).

Functional Block Diagrams

Figure 4: 16 Meg x 36 Functional Block Diagram



Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
2. 4 = (length of burst) x 2^ (number of column addresses to WRITE FIFO and READ logic).

Ball Assignments and Descriptions

Table 1: 32 Meg x 18 Ball Assignments – 168-Ball FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	NF	V_{DDQ}	NF	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	NF	V_{SSQ}	NF	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	NF	V_{DDQ}	NF	V_{SSQ}	NF	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A11	V_{SSQ}	NF	V_{DDQ}	NF	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
E	V_{SS}	A0	V_{SSQ}	NF	V_{DDQ}	NF	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS#	V_{SS}
F	A7	$NF_{(CS1/A20)}$[1]	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
G	$V_{SS(A21)}$[2]	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	$V_{SS\ (RFU)}$[3]
H	A19	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
J	V_{DDQ}	NF	V_{SSQ}	NF	V_{DDQ}	NF	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD	V_{DDQ}
K	NF	V_{SSQ}	NF	V_{DDQ}	NF	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	NF	V_{DDQ}	NF	V_{SSQ}	NF	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	NF	V_{SSQ}	NF	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	NF	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes:
1. F2 is an NF ball for both the X18 & X36 576Mb devices, but is also the Location of CS1 to support the 1Gb x18 DDP device. This same ball has been designated as the location of A20 for the future 2Gb monolithic device. F2 is Internally connected so it can mirror the A5 address signal when MF is asserted HIGH and has parasitic characteristics of an address pin.
2. G1 is a VSS ball for the 576Mb device, but has been designated as the location of A21 for the future X18 2Gb monolithic device.
3. G13 is a VSS ball for both X18 & X36 576Mb devices, but has been reserved for future use (RFU) on the 1Gb & 2Gb monolithic devices and will have parasitic characteristics of an address.
4. NF balls for the x18 configuration are internally connected and have parasitic characteristics of an I/O. Balls may be connected to V_{SSQ}.
5. MF is assumed to be tied LOW for this ball assignment.

Table 2: 16 Meg x 36 Ball Assignments – 168-Ball FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	DQ26	V_{DDQ}	DQ25	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	DQ24	V_{SSQ}	DQ23	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	DQ22	V_{DDQ}	DQ21	V_{SSQ}	DQ20	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A11	V_{SSQ}	DQ18	V_{DDQ}	QK2	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
E	V_{SS}	A0	V_{SSQ}	DQ19	V_{DDQ}	QK2#	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS#	V_{SS}
F	A7	$NF_{(CS1/A20)}$[1]	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
G	$V_{SS(NF)}$[2]	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	$V_{SS\ (RFU)}$[3]
H	$NF_{(A19)}$[4]	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
J	V_{DDQ}	QVLD1	V_{SSQ}	DQ27	V_{DDQ}	QK3#	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD0	V_{DDQ}
K	DQ29	V_{SSQ}	DQ28	V_{DDQ}	QK3	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	DQ32	V_{DDQ}	DQ31	V_{SSQ}	DQ30	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	DQ34	V_{SSQ}	DQ33	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	DQ35	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes:
1. F2 is an NF ball for both the X18 & X36 576Mb devices, but is also the Location of CS1 to support the 1Gb x18 DDP device. This same ball has been designated as the location of A20 for the future 2Gb monolithic device. F2 is Internally connected so it can mirror the A5 address signal when MF is asserted HIGH and has parasitic characteristics of an address pin.
2. G1 is a VSS ball for this 576Mb device, but will be an NF ball for the future X36 2Gb monolithic device. The NF ball (A21 for X18 2Gb device) will have parasitic characteristics of an address.
3. G13 is a VSS ball for both X18 & X36 576Mb devices, but has been reserved for future use (RFU) on the 1Gb & 2Gb monolithic devices and will have parasitic characteristics of an address.
4. NF ball for x36 configuration is internally connected and has parasitic characteristics of an address (A19 for x18 configuration). Ball may be connected to V_{SSQ}.
5. MF is assumed to be tied LOW for this ball assignment.

Table 3: Ball Descriptions

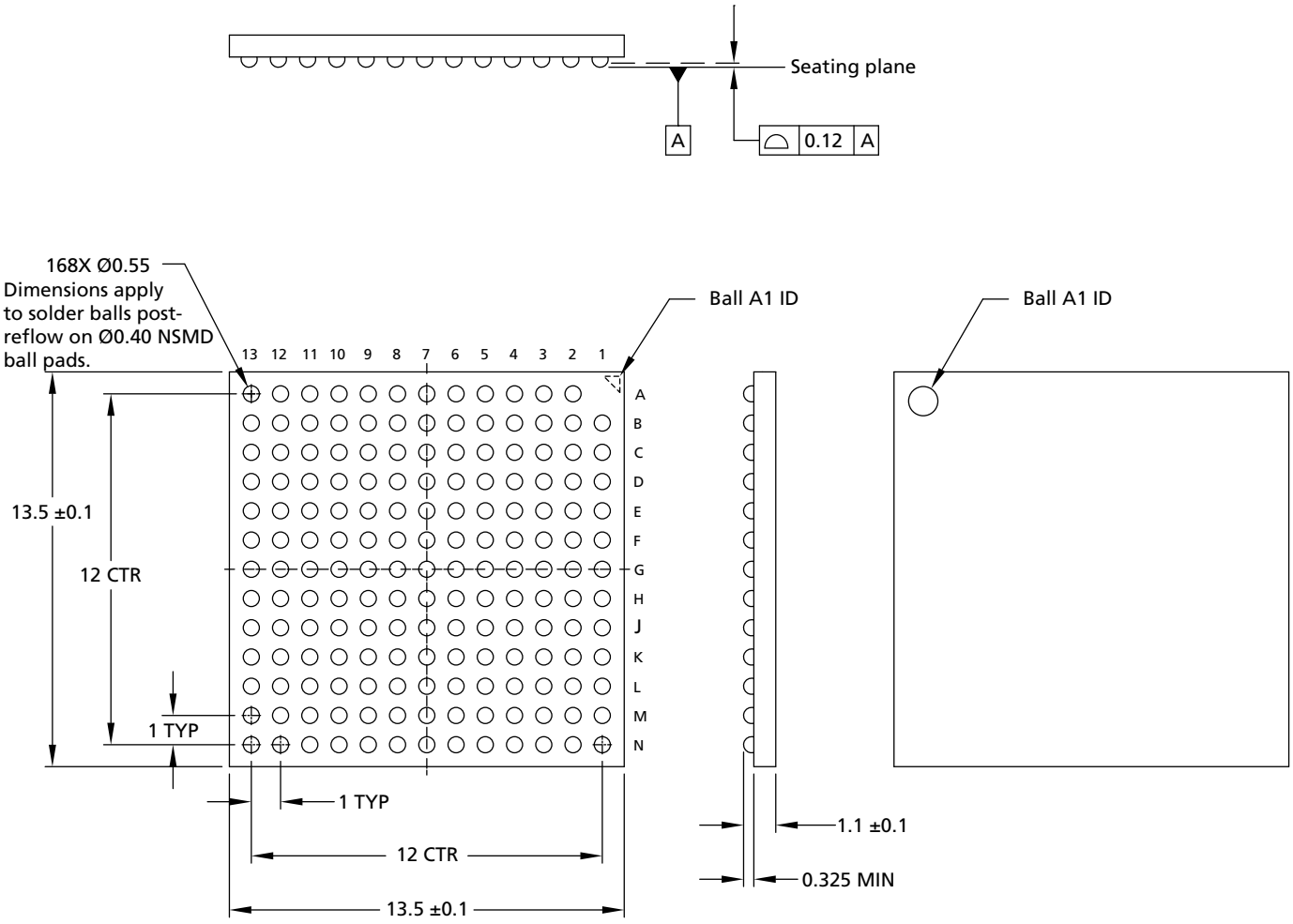
Symbol	Type	Description
A[19:0]	Input	**Address inputs:** A[19:0] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings along with BA[3:0]. They are sampled at the rising edge of CK.
BA[3:0]	Input	**Bank address inputs:** Select the internal bank to which a command is being applied.
CK/CK#	Input	**Input clock:** CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK.
CS#	Input	**Chip select:** CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
DQ[35:0]	I/O	**Data input:** The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK. During WRITE commands, the data is sampled at both edges of DK.
DK*x*, DK*x*#	Input	**Input data clock:** DK*x* and DK*x*# are differential input data clocks. All input data is referenced to both edges of DK*x*. For the x36 device, DQ[8:0] and DQ[26:18] are referenced to DK0 and DK0#, and DQ[17:9] and DQ[35:27] are referenced to DK1 and DK1#. For the x18 device, DQ[8:0] are referenced to DK0 and DK0#, and DQ[17:9] are referenced to DK1 and DK1#. DK*x* and DK*x*# are free-running signals and must always be supplied to the device.
DM[1:0]	Input	**Input data mask:** DM is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM0 is used to mask the lower byte for the x18 device and DQ[8:0] and DQ[26:18] for the x36 device. DM1 is used to mask the upper byte for the x18 device and DQ[17:9] and DQ[35:27] for the x36 device. Tie DM[1:0] to V_{SS} if not used.
TCK	Input	**IEEE 1149.1 clock input:** This ball must be tied to V_{SS} if the JTAG function is not used.
TMS, TDI	Input	**IEEE 1149.1 test inputs:** These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	**Command inputs:** Sampled at the positive edge of CK, WE# and REF# (together with CS#) define the command to be executed.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. RESET# assertion and deassertion are asynchronous. RESET# is a CMOS input defined with DC HIGH ≥ 0.8 x V_{DD} and DC LOW ≤ 0.2 x V_{DDQ}.
ZQ	Input	**External impedance:** This signal is used to tune the device's output impedance and ODT. RZQ needs to be 240Ω, where RZQ is a resistor from this signal to ground.
QK*x*, QK*x*#	Output	**Output data clocks:** QK and QK# are opposite-polarity output data clocks. They are free-running signals and during READ commands are edge-aligned with the DQs. For the x36 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9]; QK2, QK2# align with DQ[26:18]; QK3, QK3# align with DQ[35:27]. For the x18 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9].
QVLD*x*	Output	**Data valid:** The QVLD ball indicates that valid output data will be available on the subsequent rising clock edge. There is a single QVLD ball for the x18 device and two, QVLD0 and QVLD1, for the x36 device. QVLD0 aligns with DQ[17:0]; QVLD1 aligns with DQ[35:18].
MF	Input	**Mirror function:** The mirror function ball is a DC input used to create mirrored ballouts for simple dual-loaded clamshell mounting. If the ball is tied to V_{SS}, the address and command balls are in their true layout. If the ball is tied to V_{DDQ}, they are in the complement location. MF must be tied HIGH or LOW and cannot be left floating. MF is a CMOS input defined with DC HIGH ≥ 0.8 x V_{DD} and DC LOW ≤ 0.2 x V_{DDQ}.

Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
TDO	Output	**IEEE 1149.1 test output:** JTAG output. This ball may be left as no connect if the JTAG function is not used.
V_{DD}	Supply	**Power supply:** 1.35V nominal. See Table 7 (page 22) for range.
V_{DDQ}	Supply	**DQ power supply:** 1.2V nominal. Isolated on the device for improved noise immunity. See Table 7 (page 22) for range.
V_{EXT}	Supply	**Power supply:** 2.5V nominal. See Table 7 (page 22) for range.
V_{REF}	Supply	**Input reference voltage:** V_{DDQ}/2 nominal. Provides a reference voltage for the input buffers.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NC	–	**No connect:** These balls are not connected to the DRAM.
NF	–	**No function:** These balls are connected to the DRAM, but provide no functionality.

Package Dimensions

Figure 5: 168-Ball FBGA



Note: 1. All dimensions are in millimeters.

Electrical Characteristics – I_{DD} Specifications

Table 4: I_{DD} Operating Conditions and Maximum Limits

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-093E	-093	-107E	-107	-125F	-125E	-125	Units	Notes
Standby current	^{t}CK = idle; All banks idle; No inputs toggling	I_{SB1} (V_{DD}) x18	125	125	125	125	125	125	125	mA	7
		I_{SB1} (V_{DD}) x36	125	125	125	125	125	125	125		
		I_{SB1} (V_{EXT})	30	30	30	30	30	30	30		
Clock active standby current	CS# = 1; No commands; Bank address incremented and half address/ data change once every four clock cycles	I_{SB2} (V_{DD}) x18	870	870	815	815	725	725	725	mA	
		I_{SB2} (V_{DD}) x36	895	895	835	835	740	740	740		
		I_{SB2} (V_{EXT})	30	30	30	30	30	30	30		
Operational current: BL2	BL = 2; Sequential bank access; Bank transitions once every ^{t}RC; Half address transitions once every ^{t}RC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD1} (V_{DD}) x18	1175	1115	1100	1045	990	940	915	mA	
		I_{DD1} (V_{DD}) x36	1185	1125	1110	1055	1000	950	925		
		I_{DD1} (V_{EXT})	35	35	35	35	35	35	35		
Operational current: BL4	BL = 4; Sequential bank access; Bank transitions once every ^{t}RC; Half address transitions once every ^{t}RC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD2} (V_{DD}) x18	1205	1145	1130	1075	1020	970	945	mA	
		I_{DD2} (V_{DD}) x36	1215	1155	1140	1080	1030	980	950		
		I_{DD2} (V_{EXT})	35	35	35	35	35	35	35		
Operational current: BL8	BL = 8; Sequential bank access; Bank transitions once every ^{t}RC; Half address transitions once every ^{t}RC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD3} (V_{DD}) x18	1300	1220	1200	1130	1085	1030	1000	mA	
		I_{DD3} (V_{DD}) x36	NA	NA	NA	NA	N/A	NA	NA		
		I_{DD3} (V_{EXT})	35	35	35	35	35	35	35		
Burst refresh current	Sixteen bank cyclic refresh using Bank Address Control AREF protocol; Command bus remains in refresh for all sixteen banks; DQs are High-Z and at V_{DDQ}/2; Addresses are at V_{DDQ}/2	I_{REF1} (V_{DD}) x18	1550	1550	1400	1400	1230	1230	1230	mA	
		I_{REF1} (V_{DD}) x36	1570	1570	1420	1420	1245	1245	1245		
		I_{REF1} (V_{EXT})	80	80	75	75	70	70	70		

Table 4: I_{DD} Operating Conditions and Maximum Limits (Continued)

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-093E	-093	-107E	-107	-125F	-125E	-125	Units	Notes
Distributed refresh current	Single bank refresh using Bank Address Control AREF protocol; Sequential bank access every 0.489µs; DQs are High-Z and at $V_{DDQ}/2$; Addresses are at $V_{DDQ}/2$	I_{REF2} (V_{DD}) x18	875	875	820	820	730	730	730	mA	
		I_{REF2} (V_{DD}) x36	900	900	840	840	745	745	745		
		I_{REF2} (V_{EXT})	30	30	30	30	30	30	30		
Multibank refresh current: 4 bank refresh	Quad bank refresh using Multibank AREF protocol; BL = 4; Cyclic bank access; Subject to ^{t}SAW and ^{t}MMD specifications; DQs are High-Z and at $V_{DDQ}/2$; Bank addresses are at $V_{DDQ}/2$	I_{MBREF4} (V_{DD}) x18	2130	1925	2030	1810	1885	1885	1645	mA	
		I_{MBREF4} (V_{DD}) x36	2155	1950	2050	1830	1900	1900	1660		
		I_{MBREF4} (V_{EXT})	130	130	115	115	105	105	105		
Operating burst write current : BL2	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous WRITE	I_{DD2W} (V_{DD}) x18	2110	2110	1910	1910	1665	1665	1665	mA	
		I_{DD2W} (V_{DD}) x36	2290	2290	2070	2070	1805	1805	1805		
		I_{DD2W} (V_{EXT})	80	80	75	75	70	70	70		
Operating burst write current : BL4	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DD4W} (V_{DD}) x18	1730	1730	1590	1590	1395	1395	1395	mA	
		I_{DD4W} (V_{DD}) x36	1815	1815	1665	1665	1460	1460	1460		
		I_{DD4W} (V_{EXT})	55	55	55	55	50	50	50		
Operating burst write current :BL8	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DD8W} (V_{DD}) x18	1475	1475	1335	1335	1190	1190	1190	mA	
		I_{DD8W} (V_{DD}) x36	NA	NA	NA	NA	NA	NA	NA		
		I_{DD8W} (V_{EXT})	45	45	40	40	40	40	40		
Multibank write current: Dual bank write	BL = 4; Cyclic bank access using Dual Bank WRITE; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DBWR} (V_{DD}) x18	2305	2305	2170	2170	1885	1885	1885	mA	
		I_{DBWR} (V_{DD}) x36	2400	2400	2250	2250	1960	1960	1960		
		I_{DBWR} (V_{EXT})	80	80	75	75	70	70	70		
Multibank write current: Quad bank write	BL = 4; Cyclic bank access using Quad Bank WRITE; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE; Subject to ^{t}SAW specification	I_{QBWR} (V_{DD}) x18	2965	2965	2890	2890	2525	2525	2525	mA	
		I_{QBWR} (V_{DD}) x36	3195	3195	3000	3000	2615	2615	2615		
		I_{QBWR} (V_{EXT})	130	130	115	115	100	100	100		

Table 4: I_{DD} Operating Conditions and Maximum Limits (Continued)

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-093E	-093	-107E	-107	-125F	-125E	-125	Units	Notes
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous READ	I_{DD2R} (V_{DD}) x18	2250	2250	2045	2045	1785	1785	1785	mA	
		I_{DD2R} (V_{DD}) x36	2395	2395	2180	2180	1895	1895	1895		
		I_{DD2R} (V_{EXT})	80	80	75	75	70	70	70		
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous READ	I_{DD4R} (V_{DD}) x18	1740	1740	1595	1595	1400	1400	1400	mA	
		I_{DD4R} (V_{DD}) x36	1835	1835	1685	1685	1475	1475	1475		
		I_{DD4R} (V_{EXT})	55	55	55	55	50	50	50		
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous READ	I_{DD8R} (V_{DD}) x18	1450	1450	1315	1315	1175	1175	1175	mA	
		I_{DD8R} (V_{DD}) x36	NA	NA	NA	NA	NA	NA	NA		
		I_{DD8R} (V_{EXT})	45	45	40	40	40	40	40		

Notes:
1. I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V,+1.14V ≤ V_{DDQ} ≤ +1.26V,+2.38V ≤ V_{EXT} ≤ +2.63V,V_{REF} = V_{DDQ}/2.
2. I_{DD} mesurements use ^{t}CK (MIN), ^{t}RC (MIN), and minimum data latency (RL and WL).
3. Input slew rate is 1V/ns for single ended signals and 2V/ns for differential signals.
4. Definitions for I_{DD} conditions:
   - LOW is defined as V_{IN} ≤ $V_{IL(AC)MAX}$.
   - HIGH is defined as V_{IN} ≥ $V_{IH(AC)MIN}$.
   - Continuous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
   - Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
   - Sequential bank access is defined as the bank address incrementing by one every ^{t}RC.
   - Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
6. I_{DD} parameters are specified with ODT disabled.
7. Upon exiting standby current conditions, at least one NOP command must be issued with stable clock prior to issuing any other valid command.

Electrical Specifications – Absolute Ratings and I/O Capacitance

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	–0.4	1.66	V
V_{IN},V_{OUT}	Voltage on any ball relative to V_{SS}	–0.4	1.66	V
V_{EXT}	Voltage on V_{EXT} supply relative to V_{SS}	–0.4	2.8	V

Input/Output Capacitance

Table 6: Input/Output Capacitance

Notes 1 and 2 apply to entire table

Capacitance Parameters	Symbol	RL3-2133		RL3-1866		RL3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max		
CK/CK#	C_{CK}	1.3	2.1	1.3	2.1	1.3	2.2	pF	
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	
Single-ended I/O: DQ, DM	C_{IO}	1.9	2.9	1.9	3.0	2.0	3.1	pF	3
Input strobe: DK/DK#	C_{IO}	1.9	2.9	1.9	3.0	2.0	3.1	pF	
Output strobe: QK/QK#, QVLD	C_{IO}	1.9	2.9	1.9	3.0	2.0	3.1	pF	
ΔC: DK to DK#	C_{DDK}	0	0.15	0	0.15	0	0.15	pF	
ΔC: QK to QK#	C_{DQK}	0	0.15	0	0.15	0	0.15	pF	
ΔC: DQ to QK or DQ to DK	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	4
Inputs (CMD, ADDR)	C_I	1.25	2.25	1.25	2.25	1.25	2.25	pF	5
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.5	0.3	–0.5	0.3	–0.4	0.4	pF	6
JTAG balls	C_{JTAG}	1.5	4.5	1.5	4.5	1.5	4.5	pF	7
RESET#, MF balls	C_I	–	3.0	–	3.0	–	3.0	pF	

Notes:
1. +1.28V ≤ V_{DD} ≤ +1.42V, +1.14V ≤ V_{DDQ} ≤ 1.26V, +2.38V ≤ V_{EXT} ≤ +2.63V, V_{REF} = V_{SS}, f = 100 MHz, T_C = 25°C, $V_{OUT(DC)}$ = 0.5 × V_{DDQ}, V_{OUT} (peak-to-peak) = 0.1V.
2. Capacitance is not tested on ZQ ball.
3. DM input is grouped with the I/O balls, because they are matched in loading.
4. C_{DIO} = $C_{IO(DQ)}$ - 0.5 × (C_{IO} [QK] + C_{IO} [QK#]).
5. Includes CS#, REF#, WE#, A[19:0], and BA[3:0].
6. $C_{DI\_CMD\_ADDR}$ = C_I (CMD_ADDR) - 0.5 × (C_{CK} [CK] + C_{CK} [CK#]).
7. JTAG balls are tested at 50 MHz.

AC and DC Operating Conditions

Table 7: DC Electrical Characteristics and Operating Conditions

Note 1 applies to the entire table; Unless otherwise noted: 0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V

Description	Symbol	Min	Max	Units	Notes
Supply voltage	V_{EXT}	2.38	2.63	V	
Supply voltage	V_{DD}	1.28	1.42	V	
Isolated output buffer supply	V_{DDQ}	1.14	1.26	V	
Reference voltage	V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	2, 3
Input HIGH (logic 1) voltage	$V_{IH(DC)}$	V_{REF} + 0.10	V_{DDQ}	V	
Input LOW (logic 0) voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 0.10	V	
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} ball 0V ≤ V_{IN} ≤ 1.1V (All other balls not under test = 0V)	I_{LI}	–2	2	µA	
Reference voltage current (All other balls not under test = 0V)	I_{REF}	–5	5	µA	

Notes:
1. All voltages referenced to V_{SS} (GND).
2. The nominal value of V_{REF} is expected to be 0.5 × V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
3. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2% of the DC value. DC values are determined to be less than 20 MHz. Peak-to-peak AC noise on V_{REF} should not exceed ±2% of $V_{REF(DC)}$. Thus, from V_{DDQ}/2, V_{REF} is allowed ±2% V_{DDQ}/2 for DC error and an additional ±2% V_{DDQ}/2 for AC noise. The measurement is to be taken at the nearest V_{REF} bypass capacitor.

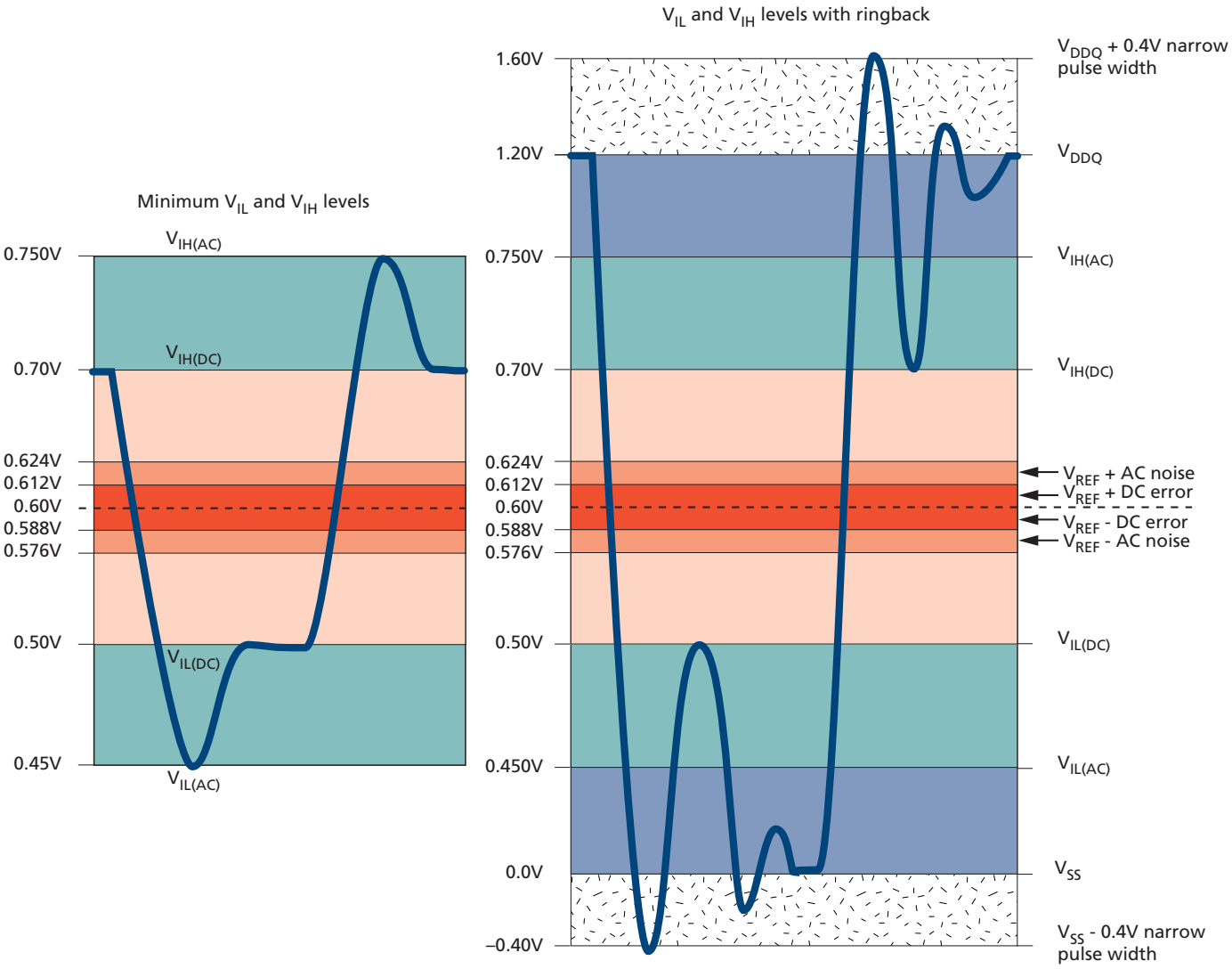
Table 8: Input AC Logic Levels

Notes 1-3 apply to entire table; Unless otherwise noted: 0°C ≤ T_C ≤ +95°C; +1.28V ≤ V_{DD} ≤ +1.42V

Description	Symbol	Min	Max	Units
Input HIGH (logic 1) voltage	$V_{IH(AC)}$	V_{REF} + 0.15	–	V
Input LOW (logic 0) voltage	$V_{IL(AC)}$	–	V_{REF} - 0.15	V

Notes:
1. All voltages referenced to V_{SS} (GND).
2. The receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above/below the DC input LOW/HIGH level.
3. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Figure 6: Single-Ended Input Signal



AC Overshoot/Undershoot Specifications

Table 9: Control and Address Balls

Parameter	RL3-2133	RL3-1866	RL3-1600
Maximum peak amplitude allowed for overshoot area	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DDQ}	0.25 Vns	0.28 Vns	0.33 Vns
Maximum undershoot area below V_{SS}/V_{SSQ}	0.25 Vns	0.28 Vns	0.33 Vns

Table 10: Clock, Data, Strobe, and Mask Balls

Parameter	RL3-2133	RL3-1866	RL3-1600
Maximum peak amplitude allowed for overshoot area	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DDQ}	0.10 Vns	0.11 Vns	0.13 Vns
Maximum undershoot area below V_{SS}/V_{SSQ}	0.10 Vns	0.11 Vns	0.13 Vns

Figure 7: Overshoot

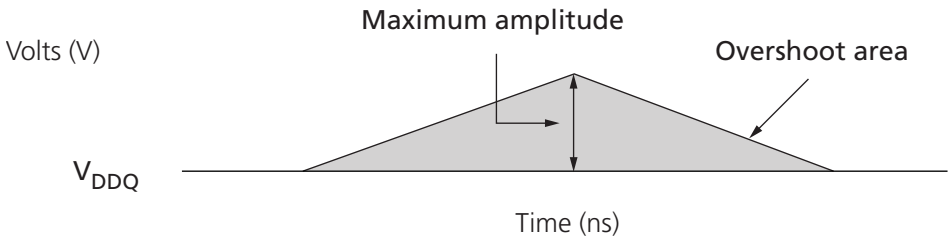


Figure 8: Undershoot

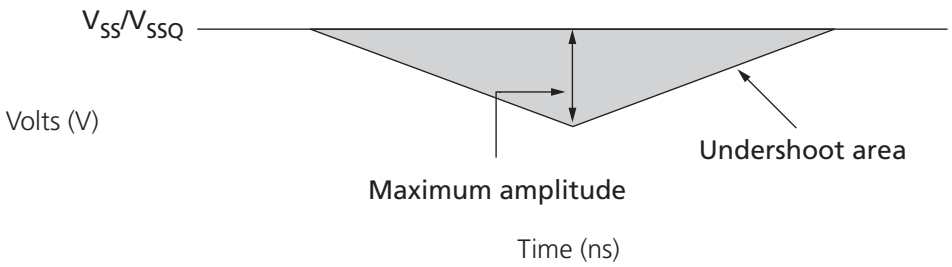


Table 11: Differential Input Operating Conditions (CK, CK# and DK*x*, DK*x*#)

Notes 1 and 2 apply to entire table

Parameter/Condition	Symbol	Min	Max	Units	Notes
Differential input voltage logic HIGH – slew	$V_{IH,diff\_slew}$	+200	n/a	mV	3
Differential input voltage logic LOW – slew	$V_{IL,diff\_slew}$	n/a	-200	mV	3
Differential input voltage logic HIGH	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	V_{DDQ}	mV	4
Differential input voltage logic LOW	$V_{IL,diff(AC)}$	V_{SSQ}	$2 \times (V_{IL(AC)} - V_{REF})$	mV	5
Differential input crossing voltage relative to $V_{DD}/2$	V_{IX}	$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150	mV	6
Single-ended HIGH level	V_{SEH}	$V_{IH(AC)}$	V_{DDQ}	mV	4
Single-ended LOW level	V_{SEL}	V_{SSQ}	$V_{IL(AC)}$	mV	5

Notes:
1. CK/CK# and DK*x*/DK*x*# are referenced to V_{DDQ} and V_{SSQ}.
2. Differential input slew rate = 2 V/ns.
3. Defines slew rate reference points, relative to input crossing voltages.
4. Maximum limit is relative to single-ended signals; overshoot specifications are applicable.
5. Minimum limit is relative to single-ended signals; undershoot specifications are applicable.
6. The typical value of V_{IX} is expected to be about 0.5 × V_{DDQ} of the transmitting device and V_{IX} is expected to track variations in V_{DDQ}. V_{IX} indicates the voltage at which differential input signals must cross.

Figure 9: V_{IX} for Differential Signals