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# RLDRAM 3

**MT44K32M18 – 2 Meg x 18 x 16 Banks**

**MT44K16M36 – 1 Meg x 36 x 16 Banks**

## Features

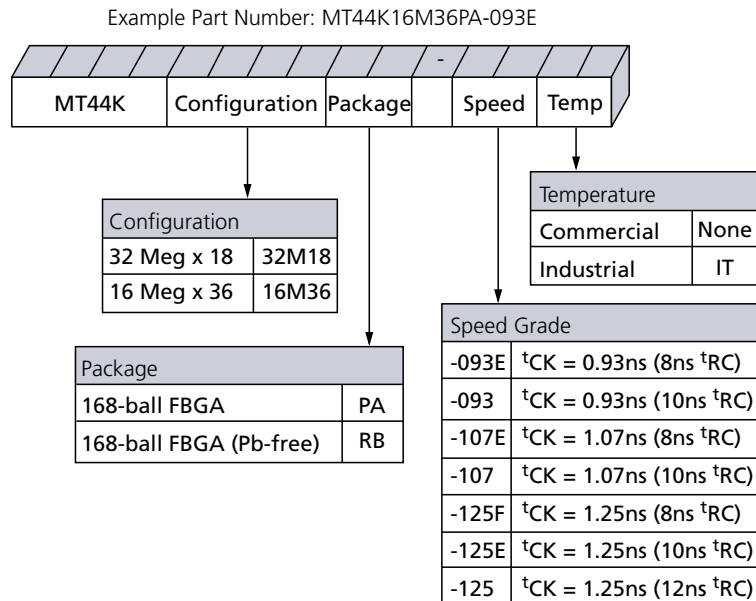
- 1066 MHz DDR operation (2133 Mb/s/ball data rate)
- 76.8 Gb/s peak bandwidth (x36 at 1066 MHz clock frequency)
- Organization
  - 32 Meg x 18, and 16 Meg x 36 common I/O (CIO)
  - 16 banks
- 1.2V center-terminated push/pull I/O
- 2.5V<sub>V<sub>EXT</sub></sub>, 1.35V<sub>V<sub>DD</sub></sub>, 1.2V<sub>V<sub>DDQ</sub></sub> I/O
- Reduced cycle time (<sup>t</sup>RC (MIN) = 8 - 12ns)
- SDR addressing
- Programmable READ/WRITE latency (RL/WL) and burst length
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Free-running differential input data clocks (DKx, DKx#) and output data clocks (QKx, QKx#)
- On-die DLL generates CK edge-aligned data and differential output data clock signals
- 64ms refresh (128K refresh per 64ms)
- 168-ball FBGA package
- 40Ω or 60Ω matched impedance outputs
- Integrated on-die termination (ODT)
- Single or multibank writes
- Extended operating range (200–1066 MHz)
- READ training register
- Multiplexed and non-multiplexed addressing capabilities
- Mirror function
- Output driver and ODT calibration
- JTAG interface (IEEE 1149.1-2001)

## Options<sup>1</sup>

- Clock cycle and <sup>t</sup>RC timing
  - 0.93ns and <sup>t</sup>RC (MIN) = 8ns (RL3-2133) -093E
  - 0.93ns and <sup>t</sup>RC (MIN) = 10ns (RL3-2133) -093
  - 1.07ns and <sup>t</sup>RC (MIN) = 8ns (RL3-1866) -107E
  - 1.07ns and <sup>t</sup>RC (MIN) = 10ns (RL3-1866) -107
  - 1.25ns and <sup>t</sup>RC (MIN) = 8ns (RL3-1600) -125F
  - 1.25ns and <sup>t</sup>RC (MIN) = 10ns (RL3-1600) -125E
  - 1.25ns and <sup>t</sup>RC (MIN) = 12ns (RL3-1600) -125
- Configuration
  - 32 Meg x 18 32M18
  - 16 Meg x 36 16M36
- Operating temperature
  - Commercial (T<sub>C</sub> = 0° to +95°C) None
  - Industrial (T<sub>C</sub> = -40°C to +95°C) IT
- Package
  - 168-ball FBGA PA<sup>2</sup>
  - 168-ball FBGA (Pb-free) RB
- Revision :A

- Notes:
1. Not all options listed can be combined to define an offered product. Use the part catalog search on [www.micron.com](http://www.micron.com) for available offerings.
  2. Consult factory.

**Figure 1: 576Mb RDRAM® 3 Part Numbers**



### BGA Part Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. Micron's BGA Part Marking Decoder is available on Micron's Web site at [www.micron.com](http://www.micron.com).

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## General Description

The Micron® RLD RAM® 3 is a high-speed memory device designed for high-bandwidth data storage—telecommunications, networking, cache applications, etc. The chip's 16-bank architecture is optimized for sustainable high-speed operation.

The DDR I/O interface transfers two data bits per clock cycle at the I/O balls. Output data is referenced to the READ strobes.

Commands, addresses, and control signals are also registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data strobes.

Read and write accesses to the RL3 device are burst-oriented. The burst length (BL) is programmable to 2, 4, or 8 by a setting in the mode register.

The device is supplied with 1.35V for the core and 1.2V for the output drivers. The 2.5V supply is used for an internal supply.

Bank-scheduled refresh is supported with the row address generated internally.

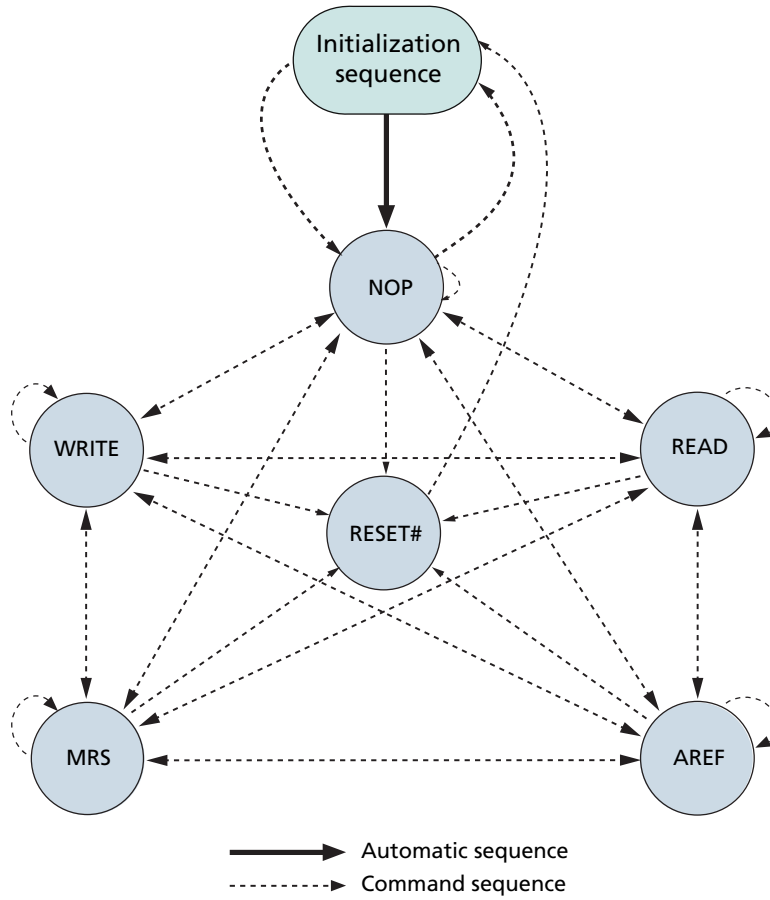
The 168-ball FBGA package is used to enable ultra-high-speed data transfer rates.

## General Notes

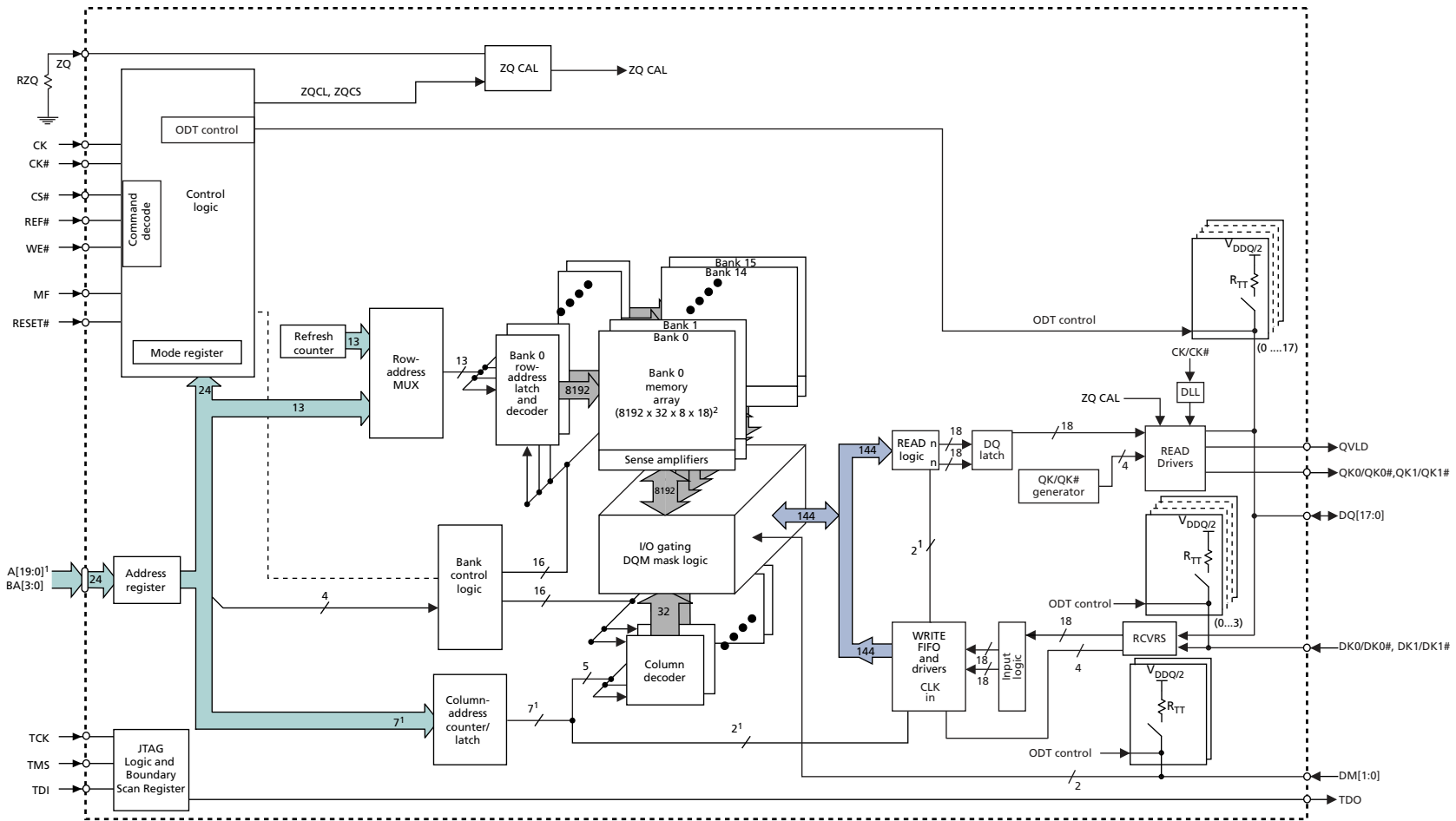
- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Nominal conditions are assumed for specifications not defined within the figures shown in this data sheet.
- Throughout this data sheet, the terms "RLDRAM," "DRAM," and "RLDRAM 3" are all used interchangeably and refer to the RLD RAM 3 SDRAM device.
- References to DQ, DK, QK, DM, and QVLD are to be interpreted as each group collectively, unless specifically stated otherwise. This includes true and complement signals of differential signals.
- Non-multiplexed operation is assumed if not specified as multiplexed.
- A X36 Device supplies four QK/QK# sets. One per 9 DQs. If a user only wants to use two QK/QK# sets, this is allowed. The user needs to use QK0/QK0# and QK1/QK1#. QK0/QK0# will control DQ[8:0] & DQ[26:18]. QK1/QK1# will control DQ[17:9] & DQ[35:27]. The QK to DQ timing parameter to be used would be <sup>t</sup>QKQ02, <sup>t</sup>QKQ13. The unused QK/QK# pins should be left floating.

## State Diagram

Figure 2: Simplified State Diagram

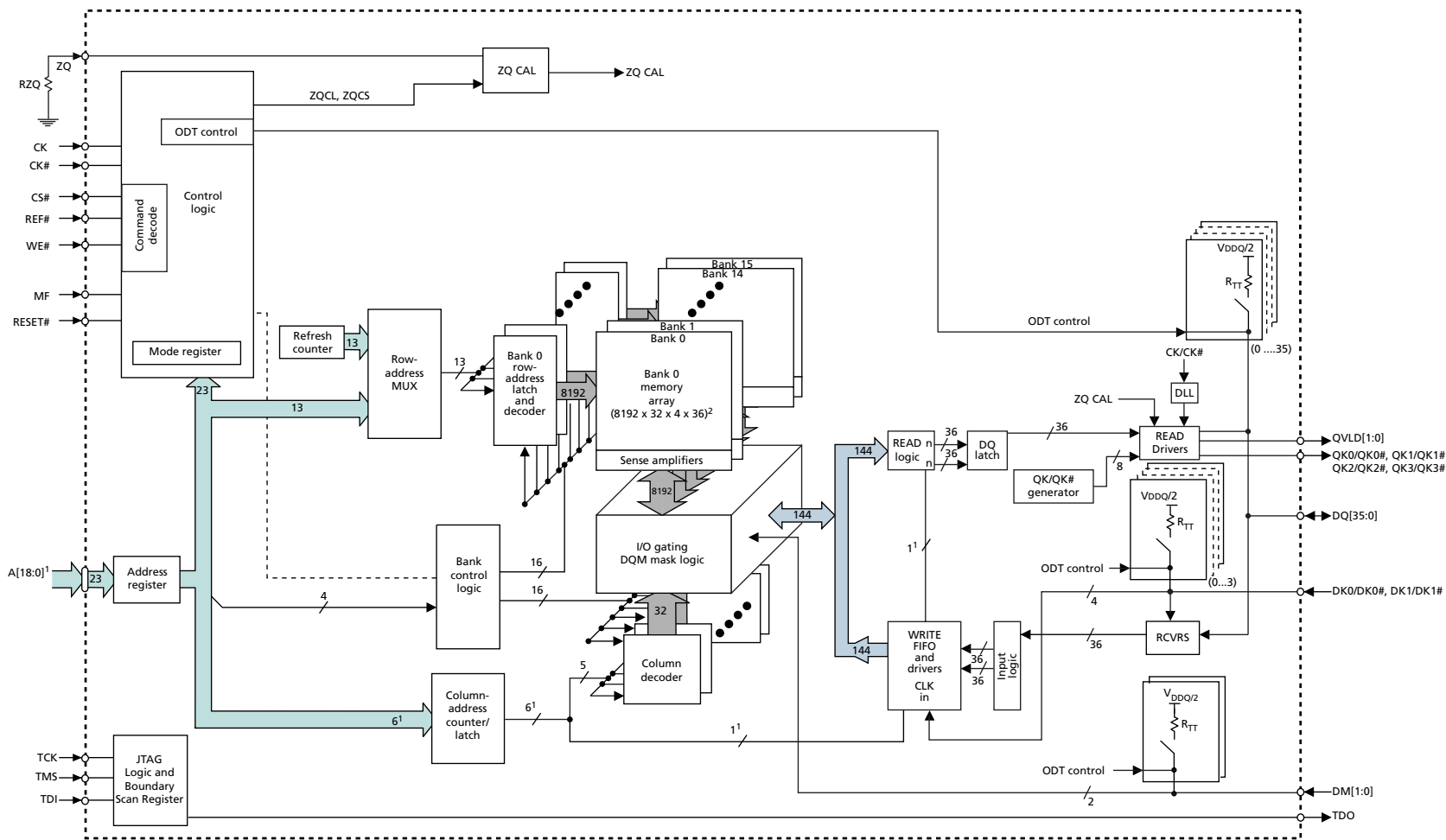


# Functional Block Diagrams

**Figure 3: 32 Meg x 18 Functional Block Diagram**


- Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
  2.  $8 = (\text{length of burst}) \times 2^{\wedge} (\text{number of column addresses to WRITE FIFO and READ logic})$ .

# Functional Block Diagrams

**Figure 4: 16 Meg x 36 Functional Block Diagram**


- Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
  2.  $4 = (\text{length of burst}) \times 2^{\wedge} (\text{number of column addresses to WRITE FIFO and READ logic})$ .

## Ball Assignments and Descriptions

**Table 1: 32 Meg x 18 Ball Assignments – 168-Ball FBGA (Top View)**

|          | 1                                 | 2                                    | 3                | 4                | 5                | 6                | 7                | 8                | 9                | 10               | 11               | 12               | 13                                 |
|----------|-----------------------------------|--------------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------------------------|
| <b>A</b> |                                   | V <sub>SS</sub>                      | V <sub>DD</sub>  | NF               | V <sub>DDQ</sub> | NF               | V <sub>REF</sub> | DQ7              | V <sub>DDQ</sub> | DQ8              | V <sub>DD</sub>  | V <sub>SS</sub>  | RESET#                             |
| <b>B</b> | V <sub>EXT</sub>                  | V <sub>SS</sub>                      | NF               | V <sub>SSQ</sub> | NF               | V <sub>DDQ</sub> | DM0              | V <sub>DDQ</sub> | DQ5              | V <sub>SSQ</sub> | DQ6              | V <sub>SS</sub>  | V <sub>EXT</sub>                   |
| <b>C</b> | V <sub>DD</sub>                   | NF                                   | V <sub>DDQ</sub> | NF               | V <sub>SSQ</sub> | NF               | DK0#             | DQ2              | V <sub>SSQ</sub> | DQ3              | V <sub>DDQ</sub> | DQ4              | V <sub>DD</sub>                    |
| <b>D</b> | A11                               | V <sub>SSQ</sub>                     | NF               | V <sub>DDQ</sub> | NF               | V <sub>SSQ</sub> | DK0              | V <sub>SSQ</sub> | QK0              | V <sub>DDQ</sub> | DQ0              | V <sub>SSQ</sub> | A13                                |
| <b>E</b> | V <sub>SS</sub>                   | A0                                   | V <sub>SSQ</sub> | NF               | V <sub>DDQ</sub> | NF               | MF               | QK0#             | V <sub>DDQ</sub> | DQ1              | V <sub>SSQ</sub> | CS#              | V <sub>SS</sub>                    |
| <b>F</b> | A7                                | NF <sub>(CS1/A20)</sub> <sup>1</sup> | V <sub>DD</sub>  | A2               | A1               | WE#              | ZQ               | REF#             | A3               | A4               | V <sub>DD</sub>  | A5               | A9                                 |
| <b>G</b> | V <sub>SS(A21)</sub> <sup>2</sup> | A15                                  | A6               | V <sub>SS</sub>  | BA1              | V <sub>SS</sub>  | CK#              | V <sub>SS</sub>  | BA0              | V <sub>SS</sub>  | A8               | A18              | V <sub>SS (RFU)</sub> <sup>3</sup> |
| <b>H</b> | A19                               | V <sub>DD</sub>                      | A14              | A16              | V <sub>DD</sub>  | BA3              | CK               | BA2              | V <sub>DD</sub>  | A17              | A12              | V <sub>DD</sub>  | A10                                |
| <b>J</b> | V <sub>DDQ</sub>                  | NF                                   | V <sub>SSQ</sub> | NF               | V <sub>DDQ</sub> | NF               | V <sub>SS</sub>  | QK1#             | V <sub>DDQ</sub> | DQ9              | V <sub>SSQ</sub> | QVLD             | V <sub>DDQ</sub>                   |
| <b>K</b> | NF                                | V <sub>SSQ</sub>                     | NF               | V <sub>DDQ</sub> | NF               | V <sub>SSQ</sub> | DK1              | V <sub>SSQ</sub> | QK1              | V <sub>DDQ</sub> | DQ10             | V <sub>SSQ</sub> | DQ11                               |
| <b>L</b> | V <sub>DD</sub>                   | NF                                   | V <sub>DDQ</sub> | NF               | V <sub>SSQ</sub> | NF               | DK1#             | DQ12             | V <sub>SSQ</sub> | DQ13             | V <sub>DDQ</sub> | DQ14             | V <sub>DD</sub>                    |
| <b>M</b> | V <sub>EXT</sub>                  | V <sub>SS</sub>                      | NF               | V <sub>SSQ</sub> | NF               | V <sub>DDQ</sub> | DM1              | V <sub>DDQ</sub> | DQ15             | V <sub>SSQ</sub> | DQ16             | V <sub>SS</sub>  | V <sub>EXT</sub>                   |
| <b>N</b> | V <sub>SS</sub>                   | TCK                                  | V <sub>DD</sub>  | TDO              | V <sub>DDQ</sub> | NF               | V <sub>REF</sub> | DQ17             | V <sub>DDQ</sub> | TDI              | V <sub>DD</sub>  | TMS              | V <sub>SS</sub>                    |

- Notes:
1. F2 is an NF ball for both the X18 & X36 576Mb devices, but is also the Location of CS1 to support the 1Gb x18 DDP device. This same ball has been designated as the location of A20 for the future 2Gb monolithic device. F2 is Internally connected so it can mirror the A5 address signal when MF is asserted HIGH and has parasitic characteristics of an address pin.
  2. G1 is a VSS ball for the 576Mb device, but has been designated as the location of A21 for the future X18 2Gb monolithic device.
  3. G13 is a VSS ball for both X18 & X36 576Mb devices, but has been reserved for future use (RFU) on the 1Gb & 2Gb monolithic devices and will have parasitic characteristics of an address.
  4. NF balls for the x18 configuration are internally connected and have parasitic characteristics of an I/O. Balls may be connected to V<sub>SSQ</sub>.
  5. MF is assumed to be tied LOW for this ball assignment.

**Table 2: 16 Meg x 36 Ball Assignments – 168-Ball FBGA (Top View)**

|          | 1                                | 2                                    | 3                | 4                | 5                | 6                | 7                | 8                | 9                | 10               | 11               | 12               | 13                                 |
|----------|----------------------------------|--------------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------------------------|
| <b>A</b> |                                  | V <sub>SS</sub>                      | V <sub>DD</sub>  | DQ26             | V <sub>DDQ</sub> | DQ25             | V <sub>REF</sub> | DQ7              | V <sub>DDQ</sub> | DQ8              | V <sub>DD</sub>  | V <sub>SS</sub>  | RESET#                             |
| <b>B</b> | V <sub>EXT</sub>                 | V <sub>SS</sub>                      | DQ24             | V <sub>SSQ</sub> | DQ23             | V <sub>DDQ</sub> | DM0              | V <sub>DDQ</sub> | DQ5              | V <sub>SSQ</sub> | DQ6              | V <sub>SS</sub>  | V <sub>EXT</sub>                   |
| <b>C</b> | V <sub>DD</sub>                  | DQ22                                 | V <sub>DDQ</sub> | DQ21             | V <sub>SSQ</sub> | DQ20             | DK0#             | DQ2              | V <sub>SSQ</sub> | DQ3              | V <sub>DDQ</sub> | DQ4              | V <sub>DD</sub>                    |
| <b>D</b> | A11                              | V <sub>SSQ</sub>                     | DQ18             | V <sub>DDQ</sub> | QK2              | V <sub>SSQ</sub> | DK0              | V <sub>SSQ</sub> | QK0              | V <sub>DDQ</sub> | DQ0              | V <sub>SSQ</sub> | A13                                |
| <b>E</b> | V <sub>SS</sub>                  | A0                                   | V <sub>SSQ</sub> | DQ19             | V <sub>DDQ</sub> | QK2#             | MF               | QK0#             | V <sub>DDQ</sub> | DQ1              | V <sub>SSQ</sub> | CS#              | V <sub>SS</sub>                    |
| <b>F</b> | A7                               | NF <sub>(CS1/A20)</sub> <sup>1</sup> | V <sub>DD</sub>  | A2               | A1               | WE#              | ZQ               | REF#             | A3               | A4               | V <sub>DD</sub>  | A5               | A9                                 |
| <b>G</b> | V <sub>SS(NF)</sub> <sup>2</sup> | A15                                  | A6               | V <sub>SS</sub>  | BA1              | V <sub>SS</sub>  | CK#              | V <sub>SS</sub>  | BA0              | V <sub>SS</sub>  | A8               | A18              | V <sub>SS (RFU)</sub> <sup>3</sup> |
| <b>H</b> | NF <sub>(A19)</sub> <sup>4</sup> | V <sub>DD</sub>                      | A14              | A16              | V <sub>DD</sub>  | BA3              | CK               | BA2              | V <sub>DD</sub>  | A17              | A12              | V <sub>DD</sub>  | A10                                |
| <b>J</b> | V <sub>DDQ</sub>                 | QVLD1                                | V <sub>SSQ</sub> | DQ27             | V <sub>DDQ</sub> | QK3#             | V <sub>SS</sub>  | QK1#             | V <sub>DDQ</sub> | DQ9              | V <sub>SSQ</sub> | QVLD0            | V <sub>DDQ</sub>                   |
| <b>K</b> | DQ29                             | V <sub>SSQ</sub>                     | DQ28             | V <sub>DDQ</sub> | QK3              | V <sub>SSQ</sub> | DK1              | V <sub>SSQ</sub> | QK1              | V <sub>DDQ</sub> | DQ10             | V <sub>SSQ</sub> | DQ11                               |
| <b>L</b> | V <sub>DD</sub>                  | DQ32                                 | V <sub>DDQ</sub> | DQ31             | V <sub>SSQ</sub> | DQ30             | DK1#             | DQ12             | V <sub>SSQ</sub> | DQ13             | V <sub>DDQ</sub> | DQ14             | V <sub>DD</sub>                    |
| <b>M</b> | V <sub>EXT</sub>                 | V <sub>SS</sub>                      | DQ34             | V <sub>SSQ</sub> | DQ33             | V <sub>DDQ</sub> | DM1              | V <sub>DDQ</sub> | DQ15             | V <sub>SSQ</sub> | DQ16             | V <sub>SS</sub>  | V <sub>EXT</sub>                   |
| <b>N</b> | V <sub>SS</sub>                  | TCK                                  | V <sub>DD</sub>  | TDO              | V <sub>DDQ</sub> | DQ35             | V <sub>REF</sub> | DQ17             | V <sub>DDQ</sub> | TDI              | V <sub>DD</sub>  | TMS              | V <sub>SS</sub>                    |

- Notes:
1. F2 is an NF ball for both the X18 & X36 576Mb devices, but is also the Location of CS1 to support the 1Gb x18 DDP device. This same ball has been designated as the location of A20 for the future 2Gb monolithic device. F2 is Internally connected so it can mirror the A5 address signal when MF is asserted HIGH and has parasitic characteristics of an address pin.
  2. G1 is a VSS ball for this 576Mb device, but will be an NF ball for the future X36 2Gb monolithic device. The NF ball (A21 for X18 2Gb device) will have parasitic characteristics of an address.
  3. G13 is a VSS ball for both X18 & X36 576Mb devices, but has been reserved for future use (RFU) on the 1Gb & 2Gb monolithic devices and will have parasitic characteristics of an address.
  4. NF ball for x36 configuration is internally connected and has parasitic characteristics of an address (A19 for x18 configuration). Ball may be connected to V<sub>SSQ</sub>.
  5. MF is assumed to be tied LOW for this ball assignment.

**Table 3: Ball Descriptions**

| Symbol    | Type   | Description   |
|-----------|--------|---|
| A[19:0]   | Input  | <b>Address inputs:</b> A[19:0] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings along with BA[3:0]. They are sampled at the rising edge of CK.  |
| BA[3:0]   | Input  | <b>Bank address inputs:</b> Select the internal bank to which a command is being applied.   |
| CK/CK#    | Input  | <b>Input clock:</b> CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK.  |
| CS#       | Input  | <b>Chip select:</b> CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.   |
| DQ[35:0]  | I/O    | <b>Data input:</b> The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK. During WRITE commands, the data is sampled at both edges of DK.   |
| DKx, DKx# | Input  | <b>Input data clock:</b> DKx and DKx# are differential input data clocks. All input data is referenced to both edges of DKx. For the x36 device, DQ[8:0] and DQ[26:18] are referenced to DK0 and DK0#, and DQ[17:9] and DQ[35:27] are referenced to DK1 and DK1#. For the x18 device, DQ[8:0] are referenced to DK0 and DK0#, and DQ[17:9] are referenced to DK1 and DK1#. DKx and DKx# are free-running signals and must always be supplied to the device.                                 |
| DM[1:0]   | Input  | <b>Input data mask:</b> DM is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM0 is used to mask the lower byte for the x18 device and DQ[8:0] and DQ[26:18] for the x36 device. DM1 is used to mask the upper byte for the x18 device and DQ[17:9] and DQ[35:27] for the x36 device. Tie DM[1:0] to V <sub>SS</sub> if not used.  |
| TCK       | Input  | <b>IEEE 1149.1 clock input:</b> This ball must be tied to V <sub>SS</sub> if the JTAG function is not used.   |
| TMS, TDI  | Input  | <b>IEEE 1149.1 test inputs:</b> These balls may be left as no connects if the JTAG function is not used.  |
| WE#, REF# | Input  | <b>Command inputs:</b> Sampled at the positive edge of CK, WE# and REF# (together with CS#) define the command to be executed.  |
| RESET#    | Input  | <b>Reset:</b> RESET# is an active LOW CMOS input referenced to V <sub>SS</sub> . RESET# assertion and deassertion are asynchronous. RESET# is a CMOS input defined with DC HIGH $\geq 0.8 \times V_{DD}$ and DC LOW $\leq 0.2 \times V_{DDQ}$ .   |
| ZQ        | Input  | <b>External impedance:</b> This signal is used to tune the device's output impedance and ODT. RZQ needs to be 240 $\Omega$ , where RZQ is a resistor from this signal to ground.  |
| QKx, QKx# | Output | <b>Output data clocks:</b> QK and QK# are opposite-polarity output data clocks. They are free-running signals and during READ commands are edge-aligned with the DQs. For the x36 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9]; QK2, QK2# align with DQ[26:18]; QK3, QK3# align with DQ[35:27]. For the x18 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9].   |
| QVLDx     | Output | <b>Data valid:</b> The QVLD ball indicates that valid output data will be available on the subsequent rising clock edge. There is a single QVLD ball for the x18 device and two, QVLD0 and QVLD1, for the x36 device. QVLD0 aligns with DQ[17:0]; QVLD1 aligns with DQ[35:18].  |
| MF        | Input  | <b>Mirror function:</b> The mirror function ball is a DC input used to create mirrored ballouts for simple dual-loaded clamshell mounting. If the ball is tied to V <sub>SS</sub> , the address and command balls are in their true layout. If the ball is tied to V <sub>DDQ</sub> , they are in the complement location. MF must be tied HIGH or LOW and cannot be left floating. MF is a CMOS input defined with DC HIGH $\geq 0.8 \times V_{DD}$ and DC LOW $\leq 0.2 \times V_{DDQ}$ . |

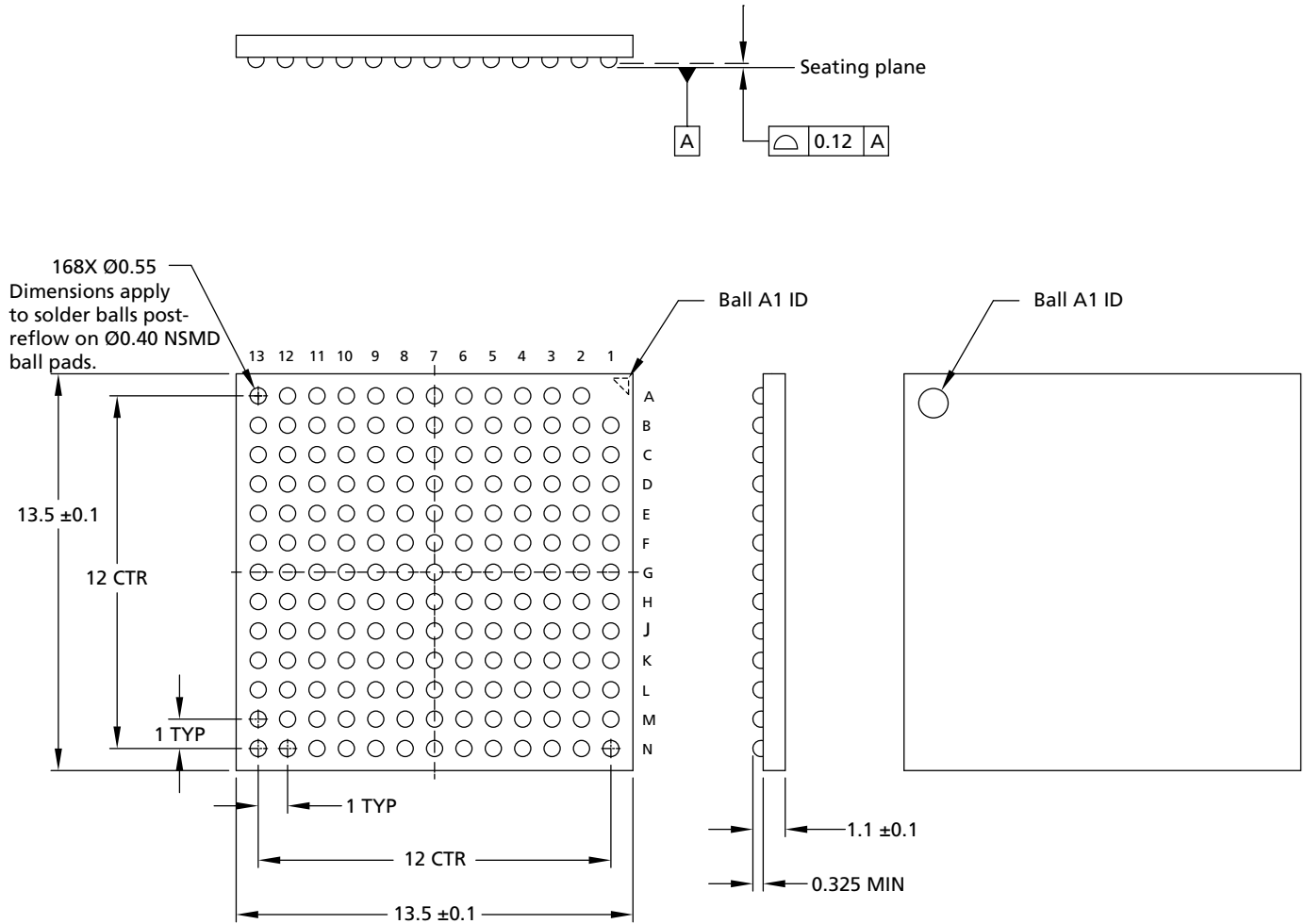
**Table 3: Ball Descriptions (Continued)**

| Symbol           | Type   | Description  |
|------------------|--------|--|
| TDO              | Output | <b>IEEE 1149.1 test output:</b> JTAG output. This ball may be left as no connect if the JTAG function is not used.         |
| V <sub>DD</sub>  | Supply | <b>Power supply:</b> 1.35V nominal. See Table 7 (page 22) for range.   |
| V <sub>DDQ</sub> | Supply | <b>DQ power supply:</b> 1.2V nominal. Isolated on the device for improved noise immunity. See Table 7 (page 22) for range. |
| V <sub>EXT</sub> | Supply | <b>Power supply:</b> 2.5V nominal. See Table 7 (page 22) for range.  |
| V <sub>REF</sub> | Supply | <b>Input reference voltage:</b> V <sub>DDQ</sub> /2 nominal. Provides a reference voltage for the input buffers.           |
| V <sub>SS</sub>  | Supply | Ground.  |
| V <sub>SSQ</sub> | Supply | <b>DQ ground:</b> Isolated on the device for improved noise immunity.  |
| NC               | –      | <b>No connect:</b> These balls are not connected to the DRAM.  |
| NF               | –      | <b>No function:</b> These balls are connected to the DRAM, but provide no functionality.                                   |



## Package Dimensions

Figure 5: 168-Ball FBGA



Note: 1. All dimensions are in millimeters.

## Electrical Characteristics – I<sub>DD</sub> Specifications

**Table 4: I<sub>DD</sub> Operating Conditions and Maximum Limits**

Notes 1–6 apply to the entire table

| Description                  | Condition   | Symbol                                   | -093E | -093 | -107E | -107 | -125F | -125E | -125 | Units | Notes |
|------------------------------|---|--|-------|------|-------|------|-------|-------|------|-------|-------|
| Standby current              | <sup>t</sup> CK = idle; All banks idle; No inputs toggling  | I <sub>SB1</sub> (V <sub>DD</sub> ) x18  | 125   | 125  | 125   | 125  | 125   | 125   | 125  | mA    | 7     |
|                              |   | I <sub>SB1</sub> (V <sub>DD</sub> ) x36  | 125   | 125  | 125   | 125  | 125   | 125   | 125  |       |       |
|                              |   | I <sub>SB1</sub> (V <sub>EXT</sub> )     | 30    | 30   | 30    | 30   | 30    | 30    | 30   |       |       |
| Clock active standby current | CS# = 1; No commands; Bank address incremented and half address/data change once every four clock cycles  | I <sub>SB2</sub> (V <sub>DD</sub> ) x18  | 870   | 870  | 815   | 815  | 725   | 725   | 725  | mA    |       |
|                              |   | I <sub>SB2</sub> (V <sub>DD</sub> ) x36  | 895   | 895  | 835   | 835  | 740   | 740   | 740  |       |       |
|                              |   | I <sub>SB2</sub> (V <sub>EXT</sub> )     | 30    | 30   | 30    | 30   | 30    | 30    | 30   |       |       |
| Operational current: BL2     | BL = 2; Sequential bank access; Bank transitions once every <sup>t</sup> RC; Half address transitions once every <sup>t</sup> RC; Read followed by write sequence; Continuous data during WRITE commands    | I <sub>DD1</sub> (V <sub>DD</sub> ) x18  | 1175  | 1115 | 1100  | 1045 | 990   | 940   | 915  | mA    |       |
|                              |   | I <sub>DD1</sub> (V <sub>DD</sub> ) x36  | 1185  | 1125 | 1110  | 1055 | 1000  | 950   | 925  |       |       |
|                              |   | I <sub>DD1</sub> (V <sub>EXT</sub> )     | 35    | 35   | 35    | 35   | 35    | 35    | 35   |       |       |
| Operational current: BL4     | BL = 4; Sequential bank access; Bank transitions once every <sup>t</sup> RC; Half address transitions once every <sup>t</sup> RC; Read followed by write sequence; Continuous data during WRITE commands    | I <sub>DD2</sub> (V <sub>DD</sub> ) x18  | 1205  | 1145 | 1130  | 1075 | 1020  | 970   | 945  | mA    |       |
|                              |   | I <sub>DD2</sub> (V <sub>DD</sub> ) x36  | 1215  | 1155 | 1140  | 1080 | 1030  | 980   | 950  |       |       |
|                              |   | I <sub>DD2</sub> (V <sub>EXT</sub> )     | 35    | 35   | 35    | 35   | 35    | 35    | 35   |       |       |
| Operational current: BL8     | BL = 8; Sequential bank access; Bank transitions once every <sup>t</sup> RC; Half address transitions once every <sup>t</sup> RC; Read followed by write sequence; Continuous data during WRITE commands    | I <sub>DD3</sub> (V <sub>DD</sub> ) x18  | 1300  | 1220 | 1200  | 1130 | 1085  | 1030  | 1000 | mA    |       |
|                              |   | I <sub>DD3</sub> (V <sub>DD</sub> ) x36  | NA    | NA   | NA    | NA   | N/A   | NA    | NA   |       |       |
|                              |   | I <sub>DD3</sub> (V <sub>EXT</sub> )     | 35    | 35   | 35    | 35   | 35    | 35    | 35   |       |       |
| Burst refresh current        | Sixteen bank cyclic refresh using Bank Address Control AREF protocol; Command bus remains in refresh for all sixteen banks; DQs are High-Z and at V <sub>DDQ</sub> /2; Addresses are at V <sub>DDQ</sub> /2 | I <sub>REF1</sub> (V <sub>DD</sub> ) x18 | 1550  | 1550 | 1400  | 1400 | 1230  | 1230  | 1230 | mA    |       |
|                              |   | I <sub>REF1</sub> (V <sub>DD</sub> ) x36 | 1570  | 1570 | 1420  | 1420 | 1245  | 1245  | 1245 |       |       |
|                              |   | I <sub>REF1</sub> (V <sub>EXT</sub> )    | 80    | 80   | 75    | 75   | 70    | 70    | 70   |       |       |

**Table 4: I<sub>DD</sub> Operating Conditions and Maximum Limits (Continued)**

Notes 1–6 apply to the entire table

| Description                               | Condition  | Symbol                                     | -093E | -093 | -107E | -107 | -125F | -125E | -125 | Units | Notes |
|---|--|--|-------|------|-------|------|-------|-------|------|-------|-------|
| Distributed refresh current               | Single bank refresh using Bank Address Control AREF protocol; Sequential bank access every 0.489μs; DQs are High-Z and at V <sub>DDQ</sub> /2; Addresses are at V <sub>DDQ</sub> /2  | I <sub>REF2</sub> (V <sub>DD</sub> ) x18   | 875   | 875  | 820   | 820  | 730   | 730   | 730  | mA    |       |
|   |  | I <sub>REF2</sub> (V <sub>DD</sub> ) x36   | 900   | 900  | 840   | 840  | 745   | 745   | 745  |       |       |
|   |  | I <sub>REF2</sub> (V <sub>EXT</sub> )      | 30    | 30   | 30    | 30   | 30    | 30    | 30   |       |       |
| Multibank refresh current: 4 bank refresh | Quad bank refresh using Multibank AREF protocol; BL = 4; Cyclic bank access; Subject to <sup>t</sup> SAW and <sup>t</sup> MMD specifications; DQs are High-Z and at V <sub>DDQ</sub> /2; Bank addresses are at V <sub>DDQ</sub> /2 | I <sub>MBREF4</sub> (V <sub>DD</sub> ) x18 | 2130  | 1925 | 2030  | 1810 | 1885  | 1885  | 1645 | mA    |       |
|   |  | I <sub>MBREF4</sub> (V <sub>DD</sub> ) x36 | 2155  | 1950 | 2050  | 1830 | 1900  | 1900  | 1660 |       |       |
|   |  | I <sub>MBREF4</sub> (V <sub>EXT</sub> )    | 130   | 130  | 115   | 115  | 105   | 105   | 105  |       |       |
| Operating burst write current : BL2       | BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous WRITE   | I <sub>DD2W</sub> (V <sub>DD</sub> ) x18   | 2110  | 2110 | 1910  | 1910 | 1665  | 1665  | 1665 | mA    |       |
|   |  | I <sub>DD2W</sub> (V <sub>DD</sub> ) x36   | 2290  | 2290 | 2070  | 2070 | 1805  | 1805  | 1805 |       |       |
|   |  | I <sub>DD2W</sub> (V <sub>EXT</sub> )      | 80    | 80   | 75    | 75   | 70    | 70    | 70   |       |       |
| Operating burst write current : BL4       | BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE  | I <sub>DD4W</sub> (V <sub>DD</sub> ) x18   | 1730  | 1730 | 1590  | 1590 | 1395  | 1395  | 1395 | mA    |       |
|   |  | I <sub>DD4W</sub> (V <sub>DD</sub> ) x36   | 1815  | 1815 | 1665  | 1665 | 1460  | 1460  | 1460 |       |       |
|   |  | I <sub>DD4W</sub> (V <sub>EXT</sub> )      | 55    | 55   | 55    | 55   | 50    | 50    | 50   |       |       |
| Operating burst write current :BL8        | BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous WRITE   | I <sub>DD8W</sub> (V <sub>DD</sub> ) x18   | 1475  | 1475 | 1335  | 1335 | 1190  | 1190  | 1190 | mA    |       |
|   |  | I <sub>DD8W</sub> (V <sub>DD</sub> ) x36   | NA    | NA   | NA    | NA   | NA    | NA    | NA   |       |       |
|   |  | I <sub>DD8W</sub> (V <sub>EXT</sub> )      | 45    | 45   | 40    | 40   | 40    | 40    | 40   |       |       |
| Multibank write current: Dual bank write  | BL = 4; Cyclic bank access using Dual Bank WRITE; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE  | I <sub>DBWR</sub> (V <sub>DD</sub> ) x18   | 2305  | 2305 | 2170  | 2170 | 1885  | 1885  | 1885 | mA    |       |
|   |  | I <sub>DBWR</sub> (V <sub>DD</sub> ) x36   | 2400  | 2400 | 2250  | 2250 | 1960  | 1960  | 1960 |       |       |
|   |  | I <sub>DBWR</sub> (V <sub>EXT</sub> )      | 80    | 80   | 75    | 75   | 70    | 70    | 70   |       |       |
| Multibank write current: Quad bank write  | BL = 4; Cyclic bank access using Quad Bank WRITE; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE; Subject to <sup>t</sup> SAW specification                     | I <sub>QBWR</sub> (V <sub>DD</sub> ) x18   | 2965  | 2965 | 2890  | 2890 | 2525  | 2525  | 2525 | mA    |       |
|   |  | I <sub>QBWR</sub> (V <sub>DD</sub> ) x36   | 3195  | 3195 | 3000  | 3000 | 2615  | 2615  | 2615 |       |       |
|   |  | I <sub>QBWR</sub> (V <sub>EXT</sub> )      | 130   | 130  | 115   | 115  | 100   | 100   | 100  |       |       |

**Table 4: I<sub>DD</sub> Operating Conditions and Maximum Limits (Continued)**

Notes 1–6 apply to the entire table

| Description                          | Condition   | Symbol                                   | -093E | -093 | -107E | -107 | -125F | -125E | -125 | Units | Notes |
|--------------------------------------|---|--|-------|------|-------|------|-------|-------|------|-------|-------|
| Operating burst read current example | BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous READ       | I <sub>DD2R</sub> (V <sub>DD</sub> ) x18 | 2250  | 2250 | 2045  | 2045 | 1785  | 1785  | 1785 | mA    |       |
|                                      |   | I <sub>DD2R</sub> (V <sub>DD</sub> ) x36 | 2395  | 2395 | 2180  | 2180 | 1895  | 1895  | 1895 |       |       |
|                                      |   | I <sub>DD2R</sub> (V <sub>EXT</sub> )    | 80    | 80   | 75    | 75   | 70    | 70    | 70   |       |       |
| Operating burst read current example | BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous READ  | I <sub>DD4R</sub> (V <sub>DD</sub> ) x18 | 1740  | 1740 | 1595  | 1595 | 1400  | 1400  | 1400 | mA    |       |
|                                      |   | I <sub>DD4R</sub> (V <sub>DD</sub> ) x36 | 1835  | 1835 | 1685  | 1685 | 1475  | 1475  | 1475 |       |       |
|                                      |   | I <sub>DD4R</sub> (V <sub>EXT</sub> )    | 55    | 55   | 55    | 55   | 50    | 50    | 50   |       |       |
| Operating burst read current example | BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous READ | I <sub>DD8R</sub> (V <sub>DD</sub> ) x18 | 1450  | 1450 | 1315  | 1315 | 1175  | 1175  | 1175 | mA    |       |
|                                      |   | I <sub>DD8R</sub> (V <sub>DD</sub> ) x36 | NA    | NA   | NA    | NA   | NA    | NA    | NA   |       |       |
|                                      |   | I <sub>DD8R</sub> (V <sub>EXT</sub> )    | 45    | 45   | 40    | 40   | 40    | 40    | 40   |       |       |

- Notes:
1. I<sub>DD</sub> specifications are tested after the device is properly initialized.  $0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.28\text{V} \leq V_{DD} \leq +1.42\text{V}$ ,  $+1.14\text{V} \leq V_{DDQ} \leq +1.26\text{V}$ ,  $+2.38\text{V} \leq V_{EXT} \leq +2.63\text{V}$ ,  $V_{REF} = V_{DDQ}/2$ .
  2. I<sub>DD</sub> measurements use  $t_{CK}$  (MIN),  $t_{RC}$  (MIN), and minimum data latency (RL and WL).
  3. Input slew rate is 1V/ns for single ended signals and 2V/ns for differential signals.
  4. Definitions for I<sub>DD</sub> conditions:
    - LOW is defined as  $V_{IN} \leq V_{IL(AC)MAX}$ .
    - HIGH is defined as  $V_{IN} \geq V_{IH(AC)MIN}$ .
    - Continuous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
    - Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
    - Sequential bank access is defined as the bank address incrementing by one every  $t_{RC}$ .
    - Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
  5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
  6. I<sub>DD</sub> parameters are specified with ODT disabled.
  7. Upon exiting standby current conditions, at least one NOP command must be issued with stable clock prior to issuing any other valid command.

## Electrical Specifications – Absolute Ratings and I/O Capacitance

### Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 5: Absolute Maximum Ratings**

| Symbol            | Parameter  | Min  | Max   | Units |
|-------------------|--|------|-------|-------|
| $V_{DD}$          | $V_{DD}$ supply voltage relative to $V_{SS}$     | -0.4 | 1.975 | V     |
| $V_{DDQ}$         | Voltage on $V_{DDQ}$ supply relative to $V_{SS}$ | -0.4 | 1.66  | V     |
| $V_{IN}, V_{OUT}$ | Voltage on any ball relative to $V_{SS}$         | -0.4 | 1.66  | V     |
| $V_{EXT}$         | Voltage on $V_{EXT}$ supply relative to $V_{SS}$ | -0.4 | 2.8   | V     |

### Input/Output Capacitance

**Table 6: Input/Output Capacitance**

Notes 1 and 2 apply to entire table

| Capacitance Parameters            | Symbol              | RL3-2133 |      | RL3-1866 |      | RL3-1600 |      | Units | Notes |
|-----------------------------------|---------------------|----------|------|----------|------|----------|------|-------|-------|
|                                   |                     | Min      | Max  | Min      | Max  | Min      | Max  |       |       |
| CK/CK#                            | $C_{CK}$            | 1.3      | 2.1  | 1.3      | 2.1  | 1.3      | 2.2  | pF    |       |
| $\Delta C$ : CK to CK#            | $C_{DCK}$           | 0        | 0.15 | 0        | 0.15 | 0        | 0.15 | pF    |       |
| Single-ended I/O: DQ, DM          | $C_{IO}$            | 1.9      | 2.9  | 1.9      | 3.0  | 2.0      | 3.1  | pF    | 3     |
| Input strobe: DK/DK#              | $C_{IO}$            | 1.9      | 2.9  | 1.9      | 3.0  | 2.0      | 3.1  | pF    |       |
| Output strobe: QK/QK#, QVLD       | $C_{IO}$            | 1.9      | 2.9  | 1.9      | 3.0  | 2.0      | 3.1  | pF    |       |
| $\Delta C$ : DK to DK#            | $C_{DDK}$           | 0        | 0.15 | 0        | 0.15 | 0        | 0.15 | pF    |       |
| $\Delta C$ : QK to QK#            | $C_{DQK}$           | 0        | 0.15 | 0        | 0.15 | 0        | 0.15 | pF    |       |
| $\Delta C$ : DQ to QK or DQ to DK | $C_{DIO}$           | -0.5     | 0.3  | -0.5     | 0.3  | -0.5     | 0.3  | pF    | 4     |
| Inputs (CMD, ADDR)                | $C_I$               | 1.25     | 2.25 | 1.25     | 2.25 | 1.25     | 2.25 | pF    | 5     |
| $\Delta C$ : CMD_ADDR to CK       | $C_{DI\_CMD\_ADDR}$ | -0.5     | 0.3  | -0.5     | 0.3  | -0.4     | 0.4  | pF    | 6     |
| JTAG balls                        | $C_{JTAG}$          | 1.5      | 4.5  | 1.5      | 4.5  | 1.5      | 4.5  | pF    | 7     |
| RESET#, MF balls                  | $C_I$               | -        | 3.0  | -        | 3.0  | -        | 3.0  | pF    |       |

- Notes:
- $+1.28V \leq V_{DD} \leq +1.42V$ ,  $+1.14V \leq V_{DDQ} \leq 1.26V$ ,  $+2.38V \leq V_{EXT} \leq +2.63V$ ,  $V_{REF} = V_{SS}$ ,  $f = 100$  MHz,  $T_C = 25^\circ C$ ,  $V_{OUT(DC)} = 0.5 \times V_{DDQ}$ ,  $V_{OUT}$  (peak-to-peak) = 0.1V.
  - Capacitance is not tested on ZQ ball.
  - DM input is grouped with the I/O balls, because they are matched in loading.
  - $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO} [QK] + C_{IO} [QK\#])$ .
  - Includes CS#, REF#, WE#, A[19:0], and BA[3:0].
  - $C_{DI\_CMD\_ADDR} = C_I$  (CMD\_ADDR) -  $0.5 \times (C_{CK} [CK] + C_{CK} [CK\#])$ .
  - JTAG balls are tested at 50 MHz.

## AC and DC Operating Conditions

**Table 7: DC Electrical Characteristics and Operating Conditions**

Note 1 applies to the entire table; Unless otherwise noted:  $0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.28\text{V} \leq V_{DD} \leq +1.42\text{V}$

| Description   | Symbol       | Min                   | Max                   | Units         | Notes |
|---|--------------|-----------------------|-----------------------|---------------|-------|
| Supply voltage  | $V_{EXT}$    | 2.38                  | 2.63                  | V             |       |
| Supply voltage  | $V_{DD}$     | 1.28                  | 1.42                  | V             |       |
| Isolated output buffer supply   | $V_{DDQ}$    | 1.14                  | 1.26                  | V             |       |
| Reference voltage   | $V_{REF}$    | $0.49 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V             | 2, 3  |
| Input HIGH (logic 1) voltage  | $V_{IH(DC)}$ | $V_{REF} + 0.10$      | $V_{DDQ}$             | V             |       |
| Input LOW (logic 0) voltage   | $V_{IL(DC)}$ | $V_{SS}$              | $V_{REF} - 0.10$      | V             |       |
| Input leakage current: Any input $0\text{V} \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ ball<br>$0\text{V} \leq V_{IN} \leq 1.1\text{V}$ (All other balls not under test = 0V) | $I_{LI}$     | -2                    | 2                     | $\mu\text{A}$ |       |
| Reference voltage current (All other balls not under test = 0V)   | $I_{REF}$    | -5                    | 5                     | $\mu\text{A}$ |       |

- Notes:
1. All voltages referenced to  $V_{SS}$  (GND).
  2. The nominal value of  $V_{REF}$  is expected to be  $0.5 \times V_{DDQ}$  of the transmitting device.  $V_{REF}$  is expected to track variations in  $V_{DDQ}$ .
  3. Peak-to-peak noise (non-common mode) on  $V_{REF}$  may not exceed  $\pm 2\%$  of the DC value. DC values are determined to be less than 20 MHz. Peak-to-peak AC noise on  $V_{REF}$  should not exceed  $\pm 2\%$  of  $V_{REF(DC)}$ . Thus, from  $V_{DDQ}/2$ ,  $V_{REF}$  is allowed  $\pm 2\% V_{DDQ}/2$  for DC error and an additional  $\pm 2\% V_{DDQ}/2$  for AC noise. The measurement is to be taken at the nearest  $V_{REF}$  bypass capacitor.

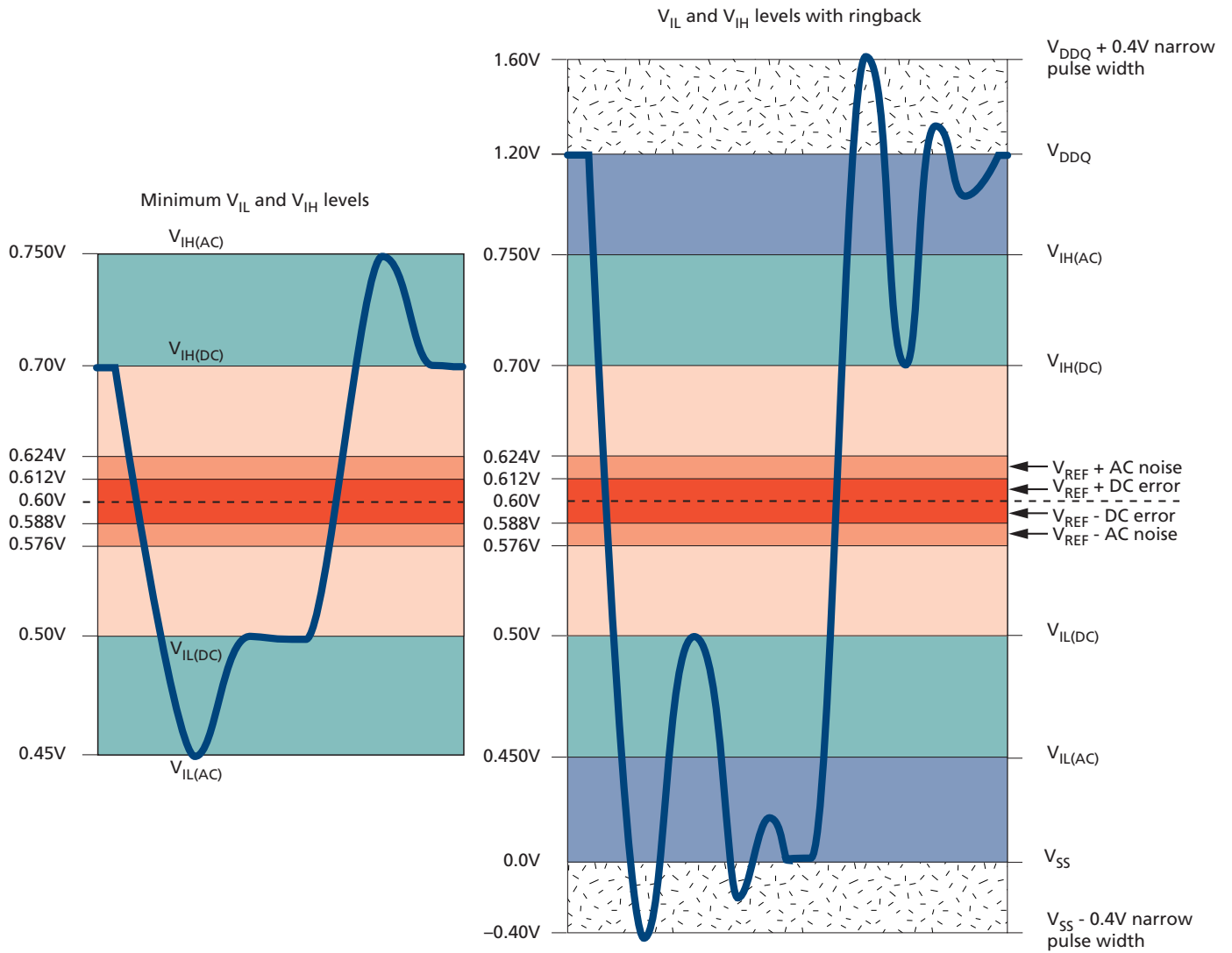
**Table 8: Input AC Logic Levels**

Notes 1-3 apply to entire table; Unless otherwise noted:  $0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.28\text{V} \leq V_{DD} \leq +1.42\text{V}$

| Description                  | Symbol       | Min              | Max              | Units |
|------------------------------|--------------|------------------|------------------|-------|
| Input HIGH (logic 1) voltage | $V_{IH(AC)}$ | $V_{REF} + 0.15$ | -                | V     |
| Input LOW (logic 0) voltage  | $V_{IL(AC)}$ | -                | $V_{REF} - 0.15$ | V     |

- Notes:
1. All voltages referenced to  $V_{SS}$  (GND).
  2. The receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above/below the DC input LOW/HIGH level.
  3. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

**Figure 6: Single-Ended Input Signal**





## AC Overshoot/Undershoot Specifications

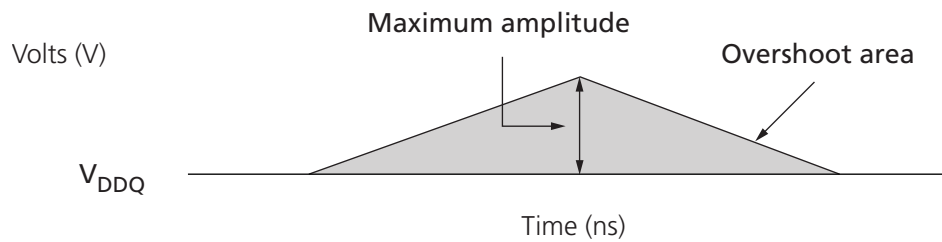
**Table 9: Control and Address Balls**

| Parameter  | RL3-2133 | RL3-1866 | RL3-1600 |
|--|----------|----------|----------|
| Maximum peak amplitude allowed for overshoot area  | 0.4V     | 0.4V     | 0.4V     |
| Maximum peak amplitude allowed for undershoot area | 0.4V     | 0.4V     | 0.4V     |
| Maximum overshoot area above $V_{DDQ}$             | 0.25 Vns | 0.28 Vns | 0.33 Vns |
| Maximum undershoot area below $V_{SS}/V_{SSQ}$     | 0.25 Vns | 0.28 Vns | 0.33 Vns |

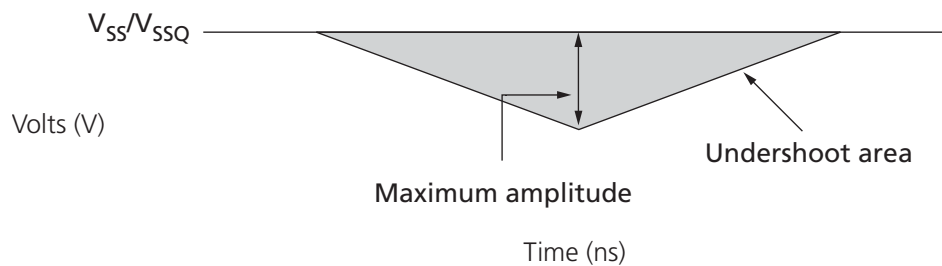
**Table 10: Clock, Data, Strobe, and Mask Balls**

| Parameter  | RL3-2133 | RL3-1866 | RL3-1600 |
|--|----------|----------|----------|
| Maximum peak amplitude allowed for overshoot area  | 0.4V     | 0.4V     | 0.4V     |
| Maximum peak amplitude allowed for undershoot area | 0.4V     | 0.4V     | 0.4V     |
| Maximum overshoot area above $V_{DDQ}$             | 0.10 Vns | 0.11 Vns | 0.13 Vns |
| Maximum undershoot area below $V_{SS}/V_{SSQ}$     | 0.10 Vns | 0.11 Vns | 0.13 Vns |

**Figure 7: Overshoot**



**Figure 8: Undershoot**



**Table 11: Differential Input Operating Conditions (CK, CK# and DKx, DKx#)**

Notes 1 and 2 apply to entire table

| Parameter/Condition  | Symbol              | Min                               | Max                               | Units | Notes |
|--|---------------------|-----------------------------------|-----------------------------------|-------|-------|
| Differential input voltage logic HIGH – slew               | $V_{IH,diff\_slew}$ | +200                              | n/a                               | mV    | 3     |
| Differential input voltage logic LOW – slew                | $V_{IL,diff\_slew}$ | n/a                               | -200                              | mV    | 3     |
| Differential input voltage logic HIGH                      | $V_{IH,diff(AC)}$   | $2 \times (V_{IH(AC)} - V_{REF})$ | $V_{DDQ}$                         | mV    | 4     |
| Differential input voltage logic LOW                       | $V_{IL,diff(AC)}$   | $V_{SSQ}$                         | $2 \times (V_{IL(AC)} - V_{REF})$ | mV    | 5     |
| Differential input crossing voltage relative to $V_{DD}/2$ | $V_{IX}$            | $V_{REF(DC)} - 150$               | $V_{REF(DC)} + 150$               | mV    | 6     |
| Single-ended HIGH level                                    | $V_{SEH}$           | $V_{IH(AC)}$                      | $V_{DDQ}$                         | mV    | 4     |
| Single-ended LOW level                                     | $V_{SEL}$           | $V_{SSQ}$                         | $V_{IL(AC)}$                      | mV    | 5     |

- Notes:
1. CK/CK# and DKx/DKx# are referenced to  $V_{DDQ}$  and  $V_{SSQ}$ .
  2. Differential input slew rate = 2 V/ns.
  3. Defines slew rate reference points, relative to input crossing voltages.
  4. Maximum limit is relative to single-ended signals; overshoot specifications are applicable.
  5. Minimum limit is relative to single-ended signals; undershoot specifications are applicable.
  6. The typical value of  $V_{IX}$  is expected to be about  $0.5 \times V_{DDQ}$  of the transmitting device and  $V_{IX}$  is expected to track variations in  $V_{DDQ}$ .  $V_{IX}$  indicates the voltage at which differential input signals must cross.

**Figure 9:  $V_{IX}$  for Differential Signals**

