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# RLDRAM 3

**MT44K64M18 – 4 Meg x 18 x 16 Banks**

**MT44K32M36 – 2 Meg x 36 x 16 Banks**

## Features

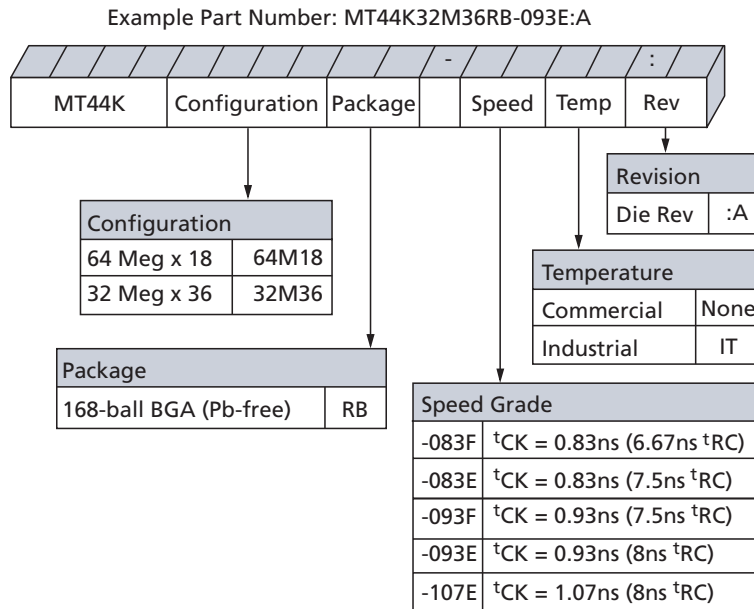
- 1200 MHz DDR operation (2400 Mb/s/ball data rate)
- 86.4Gb/s peak bandwidth (x36 at 1200 MHz clock frequency)
- Organization
  - 64 Meg x 18, and 32 Meg x 36 common I/O (CIO)
  - 16 banks
- 1.2V center-terminated push/pull I/O
- 2.5V<sub>V<sub>EXT</sub></sub>, 1.35V<sub>V<sub>DD</sub></sub>, 1.2V<sub>V<sub>DDQ</sub></sub> (optional 1.35V<sub>V<sub>DDQ</sub></sub> for 2400 operation only).
- Reduced cycle time (<sup>t</sup>RC (MIN) = 6.67 - 8ns)
- SDR addressing
- Programmable READ/WRITE latency (RL/WL) and burst length
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Free-running differential input data clocks (DK<sub>x</sub>, DK<sub>x</sub>#) and output data clocks (QK<sub>x</sub>, QK<sub>x</sub>#)
- On-die DLL generates CK edge-aligned data and differential output data clock signals
- 64ms refresh (128K refresh per 64ms)
- 168-ball BGA package
- 40Ω or 60Ω matched impedance outputs
- Integrated on-die termination (ODT)
- Single or multibank writes
- Extended operating range (200–1200 MHz)
- READ training register
- Multiplexed and non-multiplexed addressing capabilities
- Mirror function
- Output driver and ODT calibration
- JTAG interface (IEEE 1149.1-2001)

## Options<sup>1</sup>

- Clock cycle and <sup>t</sup>RC timing
  - 0.83ns and <sup>t</sup>RC (MIN) = 6.67ns (RL3-2400) -083F
  - 0.83ns and <sup>t</sup>RC (MIN) = 7.5ns (RL3-2400) -083E
  - 0.93ns and <sup>t</sup>RC (MIN) = 7.5ns (RL3-2133) -093F
  - 0.93ns and <sup>t</sup>RC (MIN) = 8ns (RL3-2133) -093E
  - 1.07ns and <sup>t</sup>RC (MIN) = 8ns (RL3-1866) -107E
- Configuration
  - 64 Meg x 18 64M18
  - 32 Meg x 36 32M36
- Operating temperature
  - Commercial (T<sub>C</sub> = 0° to +95°C) None
  - Industrial (T<sub>C</sub> = -40°C to +95°C) IT
- Package
  - 168-ball BGA (Pb-free) RB
- Revision :A

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on [www.micron.com](http://www.micron.com) for available offerings.

**Figure 1: 1Gb RLD RAM<sup>®</sup> 3 Part Numbers**



### BGA Part Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. Micron's BGA Part Marking Decoder is available on Micron's Web site at [www.micron.com](http://www.micron.com).



## Contents

General Description .....	9
General Notes .....	9
State Diagram .....	10
Functional Block Diagrams .....	11
Ball Assignments and Descriptions .....	13
Package Dimensions .....	17
Electrical Characteristics – I <sub>DD</sub> Specifications .....	18
Electrical Specifications – Absolute Ratings and I/O Capacitance .....	22
Absolute Maximum Ratings .....	22
Input/Output Capacitance .....	22
AC and DC Operating Conditions .....	23
AC Overshoot/Undershoot Specifications .....	25
Slew Rate Definitions for Single-Ended Input Signals .....	28
Slew Rate Definitions for Differential Input Signals .....	30
ODT Characteristics .....	31
ODT Resistors .....	31
ODT Sensitivity .....	33
Output Driver Impedance .....	33
Output Driver Sensitivity .....	34
Output Characteristics and Operating Conditions .....	36
Reference Output Load .....	39
Slew Rate Definitions for Single-Ended Output Signals .....	40
Slew Rate Definitions for Differential Output Signals .....	41
Speed Bin Tables .....	42
AC Electrical Characteristics .....	43
Temperature and Thermal Impedance Characteristics .....	49
Command and Address Setup, Hold, and Derating .....	51
Data Setup, Hold, and Derating .....	58
Commands .....	65
MODE REGISTER SET (MRS) Command .....	66
Mode Register 0 (MR0) .....	67
<sup>t</sup> RC .....	68
Data Latency .....	68
DLL Enable/Disable .....	68
Address Multiplexing .....	68
Mode Register 1 (MR1) .....	70
Output Drive Impedance .....	70
DQ On-Die Termination (ODT) .....	70
DLL Reset .....	70
ZQ Calibration .....	71
ZQ Calibration Long .....	72
ZQ Calibration Short .....	72
AUTO REFRESH Protocol .....	73
Burst Length (BL) .....	73
Mode Register 2 (MR2) .....	75
READ Training Register (RTR) .....	75
WRITE Protocol .....	78
Post Package Repair – PPR .....	78
PPR Row Repair Sequence .....	78
WRITE Command .....	80



Multibank WRITE .....	80
READ Command .....	81
AUTO REFRESH Command .....	83
INITIALIZATION Operation .....	85
WRITE Operation .....	87
READ Operation .....	91
AUTO REFRESH Operation .....	94
RESET Operation .....	97
Clock Stop .....	98
Mirror Function .....	99
Multiplexed Address Mode .....	100
Data Latency in Multiplexed Address Mode .....	105
REFRESH Command in Multiplexed Address Mode .....	105
IEEE 1149.1 Serial Boundary Scan (JTAG) .....	109
Disabling the JTAG Feature .....	109
Test Access Port (TAP) .....	109
TAP Controller .....	110
Performing a TAP RESET .....	112
TAP Registers .....	112
TAP Instruction Set .....	113

## List of Figures

Figure 1: 1Gb RLD RAM <sup>®</sup> 3 Part Numbers .....	2
Figure 2: Simplified State Diagram .....	10
Figure 3: 64 Meg x 18 Functional Block Diagram .....	11
Figure 4: 32 Meg x 36 Functional Block Diagram .....	12
Figure 5: 168-Ball BGA .....	17
Figure 6: Single-Ended Input Signal .....	24
Figure 7: Overshoot .....	25
Figure 8: Undershoot .....	25
Figure 9: $V_{IX}$ for Differential Signals .....	26
Figure 10: Single-Ended Requirements for Differential Signals .....	27
Figure 11: Definition of Differential AC Swing and <sup>t</sup> DVAC .....	27
Figure 12: Nominal Slew Rate Definition for Single-Ended Input Signals .....	29
Figure 13: Nominal Differential Input Slew Rate Definition for CK, CK#, DKx, and DKx# .....	30
Figure 14: ODT Levels and I-V Characteristics .....	31
Figure 15: Output Driver .....	34
Figure 16: DQ Output Signal .....	38
Figure 17: Differential Output Signal .....	39
Figure 18: Reference Output Load for AC Timing and Output Slew Rate .....	39
Figure 19: Nominal Slew Rate Definition for Single-Ended Output Signals .....	40
Figure 20: Nominal Differential Output Slew Rate Definition for QKx, QKx# .....	41
Figure 21: Example Temperature Test Point Location .....	50
Figure 22: Nominal Slew Rate and <sup>t</sup> VAC for <sup>t</sup> IS (Command and Address – Clock) .....	54
Figure 23: Nominal Slew Rate for <sup>t</sup> IH (Command and Address – Clock) .....	55
Figure 24: Tangent Line for <sup>t</sup> IS (Command and Address – Clock) .....	56
Figure 25: Tangent Line for <sup>t</sup> IH (Command and Address – Clock) .....	57
Figure 26: Nominal Slew Rate and <sup>t</sup> VAC for <sup>t</sup> DS (DQ – Strobe) .....	61
Figure 27: Nominal Slew Rate for <sup>t</sup> DH (DQ – Strobe) .....	62
Figure 28: Tangent Line for <sup>t</sup> DS (DQ – Strobe) .....	63
Figure 29: Tangent Line for <sup>t</sup> DH (DQ – Strobe) .....	64
Figure 30: MRS Command Protocol .....	66
Figure 31: MR0 Definition for Non-Multiplexed Address Mode .....	67
Figure 32: MR1 Definition for Non-Multiplexed Address Mode .....	70
Figure 33: ZQ Calibration Timing (ZQCL and ZQCS) .....	72
Figure 34: Read Burst Lengths .....	74
Figure 35: MR2 Definition for Non-Multiplexed Address Mode .....	75
Figure 36: READ Training Function - Back-to-Back Readout .....	77
Figure 37: Entry, Repair, and Exit Timing Diagram .....	79
Figure 38: WRITE Command .....	80
Figure 39: READ Command .....	82
Figure 40: Bank Address-Controlled AUTO REFRESH Command .....	83
Figure 41: Multibank AUTO REFRESH Command .....	84
Figure 42: Power-Up/Initialization Sequence .....	86
Figure 43: WRITE Burst .....	87
Figure 44: Consecutive WRITE Bursts .....	88
Figure 45: WRITE-to-READ .....	88
Figure 46: WRITE - DM Operation .....	89
Figure 47: Consecutive Quad Bank WRITE Bursts .....	89
Figure 48: Interleaved READ and Quad Bank WRITE Bursts .....	90
Figure 49: Basic READ Burst .....	91
Figure 50: Consecutive READ Bursts (BL = 2) .....	92

Figure 51: Consecutive READ Bursts (BL = 4) .....	92
Figure 52: READ-to-WRITE (BL = 2) .....	93
Figure 53: Read Data Valid Window .....	93
Figure 54: Bank Address-Controlled AUTO REFRESH Cycle .....	94
Figure 55: Multibank AUTO REFRESH Cycle .....	94
Figure 56: READ Burst with ODT .....	95
Figure 57: READ-NOP-READ with ODT .....	96
Figure 58: RESET Sequence .....	97
Figure 59: Command Description in Multiplexed Address Mode .....	100
Figure 60: Power-Up/Initialization Sequence in Multiplexed Address Mode .....	101
Figure 61: MR0 Definition for Multiplexed Address Mode .....	102
Figure 62: MR1 Definition for Multiplexed Address Mode .....	103
Figure 63: MR2 Definition for Multiplexed Address Mode .....	104
Figure 64: Bank Address-Controlled AUTO REFRESH Operation with Multiplexed Addressing .....	105
Figure 65: Multibank AUTO REFRESH Operation with Multiplexed Addressing .....	106
Figure 66: Consecutive WRITE Bursts with Multiplexed Addressing .....	106
Figure 67: WRITE-to-READ with Multiplexed Addressing .....	107
Figure 68: Consecutive READ Bursts with Multiplexed Addressing .....	107
Figure 69: READ-to-WRITE with Multiplexed Addressing .....	108
Figure 70: TAP Controller State Diagram .....	111
Figure 71: TAP Controller Functional Block Diagram .....	111
Figure 72: JTAG Operation – Loading Instruction Code and Shifting Out Data .....	115
Figure 73: TAP Timing .....	116

## List of Tables

Table 1: 64 Meg x 18 Ball Assignments – 168-Ball BGA (Top View) .....	13
Table 2: 32 Meg x 36 Ball Assignments – 168-Ball BGA (Top View) .....	14
Table 3: Ball Descriptions .....	15
Table 4: I <sub>DD</sub> Operating Conditions and Maximum Limits .....	18
Table 5: Absolute Maximum Ratings .....	22
Table 6: Input/Output Capacitance .....	22
Table 7: DC Electrical Characteristics and Operating Conditions .....	23
Table 8: Input AC Logic Levels .....	23
Table 9: Control and Address Balls .....	25
Table 10: Clock, Data, Strobe, and Mask Balls .....	25
Table 11: Differential Input Operating Conditions (CK, CK# and DKx, DKx#) .....	26
Table 12: Allowed Time Before Ringback ( <sup>t</sup> DVAC) for CK, CK#, DKx, and DKx# .....	28
Table 13: Single-Ended Input Slew Rate Definition .....	28
Table 14: Differential Input Slew Rate Definition .....	30
Table 15: ODT DC Electrical Characteristics .....	31
Table 16: R <sub>TT</sub> Effective Impedances .....	32
Table 17: ODT Sensitivity Definition .....	33
Table 18: ODT Temperature and Voltage Sensitivity .....	33
Table 19: Driver Pull-Up and Pull-Down Impedance Calculations .....	34
Table 20: Output Driver Sensitivity Definition .....	35
Table 21: Output Driver Voltage and Temperature Sensitivity .....	35
Table 22: Single-Ended Output Driver Characteristics .....	36
Table 23: Differential Output Driver Characteristics .....	37
Table 24: Single-Ended Output Slew Rate Definition .....	40
Table 25: Differential Output Slew Rate Definition .....	41
Table 26: RL3 2400/2133/1866 Speed Bins .....	42
Table 27: AC Electrical Characteristics .....	43
Table 28: Temperature Limits .....	49
Table 29: Thermal Impedance .....	50
Table 30: Command and Address Setup and Hold Values Referenced at 1 V/ns – AC/DC-Based .....	51
Table 31: Derating Values for <sup>t</sup> IS/ <sup>t</sup> IH – AC150/DC100-Based .....	52
Table 32: Derating Values for <sup>t</sup> IS/ <sup>t</sup> IH – AC135/DC100-Based .....	52
Table 33: Derating Values for <sup>t</sup> IS/ <sup>t</sup> IH – AC120/DC100-Based .....	53
Table 34: Minimum Required Time <sup>t</sup> VAC Above V <sub>IH(AC)</sub> (or Below V <sub>IL(AC)</sub> ) for Valid Transition .....	53
Table 35: Data Setup and Hold Values (DKx, DKx# at 2 V/ns) – AC/DC-Based .....	58
Table 36: Derating Values for <sup>t</sup> DS/ <sup>t</sup> DH – AC150/DC100-Based .....	59
Table 37: Derating Values for <sup>t</sup> DS/ <sup>t</sup> DH – AC135/DC100-Based .....	59
Table 38: Derating Values for <sup>t</sup> DS/ <sup>t</sup> DH – AC120/DC100-Based .....	60
Table 39: Minimum Required Time <sup>t</sup> VAC Above V <sub>IH(AC)</sub> (or Below V <sub>IL(AC)</sub> ) for Valid Transition .....	60
Table 40: Command Descriptions .....	65
Table 41: Command Table .....	65
Table 42: <sup>t</sup> RC_MRS MR0[3:0] Values .....	68
Table 43: Address Widths of Different Burst Lengths .....	73
Table 44: RLD RAM3 PPR Timing Parameters .....	79
Table 45: 64 Meg x 18 Ball Assignments with MF Ball Tied HIGH .....	99
Table 46: Address Mapping in Multiplexed Address Mode .....	104
Table 47: TAP Input AC Logic Levels .....	116
Table 48: TAP AC Electrical Characteristics .....	116
Table 49: TAP DC Electrical Characteristics and Operating Conditions .....	117
Table 50: Scan Register Sizes .....	117





Table 51: Instruction Codes .....	118
Table 52: Identification (ID) Code Definition .....	118
Table 53: MR0_MR1 Mode Register Settings Definition .....	118
Table 54: MR2 Mode Register Settings Definition .....	119
Table 55: Boundary Scan (Exit) .....	120

## General Description

The Micron® RLD RAM® 3 is a high-speed memory device designed for high-bandwidth data storage—telecommunications, networking, cache applications, and so forth. The chip's 16-bank architecture is optimized for sustainable high-speed operation.

The DDR I/O interface transfers two data bits per clock cycle at the I/O balls. Output data is referenced to the READ strobes.

Commands, addresses, and control signals are also registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data strobes.

Read and write accesses to the RL3 device are burst-oriented. The burst length (BL) is programmable to 2, 4, or 8 by a setting in the mode register.

The device is supplied with 1.35V for the core and 1.2V for the output drivers. The 2.5V supply is used for an internal supply.

Bank-scheduled refresh is supported with the row address generated internally.

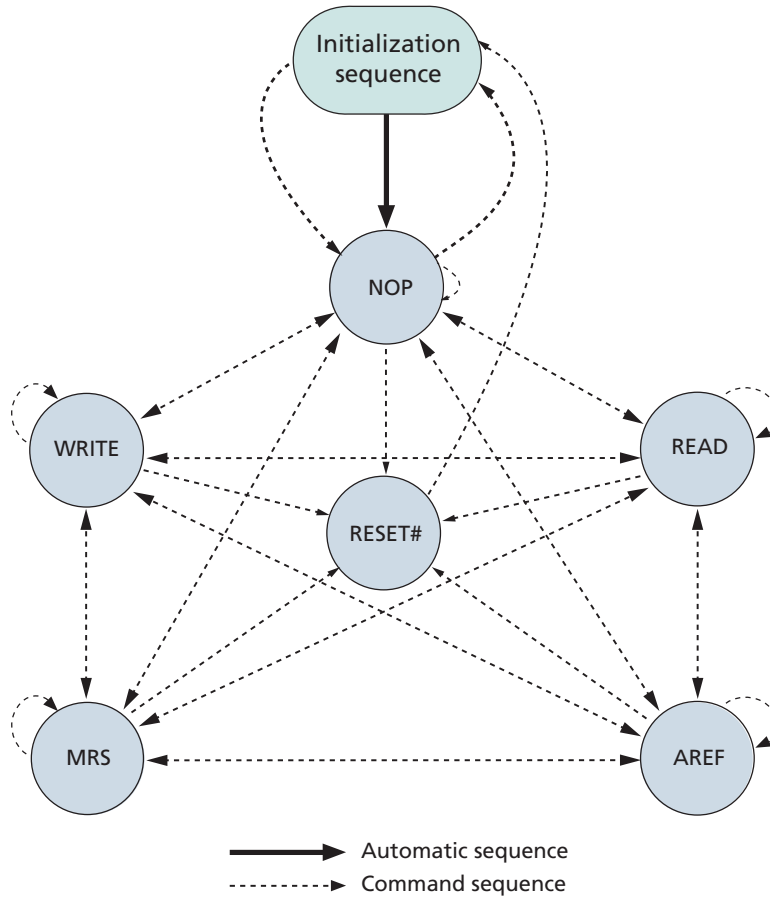
The 168-ball BGA package is used to enable ultra-high-speed data transfer rates.

## General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Nominal conditions are assumed for specifications not defined within the figures shown in this data sheet.
- Throughout this data sheet, the terms "RLDRAM," "DRAM," and "RLDRAM 3" are all used interchangeably and refer to the RLD RAM 3 SDRAM device.
- References to DQ, DK, QK, DM, and QVLD are to be interpreted as each group collectively, unless specifically stated otherwise. This includes true and complement signals of differential signals.
- Non-multiplexed operation is assumed if not specified as multiplexed.
- A x36 device supplies four QK/QK# sets, one per nine DQ. Using only two QK/QK# sets is allowed, but QK0/QK0# and QK1/QK1# must be used. QK0/QK0# control DQ[8:0] and DQ[26:18], and QK1/QK1# control DQ[17:9] and DQ[35:27]. The QK to DQ timing parameter to be used is <sup>t</sup>QKQ02, <sup>t</sup>QKQ13. The unused QK/QK# pins should be left floating.

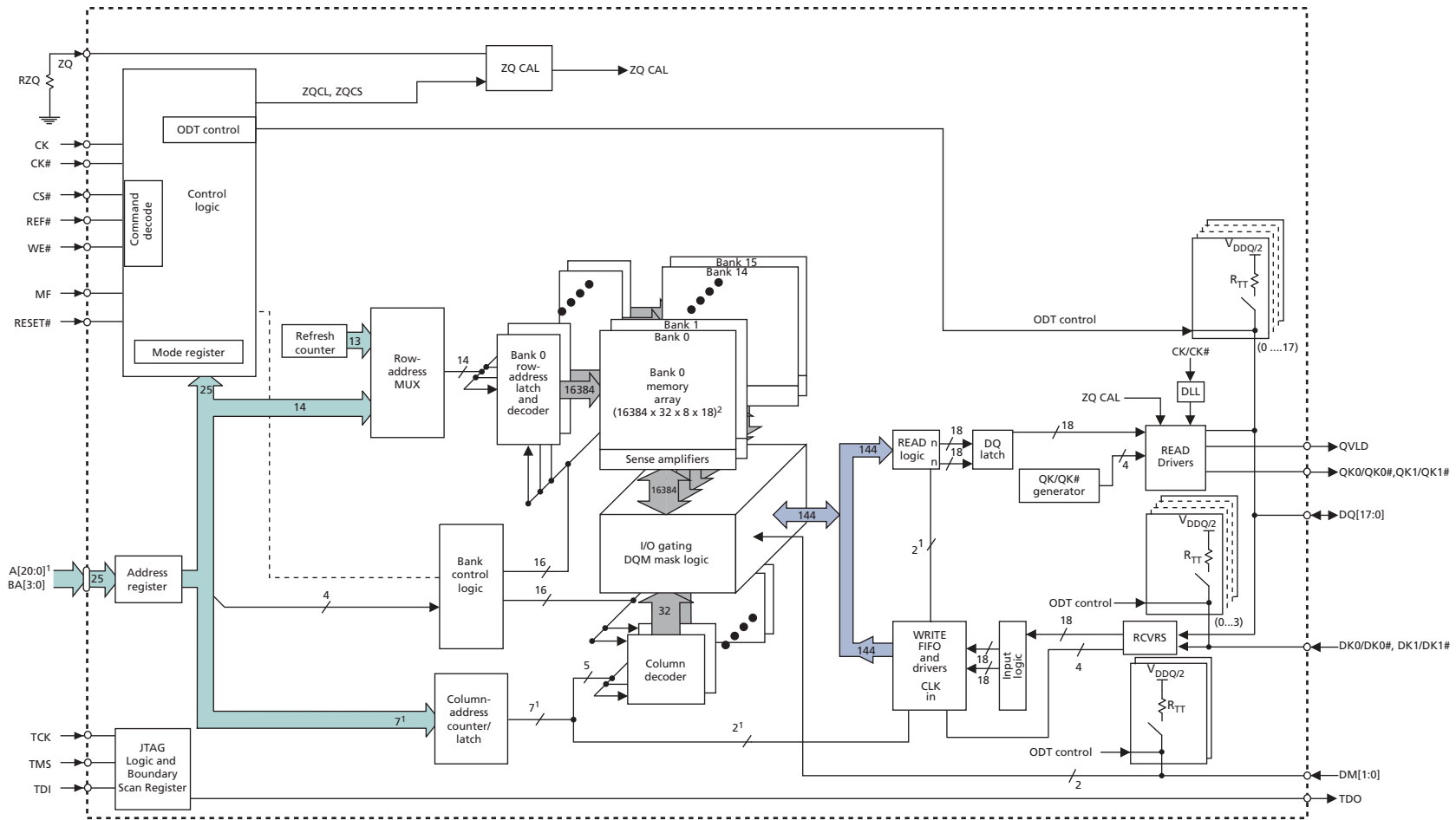
## State Diagram

Figure 2: Simplified State Diagram



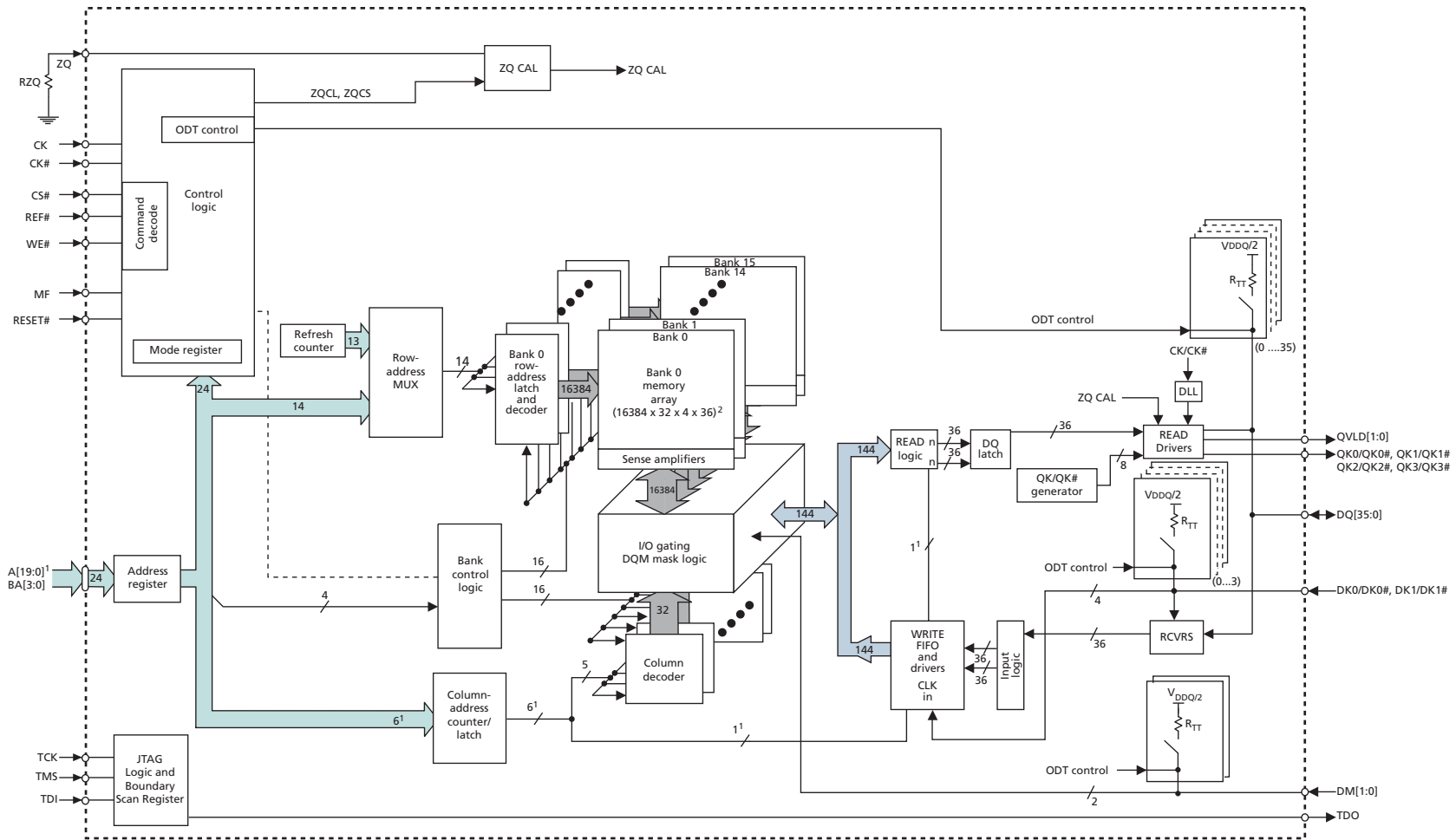
# Functional Block Diagrams

**Figure 3: 64 Meg x 18 Functional Block Diagram**



- Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
  2.  $8 = (\text{length of burst}) \times 2^{\wedge} (\text{number of column addresses to WRITE FIFO and READ logic})$ .

# Functional Block Diagrams

**Figure 4: 32 Meg x 36 Functional Block Diagram**


- Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
  2.  $4 = (\text{length of burst}) \times 2^{\wedge} (\text{number of column addresses to WRITE FIFO and READ logic})$ .



## Ball Assignments and Descriptions

**Table 1: 64 Meg x 18 Ball Assignments – 168-Ball BGA (Top View)**

	1	2	3	4	5	6	7	8	9	10	11	12	13
<b>A</b>		V <sub>SS</sub>	V <sub>DD</sub>	NF	V <sub>DDQ</sub>	NF	V <sub>REF</sub>	DQ7	V <sub>DDQ</sub>	DQ8	V <sub>DD</sub>	V <sub>SS</sub>	RESET#
<b>B</b>	V <sub>EXT</sub>	V <sub>SS</sub>	NF	V <sub>SSQ</sub>	NF	V <sub>DDQ</sub>	DM0	V <sub>DDQ</sub>	DQ5	V <sub>SSQ</sub>	DQ6	V <sub>SS</sub>	V <sub>EXT</sub>
<b>C</b>	V <sub>DD</sub>	NF	V <sub>DDQ</sub>	NF	V <sub>SSQ</sub>	NF	DK0#	DQ2	V <sub>SSQ</sub>	DQ3	V <sub>DDQ</sub>	DQ4	V <sub>DD</sub>
<b>D</b>	A11	V <sub>SSQ</sub>	NF	V <sub>DDQ</sub>	NF	V <sub>SSQ</sub>	DK0	V <sub>SSQ</sub>	QK0	V <sub>DDQ</sub>	DQ0	V <sub>SSQ</sub>	A13
<b>E</b>	V <sub>SS</sub>	A0	V <sub>SSQ</sub>	NF	V <sub>DDQ</sub>	NF	MF	QK0#	V <sub>DDQ</sub>	DQ1	V <sub>SSQ</sub>	CS#	V <sub>SS</sub>
<b>F</b>	A7	A20	V <sub>DD</sub>	A2	A1	WE#	ZQ	REF#	A3	A4	V <sub>DD</sub>	A5	A9
<b>G</b>	V <sub>SS(RFU)</sub> <sup>1</sup>	A15	A6	V <sub>SS</sub>	BA1	V <sub>SS</sub>	CK#	V <sub>SS</sub>	BA0	V <sub>SS</sub>	A8	A18	V <sub>SS(CS1#)</sub> <sup>2</sup>
<b>H</b>	A19	V <sub>DD</sub>	A14	A16	V <sub>DD</sub>	BA3	CK	BA2	V <sub>DD</sub>	A17	A12	V <sub>DD</sub>	A10
<b>J</b>	V <sub>DDQ</sub>	NF	V <sub>SSQ</sub>	NF	V <sub>DDQ</sub>	NF	V <sub>SS</sub>	QK1#	V <sub>DDQ</sub>	DQ9	V <sub>SSQ</sub>	QVLD	V <sub>DDQ</sub>
<b>K</b>	NF	V <sub>SSQ</sub>	NF	V <sub>DDQ</sub>	NF	V <sub>SSQ</sub>	DK1	V <sub>SSQ</sub>	QK1	V <sub>DDQ</sub>	DQ10	V <sub>SSQ</sub>	DQ11
<b>L</b>	V <sub>DD</sub>	NF	V <sub>DDQ</sub>	NF	V <sub>SSQ</sub>	NF	DK1#	DQ12	V <sub>SSQ</sub>	DQ13	V <sub>DDQ</sub>	DQ14	V <sub>DD</sub>
<b>M</b>	V <sub>EXT</sub>	V <sub>SS</sub>	NF	V <sub>SSQ</sub>	NF	V <sub>DDQ</sub>	DM1	V <sub>DDQ</sub>	DQ15	V <sub>SSQ</sub>	DQ16	V <sub>SS</sub>	V <sub>EXT</sub>
<b>N</b>	V <sub>SS</sub>	TCK	V <sub>DD</sub>	TDO	V <sub>DDQ</sub>	NF	V <sub>REF</sub>	DQ17	V <sub>DDQ</sub>	TDI	V <sub>DD</sub>	TMS	V <sub>SS</sub>

- Notes:
1. Reserved for future use (RFU) is being identified as the location to handle possible future density increases and is the mirror function location of the 2Gb X18 DDP (CS1#) pin. Has parasitic characteristics of an address pin.
  2. Location of the additional signal (CS1#) required for the 2Gb x18 DDP configuration. Has parasitic characteristics of an address pin.
  3. NF balls for the x18 configuration are internally connected and have parasitic characteristics of an I/O. Balls may be connected to V<sub>SSQ</sub>.
  4. MF is assumed to be tied LOW for this ball assignment.

**Table 2: 32 Meg x 36 Ball Assignments – 168-Ball BGA (Top View)**

	1	2	3	4	5	6	7	8	9	10	11	12	13
<b>A</b>		V <sub>SS</sub>	V <sub>DD</sub>	DQ26	V <sub>DDQ</sub>	DQ25	V <sub>REF</sub>	DQ7	V <sub>DDQ</sub>	DQ8	V <sub>DD</sub>	V <sub>SS</sub>	RESET#
<b>B</b>	V <sub>EXT</sub>	V <sub>SS</sub>	DQ24	V <sub>SSQ</sub>	DQ23	V <sub>DDQ</sub>	DM0	V <sub>DDQ</sub>	DQ5	V <sub>SSQ</sub>	DQ6	V <sub>SS</sub>	V <sub>EXT</sub>
<b>C</b>	V <sub>DD</sub>	DQ22	V <sub>DDQ</sub>	DQ21	V <sub>SSQ</sub>	DQ20	DK0#	DQ2	V <sub>SSQ</sub>	DQ3	V <sub>DDQ</sub>	DQ4	V <sub>DD</sub>
<b>D</b>	A11	V <sub>SSQ</sub>	DQ18	V <sub>DDQ</sub>	QK2	V <sub>SSQ</sub>	DK0	V <sub>SSQ</sub>	QK0	V <sub>DDQ</sub>	DQ0	V <sub>SSQ</sub>	A13
<b>E</b>	V <sub>SS</sub>	A0	V <sub>SSQ</sub>	DQ19	V <sub>DDQ</sub>	QK2#	MF	QK0#	V <sub>DDQ</sub>	DQ1	V <sub>SSQ</sub>	CS#	V <sub>SS</sub>
<b>F</b>	A7	NF (A20) <sup>1</sup>	V <sub>DD</sub>	A2	A1	WE#	ZQ	REF#	A3	A4	V <sub>DD</sub>	A5	A9
<b>G</b>	V <sub>SS</sub>	A15	A6	V <sub>SS</sub>	BA1	V <sub>SS</sub>	CK#	V <sub>SS</sub>	BA0	V <sub>SS</sub>	A8	A18	V <sub>SS</sub>
<b>H</b>	A19	V <sub>DD</sub>	A14	A16	V <sub>DD</sub>	BA3	CK	BA2	V <sub>DD</sub>	A17	A12	V <sub>DD</sub>	A10
<b>J</b>	V <sub>DDQ</sub>	QVLD1	V <sub>SSQ</sub>	DQ27	V <sub>DDQ</sub>	QK3#	V <sub>SS</sub>	QK1#	V <sub>DDQ</sub>	DQ9	V <sub>SSQ</sub>	QVLD0	V <sub>DDQ</sub>
<b>K</b>	DQ29	V <sub>SSQ</sub>	DQ28	V <sub>DDQ</sub>	QK3	V <sub>SSQ</sub>	DK1	V <sub>SSQ</sub>	QK1	V <sub>DDQ</sub>	DQ10	V <sub>SSQ</sub>	DQ11
<b>L</b>	V <sub>DD</sub>	DQ32	V <sub>DDQ</sub>	DQ31	V <sub>SSQ</sub>	DQ30	DK1#	DQ12	V <sub>SSQ</sub>	DQ13	V <sub>DDQ</sub>	DQ14	V <sub>DD</sub>
<b>M</b>	V <sub>EXT</sub>	V <sub>SS</sub>	DQ34	V <sub>SSQ</sub>	DQ33	V <sub>DDQ</sub>	DM1	V <sub>DDQ</sub>	DQ15	V <sub>SSQ</sub>	DQ16	V <sub>SS</sub>	V <sub>EXT</sub>
<b>N</b>	V <sub>SS</sub>	TCK	V <sub>DD</sub>	TDO	V <sub>DDQ</sub>	DQ35	V <sub>REF</sub>	DQ17	V <sub>DDQ</sub>	TDI	V <sub>DD</sub>	TMS	V <sub>SS</sub>

- Notes:
1. This ball is NF for SDP 1Gb x36 configuration but becomes A20 for DDP 2Gb x 36 configuration. Has parasitic characteristics of an address pin.
  2. NF ball for x36 configuration is internally connected and has parasitic characteristics of an address. Ball may be connected to V<sub>SSQ</sub>.
  3. MF is assumed to be tied LOW for this ball assignment.

**Table 3: Ball Descriptions**

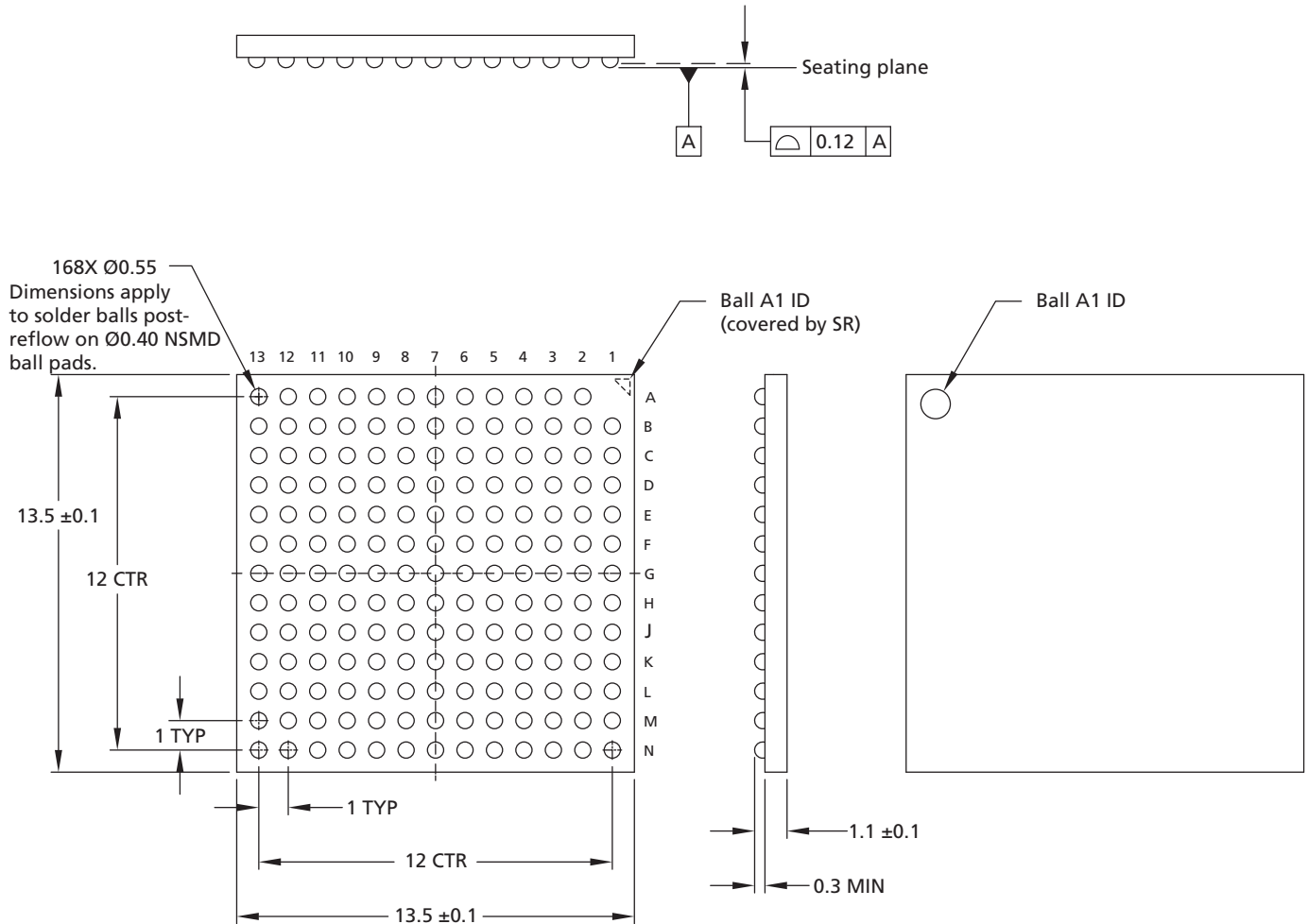
Symbol	Type	Description
A[20:0]	Input	<b>Address inputs:</b> A[20:0] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings along with BA[3:0]. They are sampled at the rising edge of CK.
BA[3:0]	Input	<b>Bank address inputs:</b> Select the internal bank to which a command is being applied.
CK/CK#	Input	<b>Input clock:</b> CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK.
CS#	Input	<b>Chip select:</b> CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
DQ[35:0]	I/O	<b>Data input:</b> The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK. During WRITE commands, the data is sampled at both edges of DK.
DKx, DKx#	Input	<b>Input data clock:</b> DKx and DKx# are differential input data clocks. All input data is referenced to both edges of DKx. For the x36 device, DQ[8:0] and DQ[26:18] are referenced to DK0 and DK0#, and DQ[17:9] and DQ[35:27] are referenced to DK1 and DK1#. For the x18 device, DQ[8:0] are referenced to DK0 and DK0#, and DQ[17:9] are referenced to DK1 and DK1#. DKx and DKx# are free-running signals and must always be supplied to the device.
DM[1:0]	Input	<b>Input data mask:</b> DM is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM0 is used to mask the lower byte for the x18 device and DQ[8:0] and DQ[26:18] for the x36 device. DM1 is used to mask the upper byte for the x18 device and DQ[17:9] and DQ[35:27] for the x36 device. Tie DM[1:0] to V <sub>SS</sub> if not used.
TCK	Input	<b>IEEE 1149.1 clock input:</b> This ball must be tied to V <sub>SS</sub> if the JTAG function is not used.
TMS, TDI	Input	<b>IEEE 1149.1 test inputs:</b> These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	<b>Command inputs:</b> Sampled at the positive edge of CK, WE#, and REF# (together with CS#) define the command to be executed.
RESET#	Input	<b>Reset:</b> RESET# is an active LOW CMOS input referenced to V <sub>SS</sub> . RESET# assertion and deassertion are asynchronous. RESET# is a CMOS input defined with DC HIGH ≥ 0.8 x V <sub>DDQ</sub> and DC LOW ≤ 0.2 x V <sub>DDQ</sub> .
ZQ	Input	<b>External impedance:</b> This signal is used to tune the device's output impedance and ODT. RZQ needs to be 240Ω, where RZQ is a resistor from this signal to ground.
QKx, QKx#	Output	<b>Output data clocks:</b> QK and QK# are opposite-polarity output data clocks. They are free-running signals and during READ commands are edge-aligned with the DQs. For the x36 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9]; QK2, QK2# align with DQ[26:18]; QK3, QK3# align with DQ[35:27]. For the x18 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9].
QVLDx	Output	<b>Data valid:</b> The QVLD ball indicates that valid output data will be available on the subsequent rising clock edge. There is a single QVLD ball for the x18 device and two, QVLD0 and QVLD1, for the x36 device. QVLD0 aligns with DQ[17:0]; QVLD1 aligns with DQ[35:18].
MF	Input	<b>Mirror function:</b> The mirror function ball is a DC input used to create mirrored ballouts for simple dual-loaded clamshell mounting. If the ball is tied to V <sub>SS</sub> , the address and command balls are in their true layout. If the ball is tied to V <sub>DDQ</sub> , they are in the complement location. MF must be tied HIGH or LOW and cannot be left floating.
TDO	Output	<b>IEEE 1149.1 test output:</b> JTAG output. This ball may be left as no connect if the JTAG function is not used.

**Table 3: Ball Descriptions (Continued)**

Symbol	Type	Description
V <sub>DD</sub>	Supply	<b>Power supply:</b> 1.35V nominal. See AC and DC Operating Conditions (page 23) for range.
V <sub>DDQ</sub>	Supply	<b>DQ power supply:</b> 1.2V or 1.35V nominal. 1.2V can be used for all speed grades. The 1.35V can only be used for 2400 Mb/s operation if required tp close timing. Isolated on the device for improved noise immunity. See AC and DC Operating Conditions (page 23) for range.
V <sub>EXT</sub>	Supply	<b>Power supply:</b> 2.5V nominal. See AC and DC Operating Conditions (page 23) for range.
V <sub>REF</sub>	Supply	<b>Input reference voltage:</b> V <sub>DDQ</sub> /2 nominal. Provides a reference voltage for the input buffers.
V <sub>SS</sub>	Supply	Ground.
V <sub>SSQ</sub>	Supply	<b>DQ ground:</b> Isolated on the device for improved noise immunity.
NC	–	<b>No connect:</b> These balls are not connected to the DRAM.
NF	–	<b>No function:</b> These balls are connected to the DRAM but provide no functionality.

## Package Dimensions

Figure 5: 168-Ball BGA



- Notes: 1. All dimensions are in millimeters.  
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).



## Electrical Characteristics – I<sub>DD</sub> Specifications

**Table 4: I<sub>DD</sub> Operating Conditions and Maximum Limits**

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-083F	-083E	-093F	-093E	-107E	Units
Standby current	<sup>t</sup> CK = idle; All banks idle; No inputs toggling	I <sub>SB1</sub> (V <sub>DD</sub> ) x18	225	225	225	225	225	mA
		I <sub>SB1</sub> (V <sub>DD</sub> ) x36	225	225	225	225	225	
		I <sub>SB1</sub> (V <sub>EXT</sub> )	55	55	55	55	55	
Clock active stand-by current	CS# = 1; No commands; Bank address incremented and half address/data change once every four clock cycles	I <sub>SB2</sub> (V <sub>DD</sub> ) x18	655	655	605	605	570	mA
		I <sub>SB2</sub> (V <sub>DD</sub> ) x36	675	675	625	625	585	
		I <sub>SB2</sub> (V <sub>EXT</sub> )	55	55	55	55	55	
Operational current: BL2	BL = 2; Sequential bank access; Bank transitions once every <sup>t</sup> RC; Half address transitions once every <sup>t</sup> RC; Read followed by write sequence; Continuous data during WRITE commands	I <sub>DD1</sub> (V <sub>DD</sub> ) x18	1220	1150	1105	1040	975	mA
		I <sub>DD1</sub> (V <sub>DD</sub> ) x36	1230	1160	1115	1050	985	
		I <sub>DD1</sub> (V <sub>EXT</sub> )	60	60	60	60	60	
Operational current: BL4	BL = 4; Sequential bank access; Bank transitions once every <sup>t</sup> RC; Half address transitions once every <sup>t</sup> RC; Read followed by write sequence; Continuous data during WRITE commands	I <sub>DD2</sub> (V <sub>DD</sub> ) x18	1330	1260	1200	1130	1060	mA
		I <sub>DD2</sub> (V <sub>DD</sub> ) x36	1340	1270	1210	1140	1070	
		I <sub>DD2</sub> (V <sub>EXT</sub> )	60	60	60	60	60	
Operational current: BL8	BL = 8; Sequential bank access; Bank transitions once every <sup>t</sup> RC; Half address transitions once every <sup>t</sup> RC; Read followed by write sequence; Continuous data during WRITE commands	I <sub>DD3</sub> (V <sub>DD</sub> ) x18	1260	1190	1160	1095	1015	mA
		I <sub>DD3</sub> (V <sub>DD</sub> ) x36	NA	NA	NA	NA	NA	
		I <sub>DD3</sub> (V <sub>EXT</sub> )	65	65	60	60	60	
Burst refresh current	Sixteen bank cyclic refresh using Bank Address Control AREF protocol; Command bus remains in refresh for all sixteen banks; DQs are High-Z and at V <sub>DDQ</sub> /2; Addresses are at V <sub>DDQ</sub> /2	I <sub>REF1</sub> (V <sub>DD</sub> ) x18	1255	1255	1135	1135	1025	mA
		I <sub>REF1</sub> (V <sub>DD</sub> ) x36	1270	1270	1150	1150	1040	
		I <sub>REF1</sub> (V <sub>EXT</sub> )	125	125	115	115	110	
Distributed refresh current	Single bank refresh using Bank Address Control AREF protocol; Sequential bank access every 0.489μs; DQs are High-Z and at V <sub>DDQ</sub> /2; Addresses are at V <sub>DDQ</sub> /2	I <sub>REF2</sub> (V <sub>DD</sub> ) x18	660	660	610	610	575	mA
		I <sub>REF2</sub> (V <sub>DD</sub> ) x36	680	680	630	630	590	
		I <sub>REF2</sub> (V <sub>EXT</sub> )	55	55	55	55	55	

**Table 4: I<sub>DD</sub> Operating Conditions and Maximum Limits (Continued)**

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-083F	-083E	-093F	-093E	-107E	Units
Multibank refresh current: 4 bank refresh	Quad bank refresh using Multibank AREF protocol; BL = 4; Cyclic bank access; Subject to <sup>t</sup> SAW and <sup>t</sup> MMD specifications; DQs are High-Z and at V <sub>DDQ</sub> /2; Bank addresses are at V <sub>DDQ</sub> /2	I <sub>MBREF4</sub> (V <sub>DD</sub> ) x18	1570	1570	1490	1490	1420	mA
		I <sub>MBREF4</sub> (V <sub>DD</sub> ) x36	1590	1590	1510	1510	1435	
		I <sub>MBREF4</sub> (V <sub>EXT</sub> )	205	205	185	185	165	
Operating burst write current : BL2	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous WRITE	I <sub>DD2W</sub> (V <sub>DD</sub> ) x18	1845	1845	1655	1655	1500	mA
		I <sub>DD2W</sub> (V <sub>DD</sub> ) x36	2000	2000	1810	1810	1635	
		I <sub>DD2W</sub> (V <sub>EXT</sub> )	85	85	80	80	75	
Operating burst write current : BL4	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE	I <sub>DD4W</sub> (V <sub>DD</sub> ) x18	1680	1680	1515	1515	1395	mA
		I <sub>DD4W</sub> (V <sub>DD</sub> ) x36	1760	1760	1595	1595	1465	
		I <sub>DD4W</sub> (V <sub>EXT</sub> )	80	80	75	75	70	
Operating burst write current :BL8	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous WRITE	I <sub>DD8W</sub> (V <sub>DD</sub> ) x18	1240	1240	1140	1140	1040	mA
		I <sub>DD8W</sub> (V <sub>DD</sub> ) x36	NA	NA	NA	NA	NA	
		I <sub>DD8W</sub> (V <sub>EXT</sub> )	70	70	70	70	65	
Multibank write current: Dual bank write	BL = 4; Cyclic bank access using Dual Bank WRITE; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE	I <sub>DBWR</sub> (V <sub>DD</sub> ) x18	2215	2215	2005	2005	1890	mA
		I <sub>DBWR</sub> (V <sub>DD</sub> ) x36	2300	2300	2090	2090	1960	
		I <sub>DBWR</sub> (V <sub>EXT</sub> )	125	125	115	115	110	
Multibank write current: Quad bank write	BL = 4; Cyclic bank access using Quad Bank WRITE; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE; Subject to <sup>t</sup> SAW specification	I <sub>QBWR</sub> (V <sub>DD</sub> ) x18	2930	2930	2620	2620	2565	mA
		I <sub>QBWR</sub> (V <sub>DD</sub> ) x36	3150	3150	2840	2840	2665	
		I <sub>QBWR</sub> (V <sub>EXT</sub> )	230	230	200	200	175	
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous READ	I <sub>DD2R</sub> (V <sub>DD</sub> ) x18	1900	1900	1715	1715	1560	mA
		I <sub>DD2R</sub> (V <sub>DD</sub> ) x36	2020	2020	1835	1835	1670	
		I <sub>DD2R</sub> (V <sub>EXT</sub> )	85	85	80	80	75	
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous READ	I <sub>DD4R</sub> (V <sub>DD</sub> ) x18	1675	1675	1510	1510	1380	mA
		I <sub>DD4R</sub> (V <sub>DD</sub> ) x36	1760	1760	1595	1595	1465	
		I <sub>DD4R</sub> (V <sub>EXT</sub> )	80	80	75	75	70	

**Table 4: I<sub>DD</sub> Operating Conditions and Maximum Limits (Continued)**

Notes 1–6 apply to the entire table

Description	Condition	Symbol	-083F	-083E	-093F	-093E	-107E	Units
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous READ	I <sub>DD8R</sub> (V <sub>DD</sub> ) x18	1240	1240	1135	1135	1040	mA
		I <sub>DD8R</sub> (V <sub>DD</sub> ) x36	NA	NA	NA	NA	NA	
		I <sub>DD8R</sub> (V <sub>EXT</sub> )	70	70	70	70	65	

- Notes:
1. I<sub>DD</sub> specifications are tested after the device is properly initialized.  $0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.28\text{V} \leq V_{DD} \leq +1.42\text{V}$ ,  $+1.14\text{V} \leq V_{DDQ} \leq +1.26\text{V}$ ,  $+2.38\text{V} \leq V_{EXT} \leq +2.63\text{V}$ ,  $V_{REF} = V_{DDQ}/2$ .
  2. I<sub>DD</sub> measurements use  $t_{CK}$  (MIN),  $t_{RC}$  (MIN), and minimum data latency (RL and WL).
  3. Input slew rate is 1 V/ns for single ended signals and 2 V/ns for differential signals.
  4. Definitions for I<sub>DD</sub> conditions:
    - LOW is defined as  $V_{IN} \leq V_{IL(AC)MAX}$ .
    - HIGH is defined as  $V_{IN} \geq V_{IH(AC)MIN}$ .
    - Continuous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
    - Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
    - Sequential bank access is defined as the bank address incrementing by one every  $t_{RC}$ .
    - Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
  5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
  6. I<sub>DD</sub> parameters are specified with ODT disabled.

## Electrical Specifications – Absolute Ratings and I/O Capacitance

### Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 5: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Units
$V_{DD}$	$V_{DD}$ supply voltage relative to $V_{SS}$	-0.4	1.975	V
$V_{DDQ}$	Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	-0.4	1.66	V
$V_{IN}, V_{OUT}$	Voltage on any ball relative to $V_{SS}$	-0.4	1.66	V
$V_{EXT}$	Voltage on $V_{EXT}$ supply relative to $V_{SS}$	-0.4	2.8	V

### Input/Output Capacitance

**Table 6: Input/Output Capacitance**

Notes 1 and 2 apply to entire table

Capacitance Parameters	Symbol	RL3-2400		RL3-2133		RL3-1866		Units	Notes
		Min	Max	Min	Max	Min	Max		
CK/CK#	$C_{CK}$	1.3	2.1	1.3	2.1	1.3	2.1	pF	
$\Delta C$ : CK to CK#	$C_{DCK}$	0	0.15	0	0.15	0	0.15	pF	
Single-ended I/O: DQ, DM	$C_{IO}$	1.9	2.9	1.9	3.0	1.9	3.1	pF	3
Input strobe: DK/DK#	$C_{IO}$	1.9	2.9	1.9	3.0	1.9	3.1	pF	
Output strobe: QK/QK#, QVLD	$C_{IO}$	1.9	2.9	1.9	3.0	1.9	3.1	pF	
$\Delta C$ : DK to DK#	$C_{DDK}$	0	0.15	0	0.15	0	0.15	pF	
$\Delta C$ : QK to QK#	$C_{DQK}$	0	0.15	0	0.15	0	0.15	pF	
$\Delta C$ : DQ to QK or DQ to DK	$C_{DIO}$	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	4
Inputs (CMD, ADDR)	$C_I$	1.25	2.25	1.25	2.25	1.25	2.25	pF	5
$\Delta C$ : CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	-0.5	0.3	-0.5	0.3	-0.4	0.4	pF	6
JTAG balls	$C_{JTAG}$	1.5	4.5	1.5	4.5	1.5	4.5	pF	7
RESET#, MF balls	$C_I$	-	3.0	-	3.0	-	3.0	pF	

- Notes:
- $+1.28V \leq V_{DD} \leq +1.42V$ ,  $+1.14V \leq V_{DDQ} \leq 1.26V$ ,  $+2.38V \leq V_{EXT} \leq +2.63V$ ,  $V_{REF} = V_{SS}$ ,  $f = 100$  MHz,  $T_C = 25^\circ C$ ,  $V_{OUT(DC)} = 0.5 \times V_{DDQ}$ ,  $V_{OUT}$  (peak-to-peak) = 0.1V.
  - Capacitance is not tested on ZQ ball.
  - DM input is grouped with the I/O balls, because they are matched in loading.
  - $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO} [QK] + C_{IO} [QK\#])$ .
  - Includes CS#, REF#, WE#, A[19:0], and BA[3:0].
  - $C_{DI\_CMD\_ADDR} = C_I$  (CMD\_ADDR) -  $0.5 \times (C_{CK} [CK] + C_{CK} [CK\#])$ .
  - JTAG balls are tested at 50 MHz.



## AC and DC Operating Conditions

**Table 7: DC Electrical Characteristics and Operating Conditions**

Note 1 applies to the entire table; Unless otherwise noted:  $0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.28\text{V} \leq V_{DD} \leq +1.42\text{V}$

Description	Symbol	Min	Max	Units	Notes
Supply voltage	$V_{EXT}$	2.38	2.63	V	
Supply voltage	$V_{DD}$	1.28	1.42	V	
Isolated output buffer supply (standard)	$V_{DDQ}$	1.14	1.26	V	
Isolated output buffer supply (optional for 2400 Mb/s support only)	$V_{DDQ}$	1.28	1.42	V	3
Reference voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2, 4
Input HIGH (logic 1) voltage	$V_{IH(DC)}$	$V_{REF} + 0.10$	$V_{DDQ}$	V	
Input LOW (logic 0) voltage	$V_{IL(DC)}$	$V_{SS}$	$V_{REF} - 0.10$	V	
Input leakage current: Any input $0\text{V} \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ ball $0\text{V} \leq V_{IN} \leq 1.1\text{V}$ (All other balls not under test = 0V)	$I_{LI}$	-2	2	$\mu\text{A}$	
Reference voltage current (All other balls not under test = 0V)	$I_{REF}$	-5	5	$\mu\text{A}$	

- Notes:
- All voltages referenced to  $V_{SS}$  (GND).
  - The nominal value of  $V_{REF}$  is expected to be  $0.5 \times V_{DDQ}$  of the transmitting device.  $V_{REF}$  is expected to track variations in  $V_{DDQ}$ .
  - $1.35V V_{DDQ}$  can only be used to support 2400Mbps operation if required to close timing. It cannot be used to support any slower data rates.  $V_{DDQ}$  must be less than or equal to  $V_{DD}$  at all times.
  - Peak-to-peak noise (non-common mode) on  $V_{REF}$  may not exceed  $\pm 2\%$  of the DC value. DC values are determined to be less than 20 MHz. Peak-to-peak AC noise on  $V_{REF}$  should not exceed  $\pm 2\%$  of  $V_{REF(DC)}$ . Thus, from  $V_{DDQ}/2$ ,  $V_{REF}$  is allowed  $\pm 2\% V_{DDQ}/2$  for DC error and an additional  $\pm 2\% V_{DDQ}/2$  for AC noise. The measurement is to be taken at the nearest  $V_{REF}$  bypass capacitor.

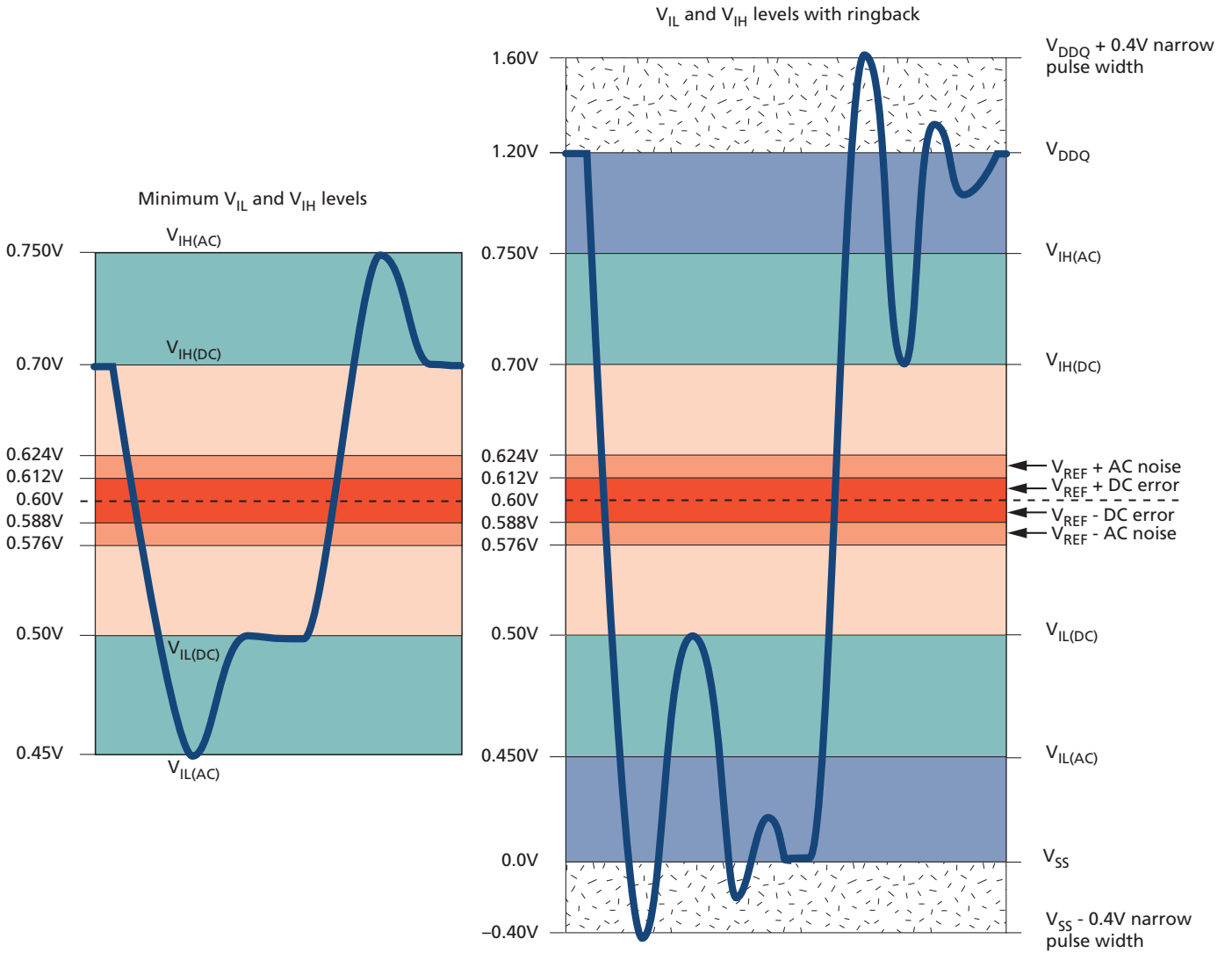
**Table 8: Input AC Logic Levels**

Notes 1-3 apply to entire table; Unless otherwise noted:  $0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.28\text{V} \leq V_{DD} \leq +1.42\text{V}$

Description	Symbol	Min	Max	Units
Input HIGH (logic 1) voltage	$V_{IH(AC150)}$	$V_{REF} + 0.15$	-	V
Input HIGH (logic 1) voltage	$V_{IH(AC135)}$	$V_{REF} + 0.135$	-	V
Input HIGH (logic 1) voltage	$V_{IH(AC120)}$	$V_{REF} + 0.12$	-	V
Input LOW (logic 0) voltage	$V_{IL(AC120)}$	-	$V_{REF} - 0.12$	V
Input LOW (logic 0) voltage	$V_{IL(AC135)}$	-	$V_{REF} - 0.135$	V
Input LOW (logic 0) voltage	$V_{IL(AC150)}$	-	$V_{REF} - 0.15$	V

- Notes:
- All voltages referenced to  $V_{SS}$  (GND).
  - The receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above/below the DC input LOW/HIGH level.
  - Single-ended input slew rate =  $1 \text{ V/ns}$ ; maximum input voltage swing under test is 900mV (peak-to-peak).

**Figure 6: Single-Ended Input Signal**



## AC Overshoot/Undershoot Specifications

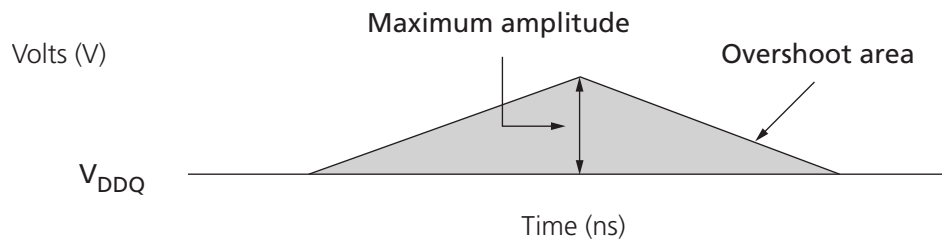
**Table 9: Control and Address Balls**

Parameter	RL3-2400	RL3-2133	RL3-1866
Maximum peak amplitude allowed for overshoot area	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area	0.4V	0.4V	0.4V
Maximum overshoot area above $V_{DDQ}$	0.22 Vns	0.25 Vns	0.28 Vns
Maximum undershoot area below $V_{SS}/V_{SSQ}$	0.22 Vns	0.25 Vns	0.28 Vns

**Table 10: Clock, Data, Strobe, and Mask Balls**

Parameter	RL3-2400	RL3-2133	RL3-1866
Maximum peak amplitude allowed for overshoot area	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area	0.4V	0.4V	0.4V
Maximum overshoot area above $V_{DDQ}$	0.09 Vns	0.10 Vns	0.11 Vns
Maximum undershoot area below $V_{SS}/V_{SSQ}$	0.09 Vns	0.10 Vns	0.11 Vns

**Figure 7: Overshoot**



**Figure 8: Undershoot**

