Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Async/Page/Burst CellularRAM® 1.0 Memory

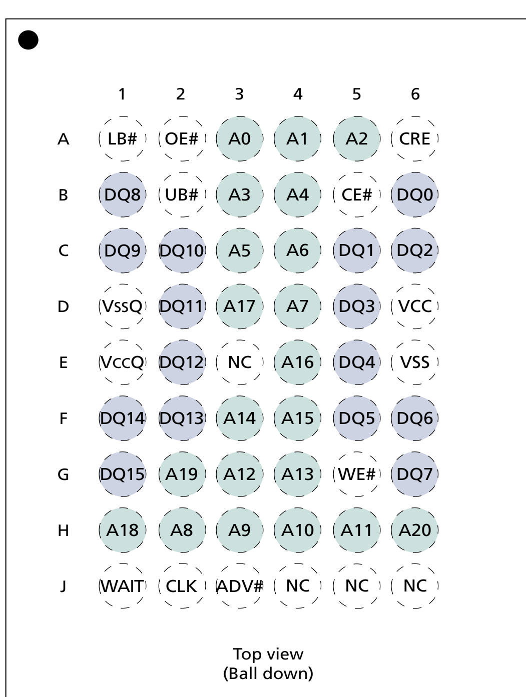
MT45W2MW16BGB

Features

- Single device supports asynchronous, page, and burst operations
- Random access time: 70ns
- VCC, VCCQ voltages
  – 1.7–1.95V VCC
  – 1.7–3.6V VCCQ
- Page mode read access
  – 16-word page size
  – Interpage read access: 70ns
  – Intrapage read access: 20ns
- Burst mode write access: continuous burst
- Burst mode read access
  – 4, 8, or 16 words or continuous burst
  – MAX clock rate: 104 MHz (^{t}CLK = 9.62ns)
  – Burst initial latency: 38.5ns (4 clocks) at 104 MHz
  – ^{t}ACLK: 7ns at 104 MHz
- Low power consumption
  – Asynchronous read: <20mA
  – Intrapage read: <15mA
  – Intrapage read initial access, burst read: (38.5ns [4 clocks] at 104 MHz) <40mA
  – Continuous burst read: <25mA
  – Standby: <110µA
  – Deep power-down: <10µA (TYP at 25°C)
- Low-power features
  – Temperature-compensated refresh (TCR)
  – On-chip temperature sensor
  – Partial-array refresh (PAR)
  – Deep power-down (DPD) mode

Options	Designator
• Configuration	
– 2 Meg x 16	MT45W2MW16B
• Package	
– 54-ball VFBGA (“green”)	GB
• Access time	
– 70ns	-70
• Frequency	
– 80 MHz	8
– 104 MHz	1

Figure 1: 54-Ball VFBGA Ball Assignment



Options (continued)	Designator
• Standby power	
– Standard	None
• Low power	L
• Operating temperature range	
– Wireless (–30°C to +85°C)	WT1
– Industrial (–40°C to +85°C)	IT2

Notes: 1. –30°C exceeds the CellularRAM Workgroup 1.0 specification of –25°C.
2. Contact factory for availability.

Part Number Example:

MT45W2MW16BGB-701WT

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Products and specifications discussed herein are subject to change by Micron without notice.

Table of Contents

Features 1
Options 1
General Description 5
Functional Block Diagram 6
Ball Descriptions 7
Bus Operations 8
Part Numbering Information 10
Valid Part Number Combinations 10
Device Marking 10
Functional Description 11
Power-Up Initialization 11
Bus Operating Modes 11
Asynchronous Mode 11
Page Mode READ Operation 13
Burst Mode Operation 13
Mixed-Mode Operation 16
WAIT Operation 16
LB#/UB# Operation 16
Low-Power Operation 19
Standby Mode Operation 19
Temperature-Compensated Refresh 19
Partial-Array Refresh 19
Deep Power-Down Operation 19
Configuration Registers 20
Access Using CRE 20
Software Access to the Configuration Register 24
Bus Configuration Register 26
Burst Length (BCR[2:0]) Default = Continuous Burst 27
Burst Wrap (BCR[3]) Default = Burst No Wrap (Within Burst Length) 27
Output Impedance (BCR[5]) Default = Outputs Use Full Drive Strength 28
WAIT Configuration (BCR[8]) Default = WAIT Transitions One Clock Before Data Valid/Invalid 28
WAIT Polarity (BCR[10]) Default = WAIT Active HIGH 29
Latency Counter (BCR[13:11]) Default = Three-Clock Latency 29
Operating Mode (BCR[15]) Default = Asynchronous Operation 29
Refresh Configuration Register 31
Partial-Array Refresh (RCR[2:0]) Default = Full Array Refresh 31
Deep Power-Down (RCR[4]) Default = DPD Disabled 32
Page Mode Operation (RCR[7]) Default = Disabled 32
Electrical Characteristics 32
Maximum and Typical Standby Currents 34
Timing Requirements 36
Timing Diagrams 40
Package Dimensions 60
Revision History 61

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

List of Figures

Figure 1: 54-Ball VFBGA Ball Assignment 1
Figure 2: Functional Block Diagram – 2 Meg x 16 6
Figure 3: Part Number Chart 10
Figure 4: Power-Up Initialization Timing 11
Figure 5: READ Operation (ADV = LOW) 12
Figure 6: WRITE Operation (ADV = LOW) 12
Figure 7: Page Mode READ Operation (ADV = LOW) 13
Figure 8: Burst Mode READ (4-Word Burst) 14
Figure 9: Burst Mode WRITE (4-Word Burst) 15
Figure 10: Wired-OR WAIT Configuration 16
Figure 11: Refresh Collision During READ Operation 17
Figure 12: Refresh Collision During WRITE Operation 18
Figure 13: Asynchronous Mode Configuration Register WRITE Followed by READ ARRAY Operation 20
Figure 14: Synchronous Mode Configuration Register WRITE Followed by READ ARRAY Operation 21
Figure 15: Asynchronous Mode Configuration Register READ Followed by READ ARRAY Operation 22
Figure 16: Synchronous Mode Configuration Register READ Followed by READ ARRAY Operation 23
Figure 17: Load Configuration Register 24
Figure 18: Read Configuration Register 25
Figure 19: Bus Configuration Register Definition 26
Figure 20: WAIT Configuration (BCR[8] = 0) 28
Figure 21: WAIT Configuration (BCR[8] = 1) 28
Figure 22: WAIT Configuration During Burst Operation 29
Figure 23: Latency Counter (Variable Latency, No Refresh Collision) 30
Figure 24: Refresh Configuration Register Mapping 31
Figure 25: Typical Refresh Current vs. Temperature 34
Figure 26: AC Input/Output Reference Waveform 35
Figure 27: Output Load Circuit 35
Figure 28: Initialization Period 39
Figure 29: Asynchronous READ 40
Figure 30: Asynchronous READ Using ADV# 41
Figure 31: Page Mode READ 42
Figure 32: Single-Access Burst READ Operation 43
Figure 33: 4-Word Burst READ Operation 44
Figure 34: READ Burst Suspend 45
Figure 35: Output Delay in Continuous Burst READ with BCR[8] = 0 for End-of-Row Condition 46
Figure 36: CE#-Controlled Asynchronous WRITE 47
Figure 37: LB#/UB#-Controlled Asynchronous WRITE 48
Figure 38: WE#-Controlled Asynchronous WRITE 49
Figure 39: Asynchronous WRITE Using ADV# 50
Figure 40: Burst WRITE Operation 51
Figure 41: Output Delay in Continuous Burst WRITE with BCR[8] = 0 for End-of-Row Condition 52
Figure 42: Burst WRITE Followed by Burst READ 53
Figure 43: Asynchronous WRITE Followed by Burst READ 54
Figure 44: Asynchronous WRITE Followed by Burst READ with ADV# LOW 55
Figure 45: Burst READ Followed by Asynchronous WRITE (WE#-Controlled) 56
Figure 46: Burst READ Followed by Asynchronous WRITE Using ADV# 57
Figure 47: Asynchronous WRITE Followed by Asynchronous READ with ADV# LOW 58
Figure 48: Asynchronous WRITE Followed by Asynchronous READ 59
Figure 49: 54-Ball VFBGA 60

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

List of Tables

Table 1: VFBGA Ball Descriptions . . . 7
Table 2: Bus Operations: Asynchronous Mode . . . 8
Table 3: Bus Operations: Burst Mode . . . 9
Table 4: Sequence and Burst Length . . . 27
Table 5: Latency Configuration . . . 29
Table 6: 32Mb Address Patterns for PAR (RCR[4] = 1) . . . 32
Table 7: Absolute Maximum Ratings . . . 32
Table 8: Electrical Characteristics and Operating Conditions . . . 33
Table 9: Partial-Array Refresh Specifications and Conditions . . . 34
Table 10: Deep Power-Down Specifications . . . 35
Table 11: Capacitance . . . 35
Table 12: Asynchronous READ Cycle Timing Requirements . . . 36
Table 13: Burst READ Cycle Timing Requirements . . . 37
Table 14: Asynchronous WRITE Cycle Timing Requirements . . . 38
Table 15: Burst WRITE Cycle Timing Requirements . . . 39
Table 16: Initialization Timing Parameters . . . 39

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

General Description

Micron® CellularRAM® is a high-speed, CMOS PSRAM memory device developed for low-power, portable applications. The MT45W2MW16BGB is a 32Mb DRAM core device organized as 2 Meg x 16 bits. This device includes an industry-standard burst mode Flash interface that dramatically increases READ/WRITE bandwidth compared with other low-power SRAM or pseudo-SRAM (PSRAM) offerings.

For seamless operation on a burst Flash bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device READ/WRITE performance.

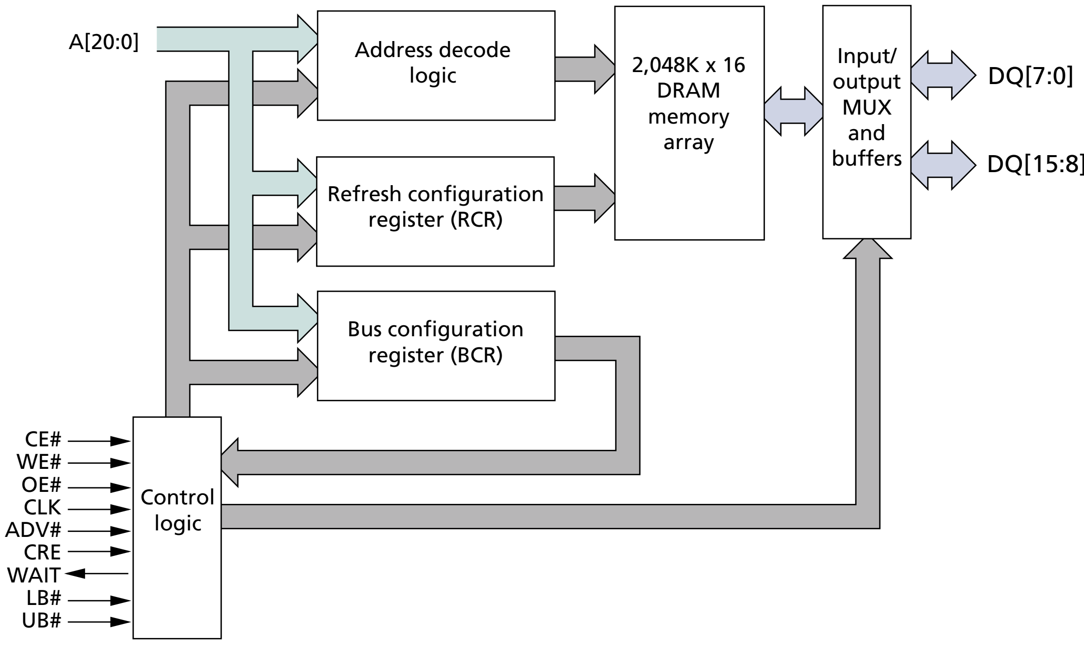
Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three system-accessible mechanisms to minimize standby current. Partial-array refresh (PAR) limits refresh to only that part of the DRAM array that contains essential data. Temperature-compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature. The refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) halts the REFRESH operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the RCR.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Functional Block Diagram

Figure 2: Functional Block Diagram – 2 Meg x 16



Note: Functional block diagrams illustrate simplified device operation. See ball description table, bus operations tables, and timing diagrams for detailed information.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Ball Descriptions

Table 1: VFBGA Ball Descriptions

VFBGA Assignment	Symbol	Type	Description
H6, G2, H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3	A[20:0]	Input	Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
J3	ADV#	Input	Address valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations.
B5	CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
J2	CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK must be static LOW or HIGH during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
A6	CRE	Input	Configuration register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations either access the RCR or the BCR.
A1	LB#	Input	Lower byte enable: DQ[7:0].
A2	OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
B2	UB#	Input	Upper byte enable: DQ[15:8].
G5	WE#	Input	WRITE enable: Determines whether a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or the memory array.
G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6	DQ[15:0]	Input/ Output	Data inputs/outputs.
J1	WAIT	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between REFRESH and READ/WRITE operations. WAIT is asserted when a burst crosses a row boundary. WAIT is also used to mask the delay associated with opening a new internal page. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH.
E3, J4, J5, J6	NC	–	Not internally connected.
D6	V_{CC}	Supply	Device power supply (1.7–1.95V): Power supply for device core operation.
E1	$V_{CC}Q$	Supply	I/O power supply (1.7–3.6V): Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	$V_{SS}Q$	Supply	$V_{SS}Q$ must be connected to ground.

Note: The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous or page mode. WAIT will be asserted, but should be ignored during asynchronous and page mode operations.

©2007 Micron Technology, Inc. All rights reserved.

Bus Operations

Table 2: Bus Operations: Asynchronous Mode

Mode	Power	CLK[1]	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[2]	DQ[15:0][3]	Notes
READ	Active	L	L	L	L	H	L	L	Low-Z	Data-out	4
WRITE	Active	L	L	L	X	L	L	L	Low-Z	Data-in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration register WRITE	Active	L	L	L	H	L	H	X	Low-Z	High-Z	
Configuration register READ	Active	L	L	L	H	H	H	X	Low-Z	Config. reg. out	8
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7

Notes:
1. CLK must be static (HIGH or LOW) during asynchronous READ and asynchronous WRITE modes and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. $V_{IN} = V_{CC}Q$ or 0V; all device balls must be static (unswitched) to achieve standby current.
7. DPD is maintained until RCR is reconfigured.
8. CRE-controlled reading of the configuration register is supported for this device, though it is not an official CellularRAM 1.0 feature.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Table 3: Bus Operations: Burst Mode

Mode	Power	CLK[1]	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[2]	DQ[15:0][3]	Notes
Asynchronous READ	Active	L	L	L	L	H	L	L	Low-Z	Data-out	4
Asynchronous WRITE	Active	L	L	L	X	L	L	L	Low-Z	Data-in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4, 6
Initial burst READ	Active	↑	L	L	X	H	L	L	Low-Z	X	4, 8
Initial burst WRITE	Active	↑	L	L	H	L	L	X	Low-Z	X	4, 8
Burst continue	Active	↑	H	L	X	X	X	L	Low-Z	Data-in or data-out	4, 8
Burst suspend	Active	X	X	L	H	X	L	X	Low-Z	High-Z	4, 8
Configuration register WRITE	Active	↑	L	L	H	L	H	X	Low-Z	High-Z	8
Configuration register READ	Active	↑	L	L	H	H	H	X	Low-Z	Config. reg. out Z	8, 9
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7

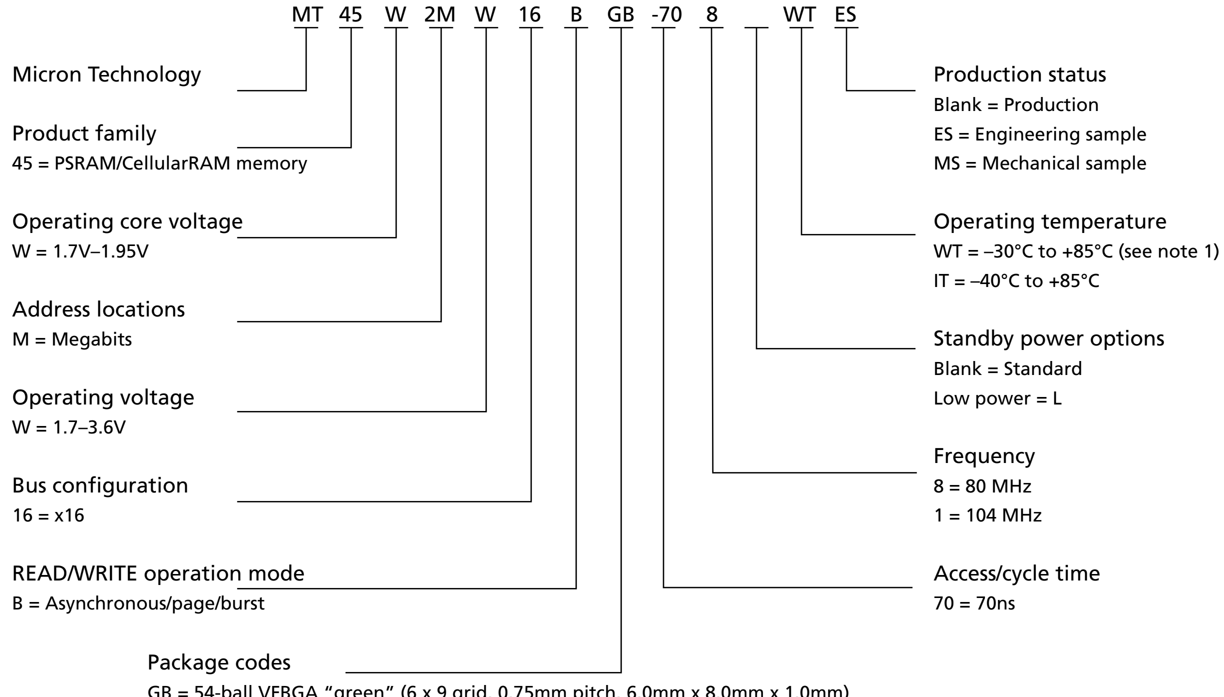
Notes:
1. CLK must be static (HIGH or LOW) during asynchronous READ and asynchronous WRITE modes and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. V_{IN} = $V_{CC}Q$ or 0V; all device balls must be static (unswitched) to achieve standby current.
7. DPD is maintained until RCR is reconfigured.
8. Burst mode operation is initialized through the bus configuration register (BCR[15]).
9. This device supports CRE-controlled configuration register READs. This feature is not an official CellularRAM 1.0 feature.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Part Numbering Information

Micron CellularRAM devices are available in several configurations and densities.

Figure 3: Part Number Chart



Note: –30°C exceeds the CellularRAM Workgroup 1.0 specification of –25°C.

Valid Part Number Combinations

After building the part number from the part numbering chart, visit the Micron Web site at www.micron.com/psram to verify that the part number is offered and valid. If the device required is not on this list, contact the factory.

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site, http://www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note, CSN-11, “Product Mark/Label,” at www.micron.com/csn.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Functional Description

In general, the MT45W2MW16BGB devices are high-density alternatives to SRAM and PSRAM products, popular in low-power, portable applications.

The MT45W2MW16BGB contains a 33,554,432-bit DRAM core organized as 2,097,152 addresses by 16 bits. This device implements the same high-speed bus interface found on burst mode Flash products.

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous READ protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Figure 19 on page 26 and Figure 24 on page 31). V_{CC} and $V_{CC}Q$ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 4: Power-Up Initialization Timing

Vcc = 1.7V
Vcc
VccQ
^{t}PU ≥ 150µs
Device initialization
Device ready for normal operation

Bus Operating Modes

The MT45W2MW16BGB CellularRAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode READ and WRITE transfers. The specific interface supported is defined by the value loaded into the bus configuration register. Page mode is controlled by the refresh configuration register (RCR[7]).

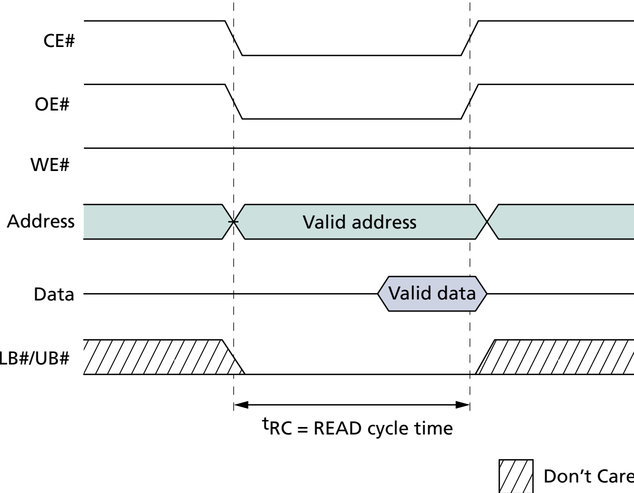
Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, and LB#/UB#). READ operations are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH (see Figure 5 on page 12). Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations occur when CE#, WE#, and LB#/UB# are driven LOW (see Figure 6 on page 12). During asynchronous WRITE operations, the OE# level is a “Don't Care,” and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB#, whichever occurs first. Asynchronous operations (page mode disabled) either can use the ADV input to latch the address, or ADV can be driven LOW during the entire READ/WRITE operation.

During asynchronous operation, the CLK input must be held static LOW or HIGH. WAIT will be driven while the device is enabled, and its state should be ignored. WE# LOW time must be limited to ^{t}CEM.

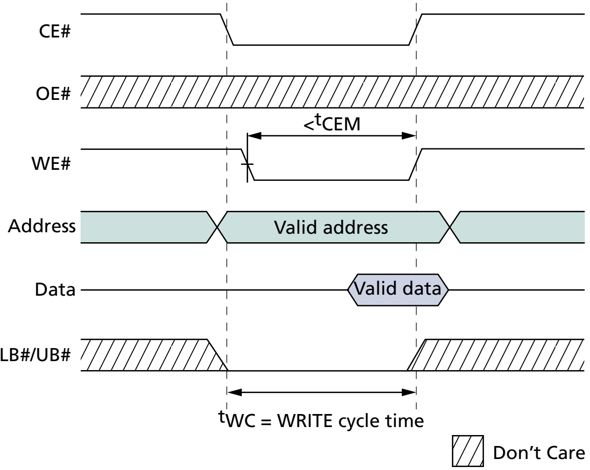
Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Figure 5: READ Operation (ADV = LOW)



Note: ADV must remain LOW for page mode operation.

Figure 6: WRITE Operation (ADV = LOW)



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Page Mode READ Operation

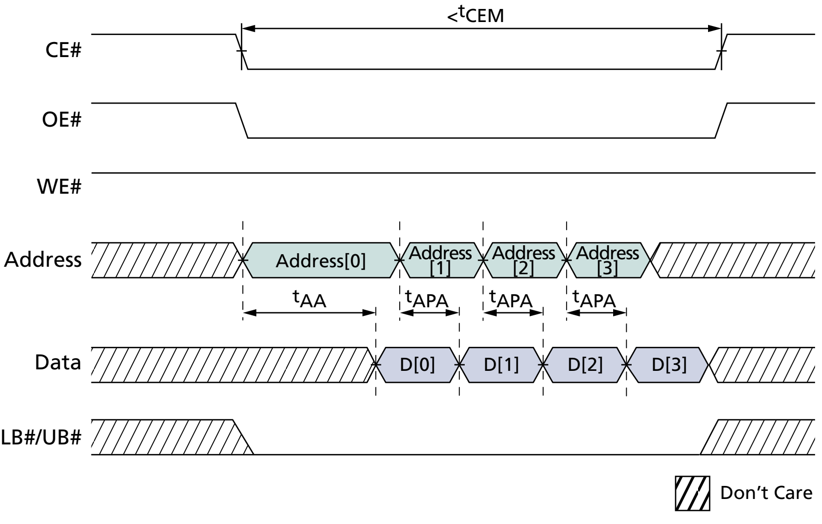
Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous READ access is performed, and then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new ^{t}AA access time. Figure 7 on page 13 shows the timing for a page mode access.

Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be held static LOW or HIGH. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled, and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. ADV must be driven LOW during all page mode READ accesses.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than ^{t}CEM.

Figure 7: Page Mode READ Operation (ADV = LOW)



Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multiclock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the next rising edge of CLK that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 8 on page 14) or WRITE (WE# = LOW, Figure 9 on page 15).

The size of a burst can be specified in the BCR either as fixed-length or continuous. Fixed-length bursts consist of 4, 8, or 16 words. Continuous bursts have the ability to start at a specified address and burst through the entire memory. The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device.

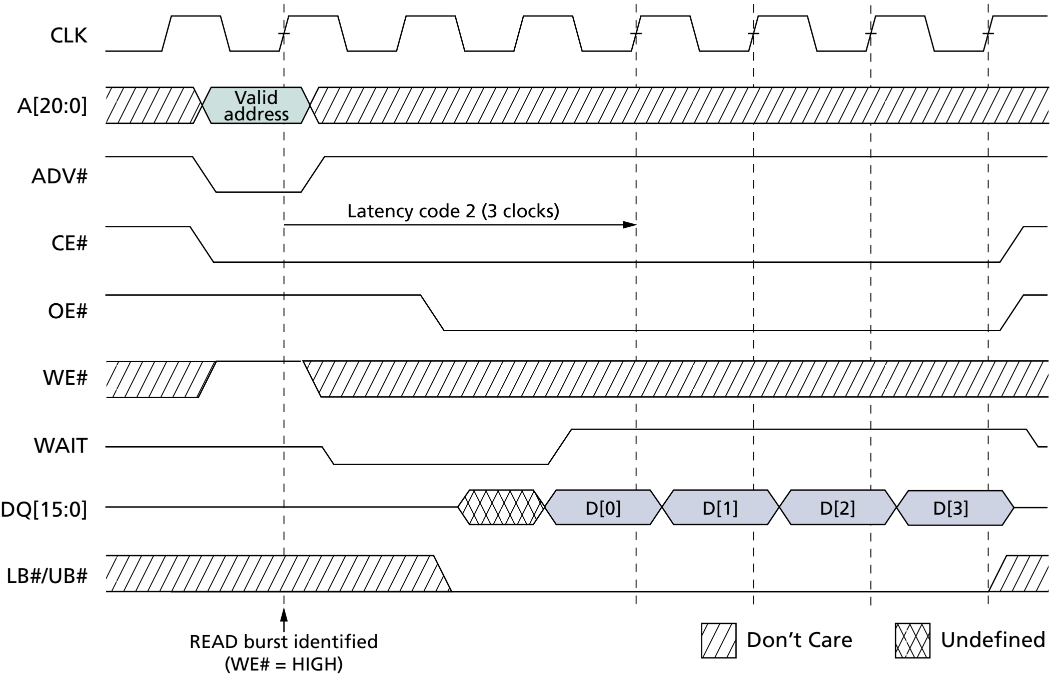
Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

The WAIT output will be asserted as soon as CE# goes LOW and will be de-asserted to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted if the burst crosses the boundary between 128-word rows. After the CellularRAM device has restored the previous row's data and accessed the next row, WAIT will be deasserted and the burst can continue (see Figure 35 on page 46).

The processor can access other devices without incurring the timing penalty of the initial latency for a new burst by suspending burst mode. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be active, and, as a result, no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, and then CLK is restarted after valid data is available on the bus.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than ^{t}CEM unless row boundaries are crossed at least every ^{t}CEM. If a burst suspension will cause CE# to remain LOW for longer than ^{t}CEM, CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

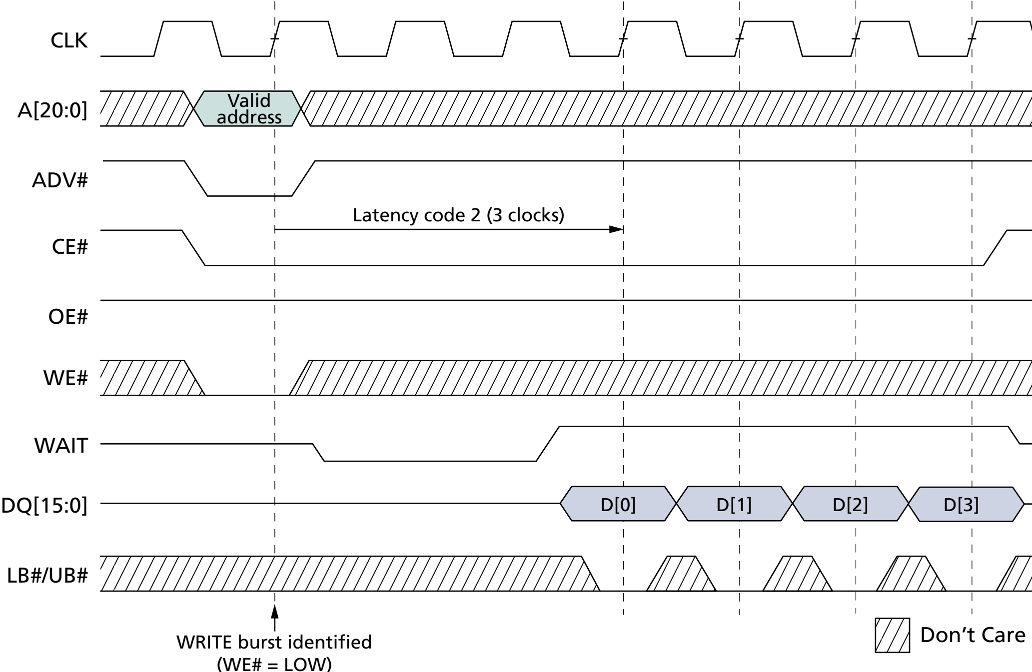
Figure 8: Burst Mode READ (4-Word Burst)



Note: Nondefault BCR settings: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Figure 9: Burst Mode WRITE (4-Word Burst)



Note: Nondefault BCR settings: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

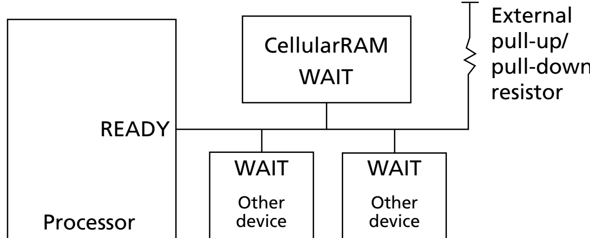
Mixed-Mode Operation

The device can support a combination of synchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. The asynchronous WRITE operation requires that the clock (CLK) be held static LOW or HIGH during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# must return HIGH when transitioning between mixed-mode operations. Note that the ^{t}CKA period is the same as a READ or WRITE cycle. This time is required to ensure adequate refresh. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers (see Figure 43 on page 54).

WAIT Operation

The WAIT output on a CellularRAM device is typically connected to a shared, system-level WAIT signal (see Figure 10). The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

Figure 10: Wired-OR WAIT Configuration



After a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

During a burst cycle, CE# must remain asserted until the first data is valid. Bringing CE# HIGH during this initial latency may cause data corruption.

The WAIT output also performs an arbitration role when a READ or WRITE operation is launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed (see Figure 11 on page 17 and Figure 12 on page 18). When the REFRESH operation has completed, the READ or WRITE operation will continue normally.

WAIT is also asserted when a continuous READ or WRITE burst crosses a row boundary. The WAIT assertion allows time for the new row to be accessed and permits any pending REFRESH operations to be performed.

LB#/UB# Operation

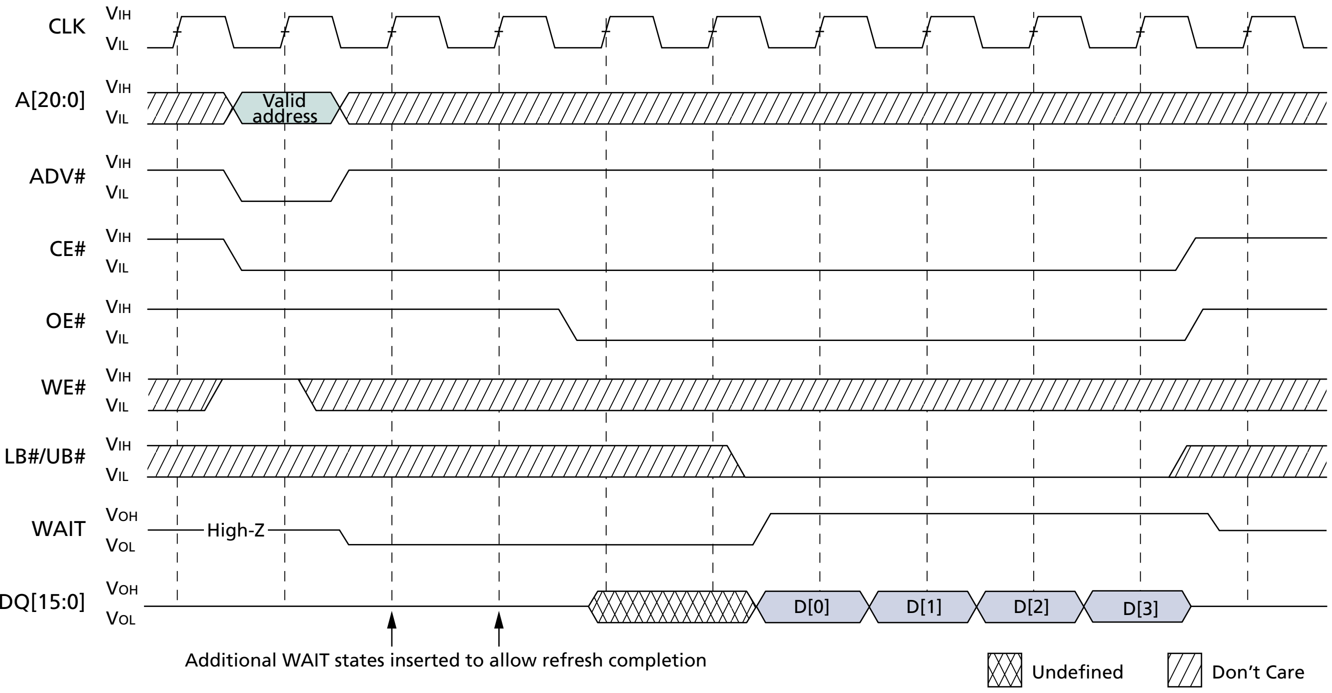
The LB# enable and UB# enable signals support byte-wide data transfers. During READ operations, the enabled byte(s) are driven onto the DQ. The DQ associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE oper-

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

ations, any disabled bytes will not be transferred to the RAM array, and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

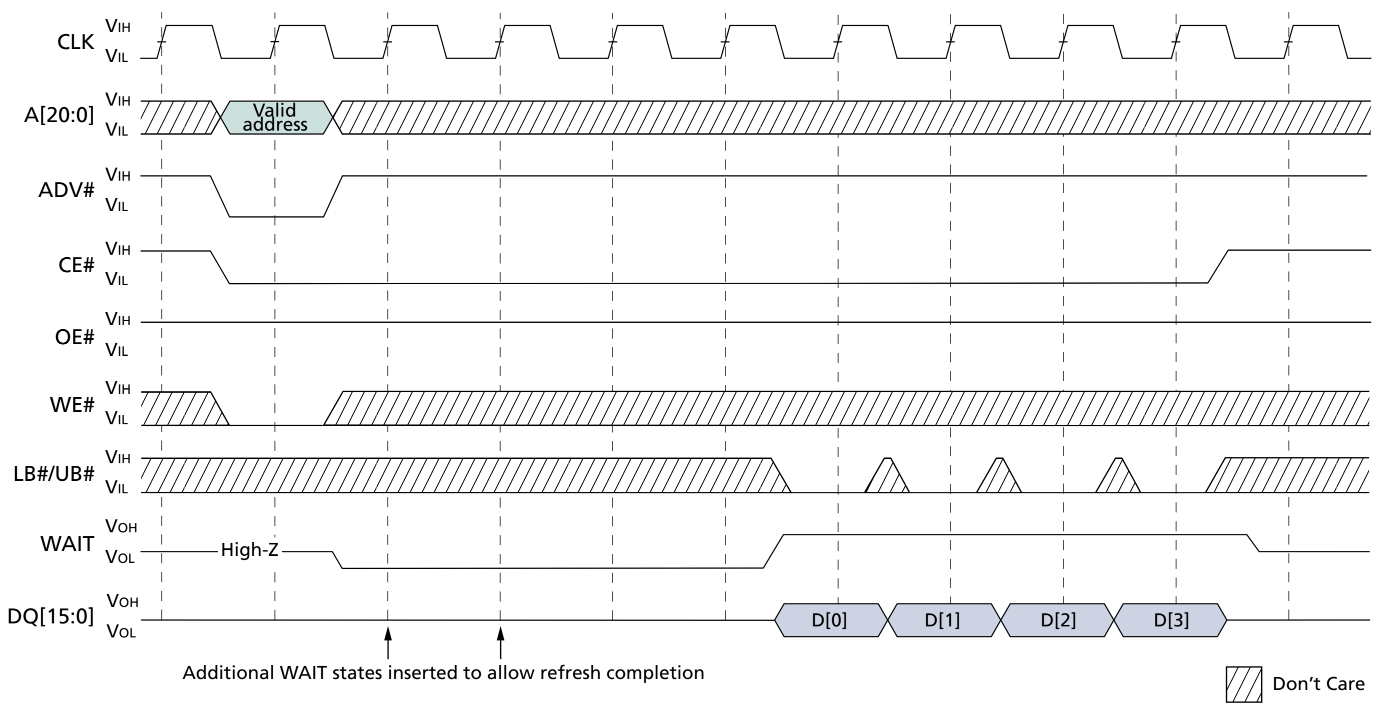
Figure 11: Refresh Collision During READ Operation



Note: Nondefault BCR settings: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Figure 12: Refresh Collision During WRITE Operation



Note: Nondefault BCR settings: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Low-Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM REFRESH operation. Standby operation occurs when CE# is HIGH.

The device will enter a reduced power state upon completion of a READ or WRITE operation or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature-Compensated Refresh

Temperature-compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor that continually adjusts the refresh rate according to the operating temperature.

Partial-Array Refresh

Partial-array refresh (PAR) restricts REFRESH operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions either can start at the beginning or the end of the address map (see Table 6 on page 32). READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When reenabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been reenabled by rewriting the RCR, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

DPD cannot be enabled or disabled by writing to the RCR using the software access sequence; the RCR should be accessed using CRE instead.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Configuration Registers

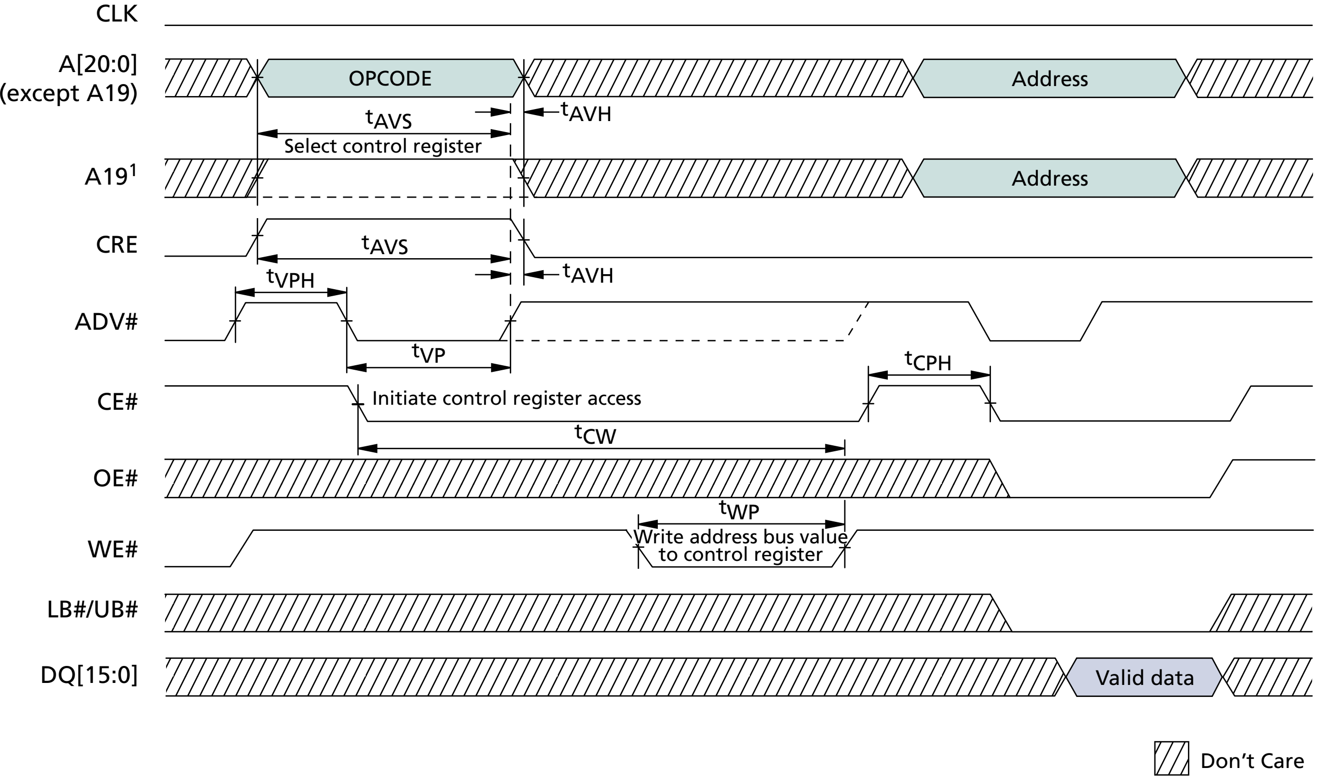
Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated any time the devices are operating in a standby state.

Access Using CRE

The configuration registers are loaded using either a synchronous or an asynchronous WRITE operation when the configuration register enable (CRE) input is HIGH (see Figure 13, and Figure 14 on page 21). When CRE is LOW, a READ or WRITE operation will access the memory array. The register values are placed on address pins A[19:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are "Don't Care." The BCR is accessed when A[19] is HIGH; the RCR is accessed when A[19] is LOW. For READs, address inputs other than A19 are "Don't Care," and register bits 15:0 are output on DQ[15:0].

Figure 13: Asynchronous Mode Configuration Register WRITE Followed by READ ARRAY Operation

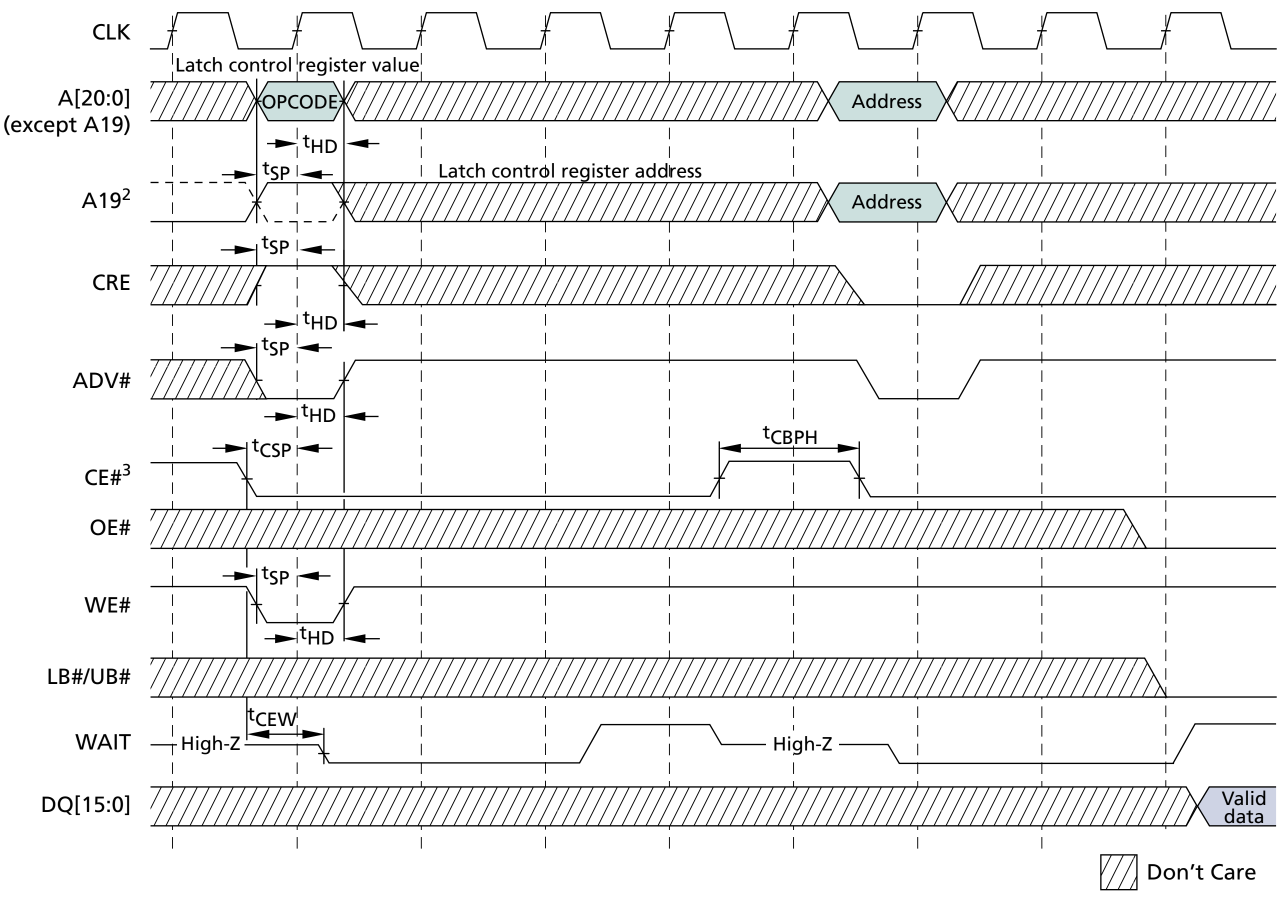
Note:



Note: A[19] = LOW to load RCR, HIGH to load BCR.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

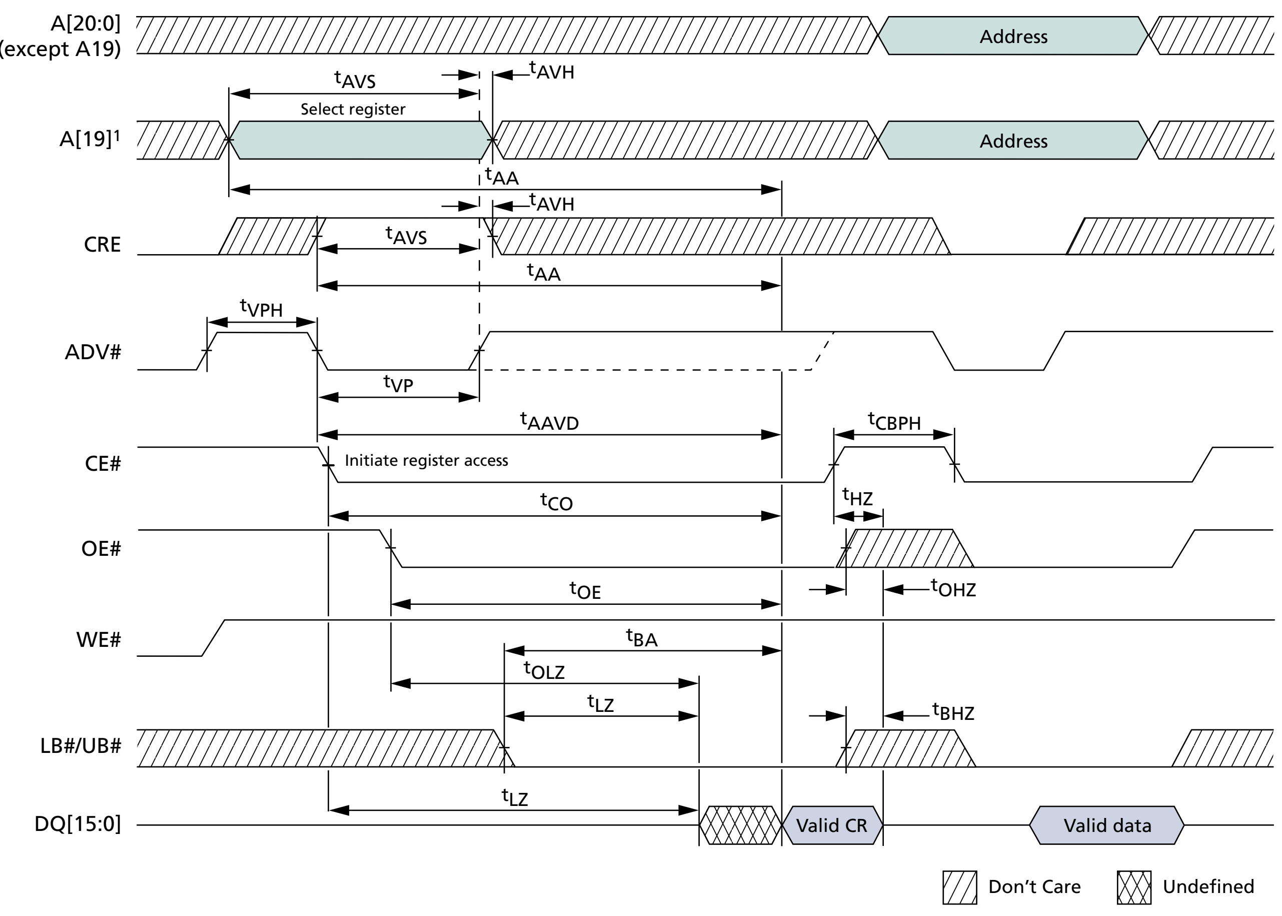
Figure 14: Synchronous Mode Configuration Register WRITE Followed by READ ARRAY Operation



Notes:
1. Nondefault BCR settings for CR WRITE in synchronous mode followed by READ ARRAY operation: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19] = LOW to load RCR, HIGH to load BCR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Figure 15: Asynchronous Mode Configuration Register READ Followed by READ ARRAY Operation



Note: A[19] = LOW to read RCR, HIGH to read BCR.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Figure 16: Synchronous Mode Configuration Register READ Followed by READ ARRAY Operation

Notes:
1. Nondefault BCR settings for synchronous mode register READ followed by READ ARRAY operation: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19] = LOW to read RCR, HIGH to read BCR.
3. CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Software Access to the Configuration Register

Software access of the configuration registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be read or modified using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 17). The READ sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 18 on page 25).

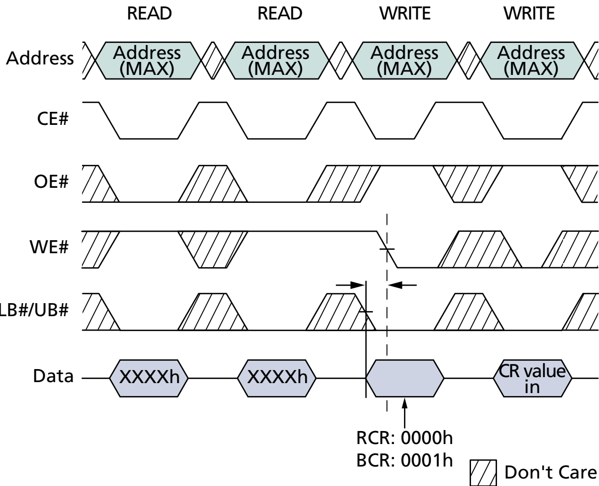
The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (1FFFFFh for 32Mb); the content at this address is not changed by using this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR or the RCR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR. During the fourth operation, DQ[15:0] transfer data into or out of bits 15–0 of the configuration registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for the control register enable (CRE) pin. If the software mechanism is used, the CRE pin can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

Software access of the RCR should not be used to enter or exit DPD.

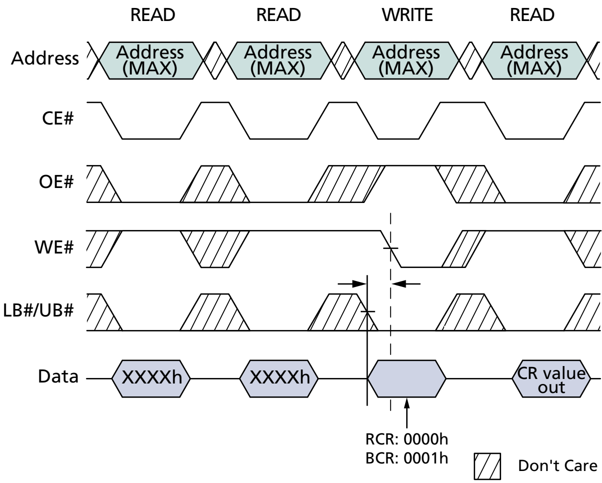
Figure 17: Load Configuration Register



Note: It is possible that the data stored at the highest memory location will be altered if the data at the falling edge of WE# is not 0000h or 0001h.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.

Figure 18: Read Configuration Register



Note: It is possible that the data stored at the highest memory location will be altered if the data at the falling edge of WE# is not 0000h or 0001h.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2007 Micron Technology, Inc. All rights reserved.