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Async/Page/Burst CellularRAM® 1.5 Memory

MT45W4MW16BCGB

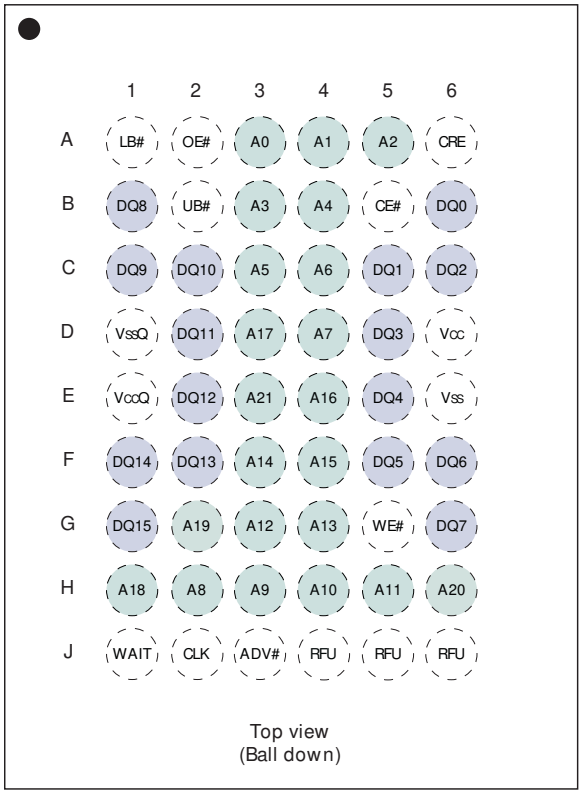
Features

- Single device supports asynchronous, page, and burst operations
- VCC, VCCQ voltages:
  - 1.7–1.95V VCC
  - 1.7–3.3V VCCQ[1]
- Random access time: 70ns
- Burst mode READ and WRITE access
  - 4, 8, 16, or 32 words or continuous burst
  - Burst wrap or sequential
  - MAX clock rate: 133 MHz[1] (^{t}CLK = 7.5ns)
  - Burst initial latency: 37.5ns (5 clocks) at 133 MHz
  - ^{t}ACLK: 5.5ns at 133 MHz
- Page mode read access
  - 16-word page size
  - Interpage read access: 70ns
  - Intrapage read access: 20ns
- Low power consumption
  - Asynchronous READ: <25mA
  - Intrapage READ: <15mA
  - Initial access, burst READ: (37.5ns [5 clocks] at 133 MHz) <45mA
  - Continuous burst READ: <40mA
  - Standby: <50µA (TYP at 25°C)
  - Deep power-down (DPD): <3µA (TYP)
- Low-power features
  - On-chip temperature-compensated refresh (TCR)
  - Partial-array refresh (PAR)
  - DPD mode

Options

Options	Designator
• Configuration: 4 Meg x 16 VCC core voltage supply: 1.7–1.95V VCCQ I/O voltage supply: 1.7–3.3V[1]	MT45W4MW16BC
• Package 54-ball VFBGA (“green”)	GB
• Access time 70ns	-70
• Frequency: 133 MHz	13
104 MHz	1
80 MHz	8

Figure 1: 54-Ball VFBGA Ball Assignment



Options (continued)

Options (continued)	Designator
• Standby power at 85°C	
– Standard: 140µA (MAX)	None
– Low power: 120µA (MAX)	L
• Operating temperature range	
– Wireless (–30°C to +85°C)	WT
– Industrial (–40°C to +85°C)	IT

Notes: 1. The 3.3V I/O voltage and 133 MHz clock frequency exceed the CellularRAM 1.5 Workgroup specification.

Part Number Example:

MT45W4MW16BCGB-701LWT

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General Description

Micron® CellularRAM® products are high-speed, CMOS memory devices developed for low-power, portable applications. The MT45W4MW16BCGB is a 64Mb DRAM core device, organized as 4 Meg x 16 bits. This device includes an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or pseudo-SRAM (PSRAM) offerings.

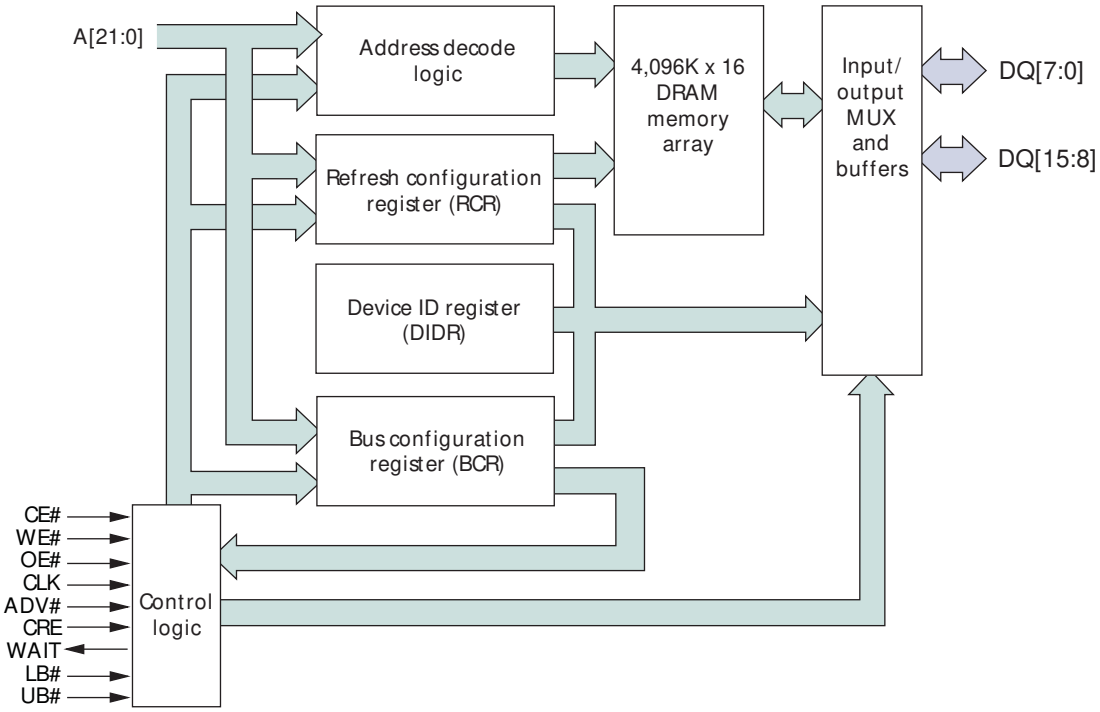
For seamless operation on a burst Flash bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current. Partial-array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature-compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system configurable refresh mechanisms are accessed through the RCR.

This CellularRAM device is compliant with the industry-standard CellularRAM 1.5 feature set established by the CellularRAM Workgroup. It includes support for both variable and fixed latency, with three output-device drive-strength settings, additional wrap options, and a device ID register (DIDR).

Figure 2: Functional Block Diagram – 4 Meg x 16



Note: Functional block diagrams illustrate simplified device operation. For detailed information, see ball descriptions in Table 1 on page 7; bus operations in Table 2 on page 8, Table 3 on page 9, and Table 2 on page 8; and timing diagrams starting on page 42.

Table 1: VFBGA Ball Descriptions

VFBGA Assignment	Symbol	Type	Description
E3, H6, G2, H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3	A[21:0]	Input	Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
J2	CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK must be static LOW during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
J3	ADV#	Input	Address valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations.
A6	CRE	Input	Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
B5	CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or DPD mode.
A2	OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write enable: Determines whether a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE either to a configuration register or to the memory array.
A1	LB#	Input	Lower byte enable. DQ[7:0]
B2	UB#	Input	Upper byte enable. DQ[15:8]
G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6	DQ[15:0]	Input/ Output	Data inputs/outputs.
J1	WAIT	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is asserted at the end of a row unless wrapping within the burst length. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH.
J4, J5, J6	RFU	–	Reserved for future use.
D6	V_{CC}	Supply	Device power supply (1.7–1.95V): Power supply for device core operation.
E1	V_{CCQ}	Supply	I/O power supply (1.7–3.3V): Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	V_{SSQ}	Supply	V_{SSQ} must be connected to ground.

Note: The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous or page mode. WAIT will be asserted, but should be ignored during asynchronous and page mode operations.

Table 2: Bus Operations – Asynchronous Mode (BCR[15] = 1; Default)

Mode	Power	CLK[1]	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[2]	DQ[15:0][3]	Notes
Read	Active	L	L	L	L	H	L	L	Low-Z	Data-out	4
Write	Active	L	L	L	X	L	L	L	Low-Z	Data-in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration register write	Active	L	L	L	H	L	H	X	Low-Z	High-Z	
Configuration register read	Active	L	L	L	L	H	H	L	Low-Z	Config. reg. out	
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7

Notes:
1. CLK must be LOW during asynchronous read and asynchronous write modes and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are enabled. When only LB# is in select mode, DQ[7:0] are enabled. When only UB# is in the select mode, DQ[15:8] are enabled.

Table 3: Bus Operations – Burst Mode (BCR[15] = 0)

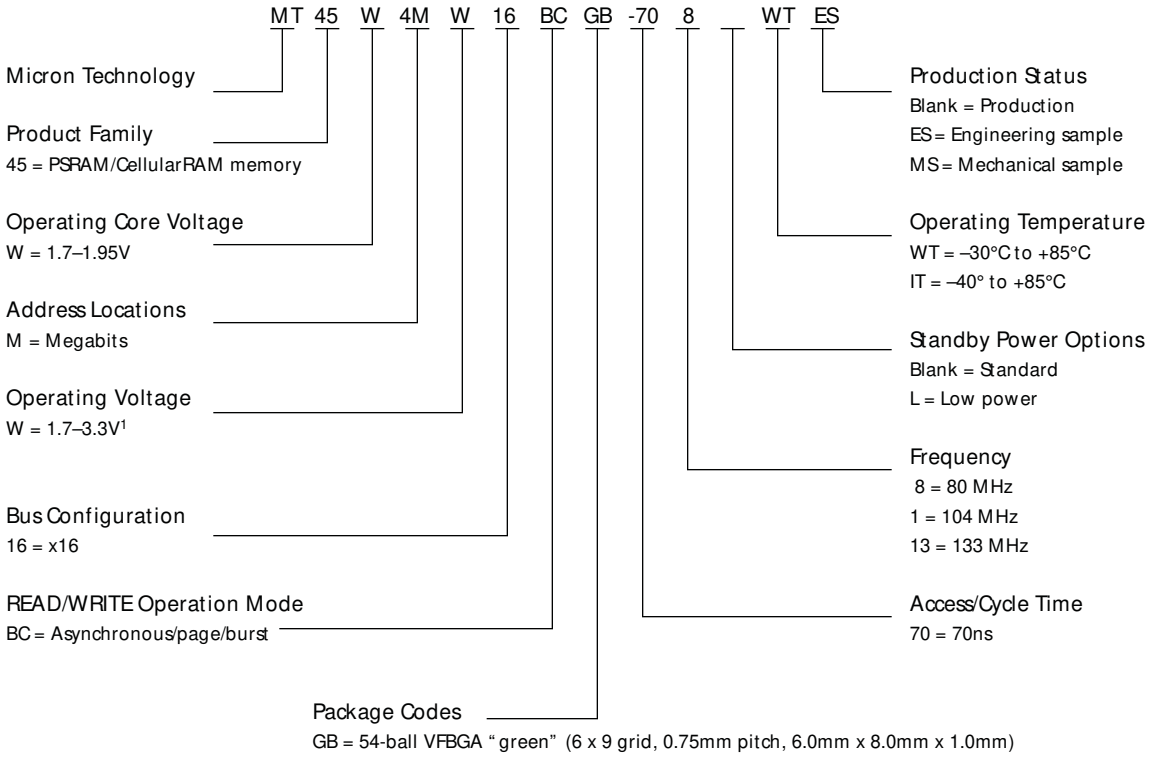
Mode	Power	CLK[1]	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[2]	DQ[15:0][3]	Notes
Asynchronous read	Active	L	L	L	L	H	L	L	Low-Z	Data-out	4
Asynchronous write	Active	L	L	L	X	L	L	L	Low-Z	Data-in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4, 6
Initial burst read	Active	⎍	L	L	X	H	L	L	Low-Z	X	4, 8
Initial burst write	Active	⎍	L	L	H	L	L	X	Low-Z	X	4, 8
Burst continue	Active	⎍	H	L	X	X	X	L	Low-Z	Data-in or data-out	4, 8
Burst suspend	Active	X	X	L	H	X	X	X	Low-Z	High-Z	4, 8
Configuration register write	Active	⎍	L	L	H	L	H	X	Low-Z	High-Z	8, 9
Configuration register read	Active	⎍	L	L	L	H	H	L	Low-Z	Config. reg. out	8, 9
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7

Notes:
1. CLK must be LOW during asynchronous read and asynchronous write modes and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are enabled. When only LB# is in select mode, DQ[7:0] are enabled. When only UB# is in the select mode, DQ[15:8] are enabled.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. V_{IN} = V_{CCQ} or 0V; all device balls must be static (unswitched) to achieve standby current.
7. DPD is initiated when CE# transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until CE# transitions from HIGH to LOW and is held LOW for ^{t}DPDX.
8. Burst mode operation is initialized through the bus configuration register (BCR[15]).
9. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single-word burst (as indicated by WAIT).

Part-Numbering Information

Micron CellularRAM devices are available in several different configurations and densities (see Figure 3).

Figure 3: Part Number Chart



Valid Part Number Combinations

After building the part number from the part numbering chart above, visit the Micron Web site at www.micron.com/support/designsupport/tools/fbga/decoder to verify that the part number is offered and valid. If the device required is not on this list, contact the factory.

Device Marking

Due to the size of the package, the Micron standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at www.micron.com/support/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/support/designsupport/documents/csn.

Functional Description

In general, the MT45W4MW16BCGB device is a high-density alternative to SRAM and PSRAM products, popular in low-power, portable applications.

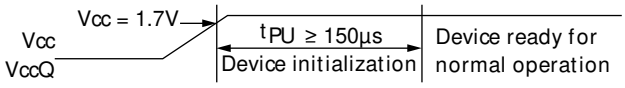
The MT45W4MW16BCGB contains a 67,108,864-bit DRAM core, organized as 4,194,304 addresses by 16 bits. The device implements the same high-speed bus interface found on burst mode Flash products.

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Figure 18 on page 25 and Figure 24 on page 31). VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 4: Power-Up Initialization Timing



Bus Operating Modes

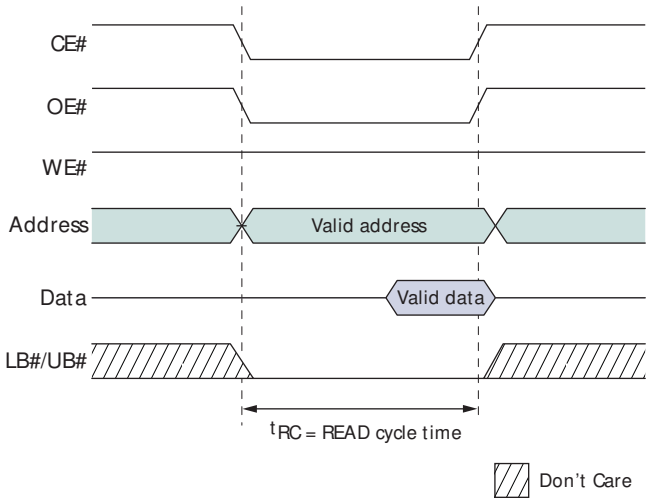
The MT45W4MW16BCGB CellularRAM product incorporates a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 5 on page 12) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 6 on page 12) occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can use the ADV input to latch the address or can drive ADV LOW during the entire READ/WRITE operation.

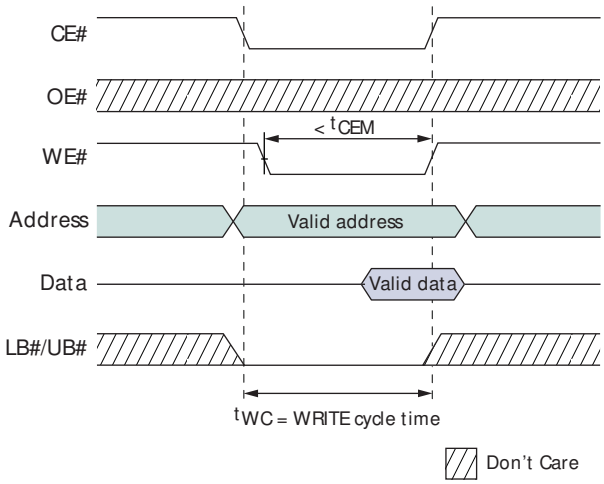
During asynchronous operation, the CLK input must be held static LOW. WAIT will be driven while the device is enabled, and its state should be ignored. WE# LOW time must be limited to ^{t}CEM.

Figure 5: READ Operation (ADV# LOW)



Note: ADV must remain LOW for page mode operation.

Figure 6: WRITE Operation (ADV# LOW)



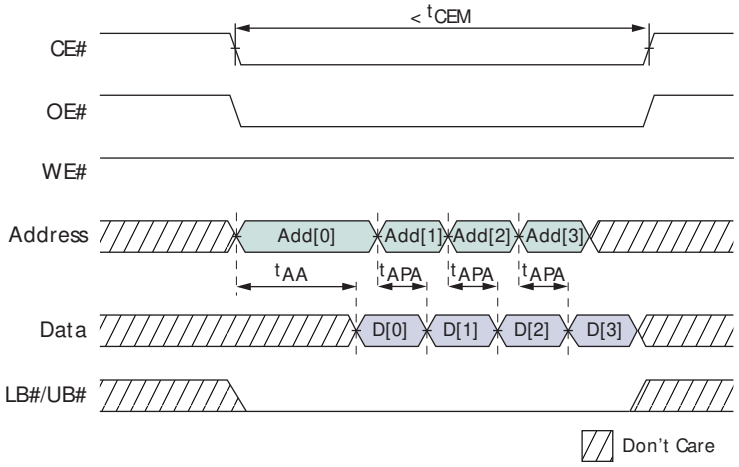
Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, and then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new ^{t}AA access time. Figure 7 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be held LOW. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled, and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. ADV must be driven LOW during all page mode read accesses.

Due to refresh considerations, CE# must not remain LOW longer than ^{t}CEM.

Figure 7: Page Mode READ Operation (ADV# LOW)



Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multiclock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the rising edge of the next clock that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 8 on page 14) or a WRITE (WE# = LOW, Figure 9 on page 15).

The size of a burst can be specified in the BCR either as a fixed-length or continuous. Fixed-length bursts consist of 4, 8, 16, or 32 words. Continuous bursts have the ability to start at a specified address and burst to the end of the 128-word row.

The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and the CellularRAM device. The initial latency for READ operations can be configured as fixed or variable

(WRITE operations always use fixed latency). Variable latency allows the CellularRAM to be configured for minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles.

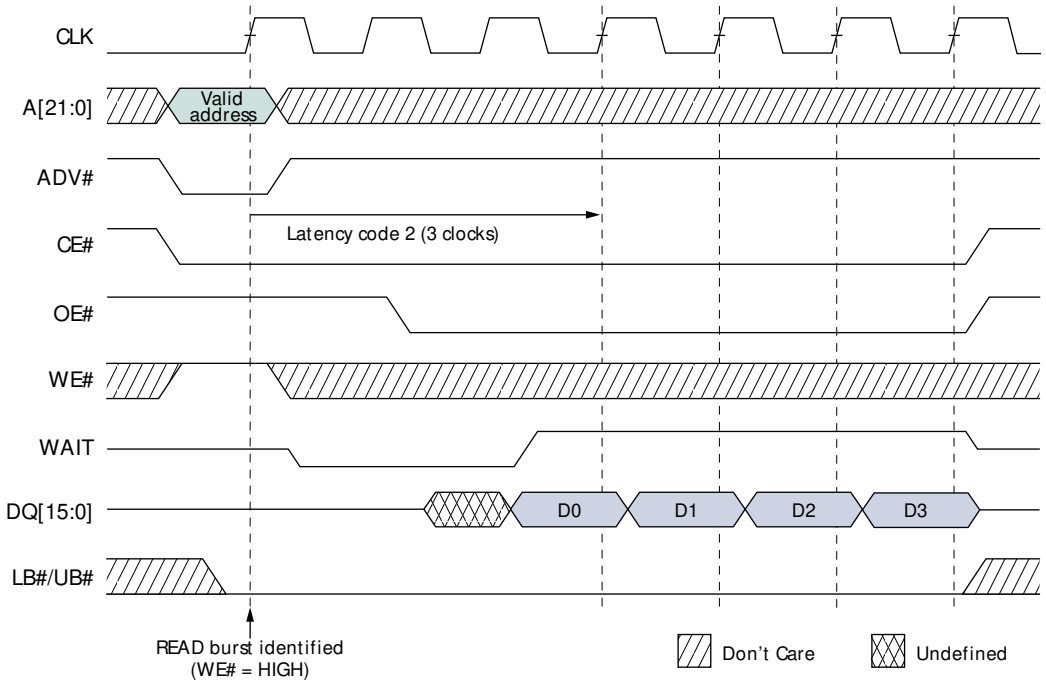
Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting. Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies.

The WAIT output asserts when a burst is initiated and de-asserts to indicate when data is to be transferred into or out of memory. WAIT will again be asserted at the boundary of the 128-word row, unless wrapping within the burst length.

To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be active and, as a result, no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, and then CLK is restarted after valid data is available on the bus.

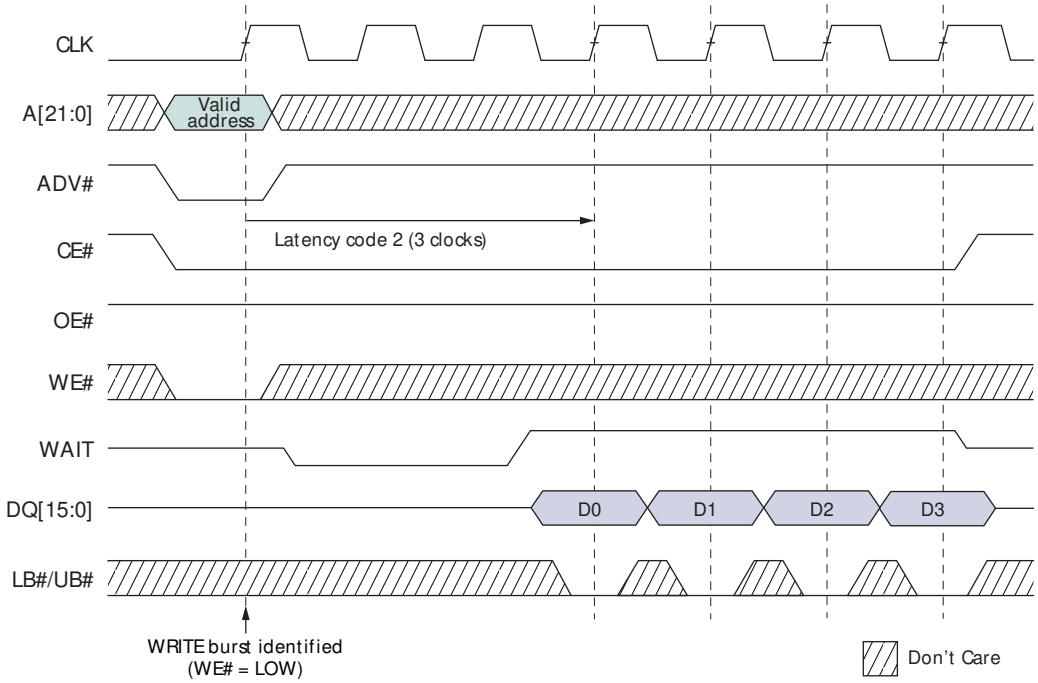
The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than ^{t}CEM. If a burst suspension will cause CE# to remain LOW for longer than ^{t}CEM, CE# should be taken HIGH and the burst should be restarted with a new CE# LOW/ADV# LOW cycle.

Figure 8: Burst Mode READ (4-Word Burst)



Note: Nondefault BCR settings for burst mode READ (4-word burst): fixed or variable latency; latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay. Figure 8 is representative of variable latency with no refresh collision or fixed-latency access.

Figure 9: Burst Mode WRITE (4-Word Burst)



Note: Nondefault BCR settings for burst mode WRITE (4-word burst): fixed or variable latency; latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

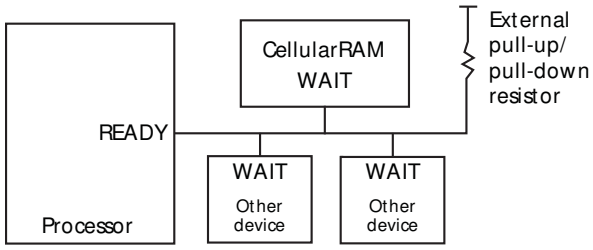
Mixed-Mode Operation

The device supports a combination of synchronous READ and asynchronous READ and WRITE operations when the BCR is configured for synchronous operation. The asynchronous READ and WRITE operations require that the clock (CLK) remain LOW during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# can remain LOW when transitioning between mixed-mode operations with fixed latency enabled; however, the CE# LOW time must not exceed ^{t}CEM. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 50 on page 63 for the "Asynchronous WRITE Followed by Burst READ" timing diagram.

WAIT Operation

The WAIT output on a CellularRAM device typically is connected to a shared, system-level WAIT signal (see Figure 10 on page 16). The shared WAIT signal is used by the processor to coordinate transactions with multiple memory devices on the synchronous bus.

Figure 10: Wired-OR WAIT Configuration



When a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

During a burst cycle, CE# must remain asserted until the first data is valid. Bringing CE# HIGH during this initial latency may cause data corruption.

When variable initial access latency is used (BCR[14] = 0), the WAIT output performs an arbitration role for READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed (see Figure 11 on page 17). When the refresh operation has completed, the READ operation will continue normally.

WAIT will be asserted but should be ignored during asynchronous READ, WRITE, and PROGRAM operations.

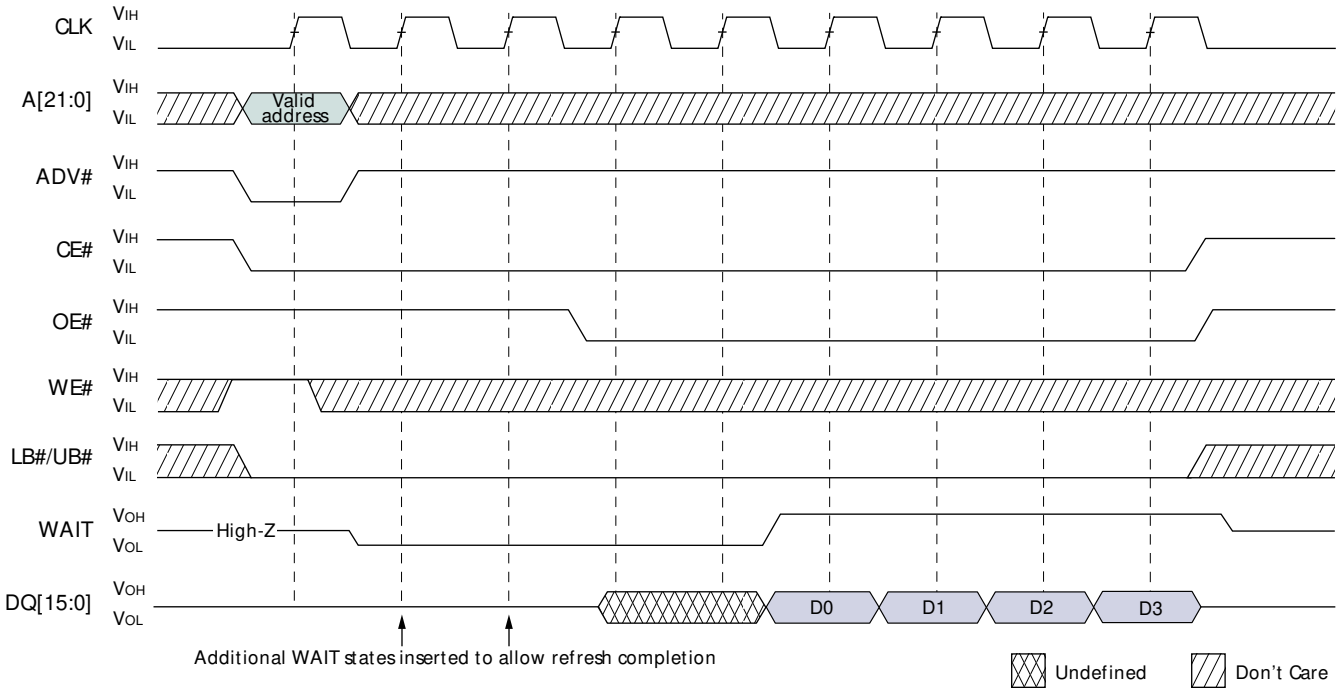
By using fixed initial latency (BCR[14] = 1), this CellularRAM device can be used in burst mode without monitoring the WAIT signal. However, WAIT can still be used to determine when valid data is available at the start of the burst and at the end of a row. If WAIT is not monitored, the controller must stop burst accesses at row boundaries on its own.

LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data WRITEs. During WRITE operations, any disabled bytes will not be transferred to the RAM array, and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first. LB#/UB# must be LOW during READ cycles.

When both LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

Figure 11: Refresh Collision During Variable-Latency READ Operation



Note: Nondefault BCR settings for refresh collision during variable-latency READ operation: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

Low-Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH.

The device will enter a reduced power state upon completion of a READ or WRITE operation or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature-Compensated Refresh

Temperature-compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature.

Partial-Array Refresh

Partial-array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start either at the beginning or the end of the address map (see Table 8 on page 32). READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When reenabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been reenabled by rewriting, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels but considerably lower than the active current specification.

DPD can be enabled by writing to the RCR using CRE or the software access sequence; DPD starts when CE# goes HIGH. DPD is disabled the next time CE# goes LOW and stays LOW for at least 10µs.

Registers

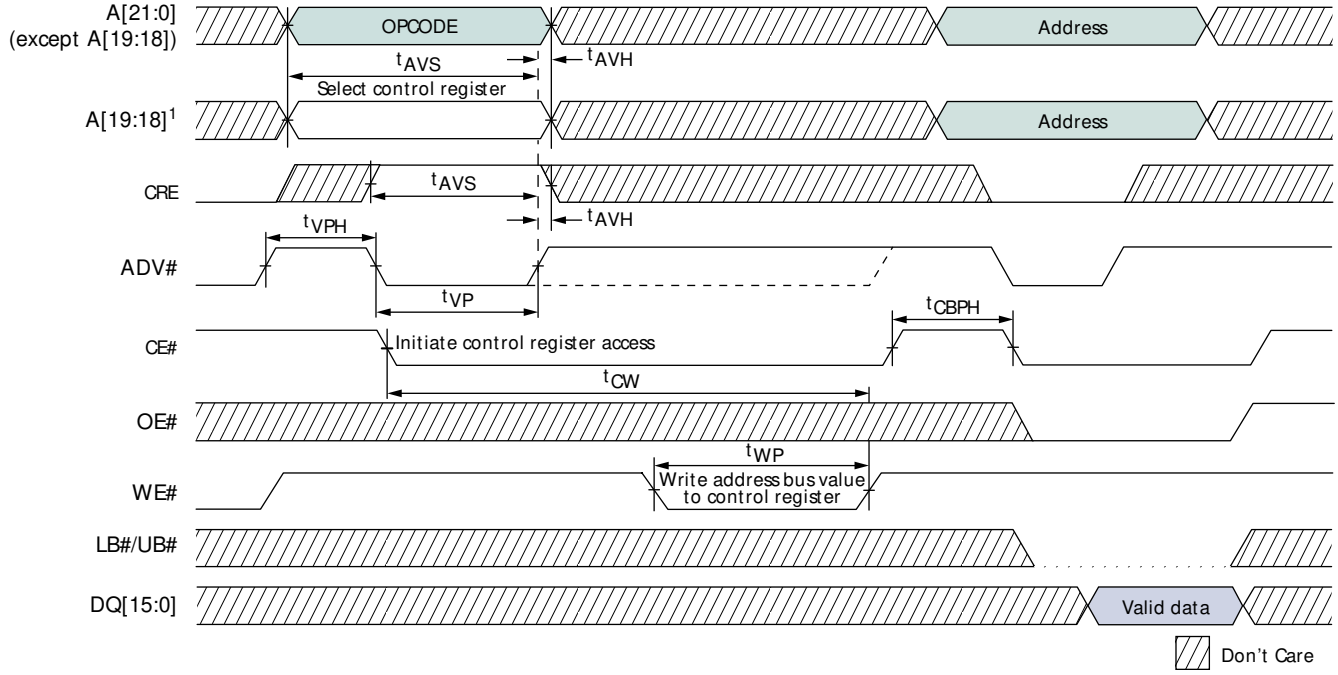
Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated any time the devices are operating in a standby state.

The DIDR provides information on the device manufacturer, the CellularRAM generation, and the specific device configuration. The DIDR is read-only.

Access Using CRE

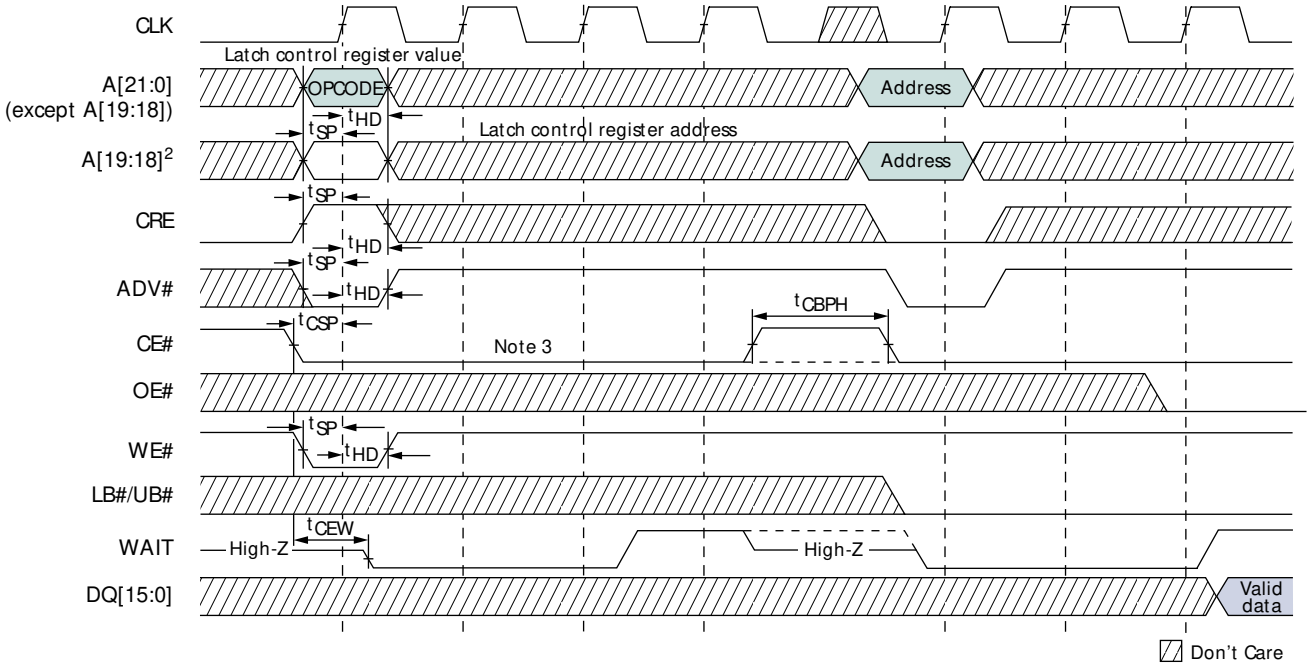
The registers can be accessed either using a synchronous or an asynchronous operation when the control register enable (CRE) input is HIGH (see Figures 12 through 15). When CRE is LOW, a READ or WRITE operation will access the memory array. The configuration register values are written via addresses A[21:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are "Don't Care." The BCR is accessed when A[19:18] are 10b; the RCR is accessed when A[19:18] are 00b. The DIDR is read when A[19:18] are 01b. For reads, address inputs other than A[19:18] are "Don't Care," and register bits 15:0 are output on DQ[15:0]. Micron strongly recommends reading the memory array immediately after performing a configuration register READ and WRITE operation.

Figure 12: Configuration Register WRITE, Asynchronous Mode Followed by READ ARRAY



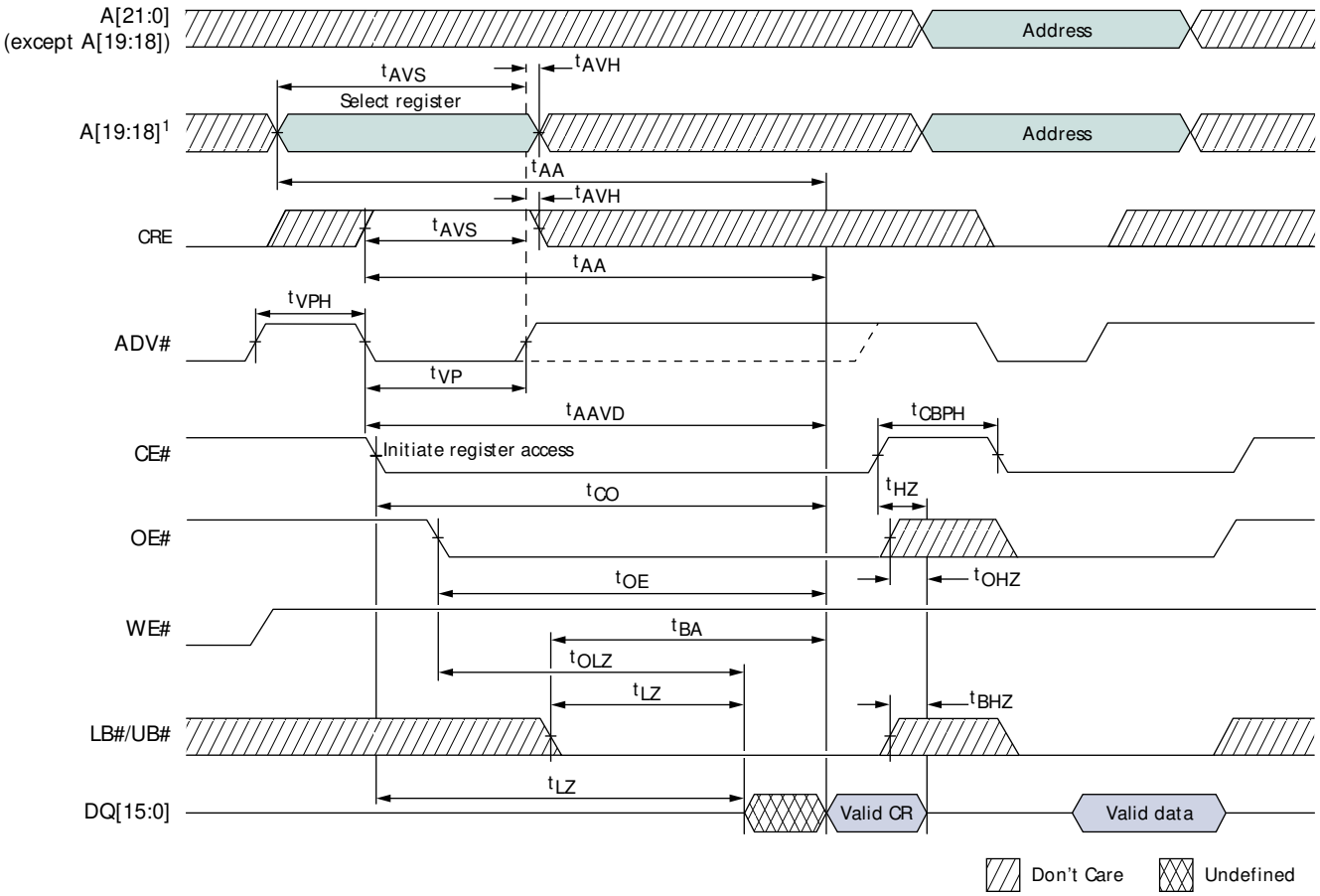
Notes: 1. A[19:18] = 00b to load RCR and A[19:18] = 10b to load BCR.

Figure 13: Configuration Register WRITE, Synchronous Mode Followed by READ ARRAY Operation



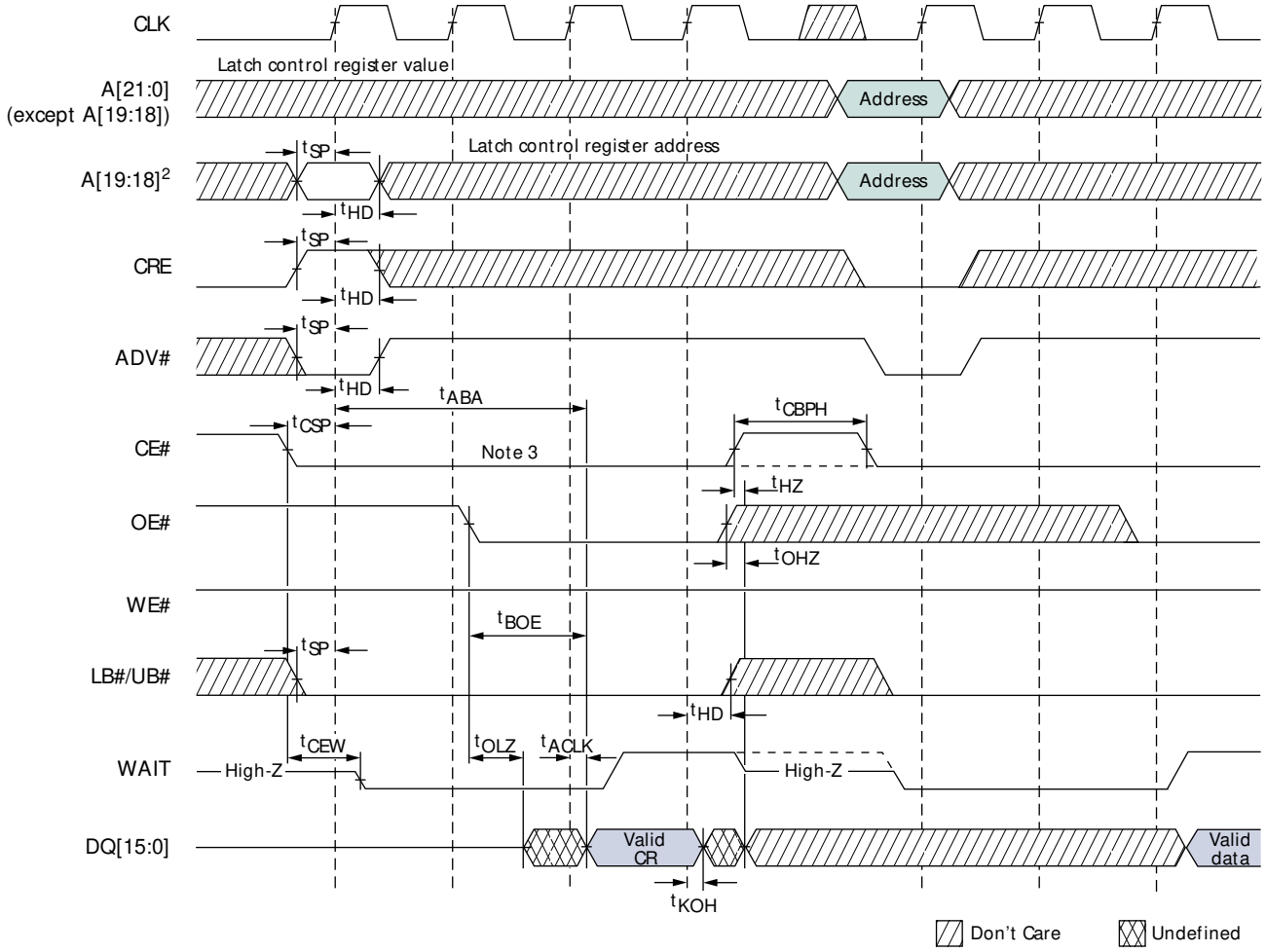
Notes:
1. Nondefault BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19:18] = 00b to load RCR and A[19:18] = 10b to load BCR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Figure 14: Register READ, Asynchronous Mode Followed by READ ARRAY Operation



Notes: 1. A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.

Figure 15: Register READ, Synchronous Mode Followed by READ ARRAY Operation



Notes:
1. Nondefault BCR settings for synchronous mode register READ followed by READ ARRAY operation: latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.
3. CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

Software Access

Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified, and all registers can be read using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 16). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 17 on page 24). The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (3FFFFFh for 64Mb); the contents of this address are not changed by using this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, or the DIDR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR; if the data is 0002h, the sequence will access the DIDR. During the fourth operation, DQ[15:0] transfer data into or out of bits 15:0 of the registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to V_{SS}. The port line often used for CRE control purposes is no longer required.

Figure 16: Load Configuration Register

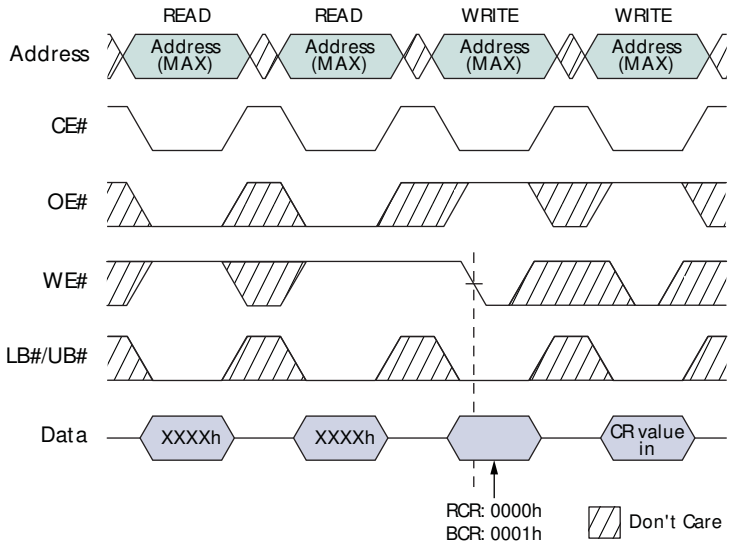
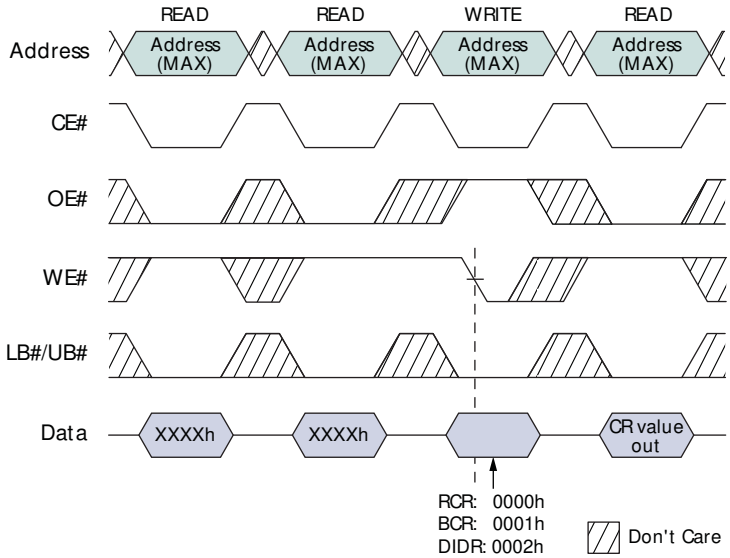


Figure 17: Read Configuration Register

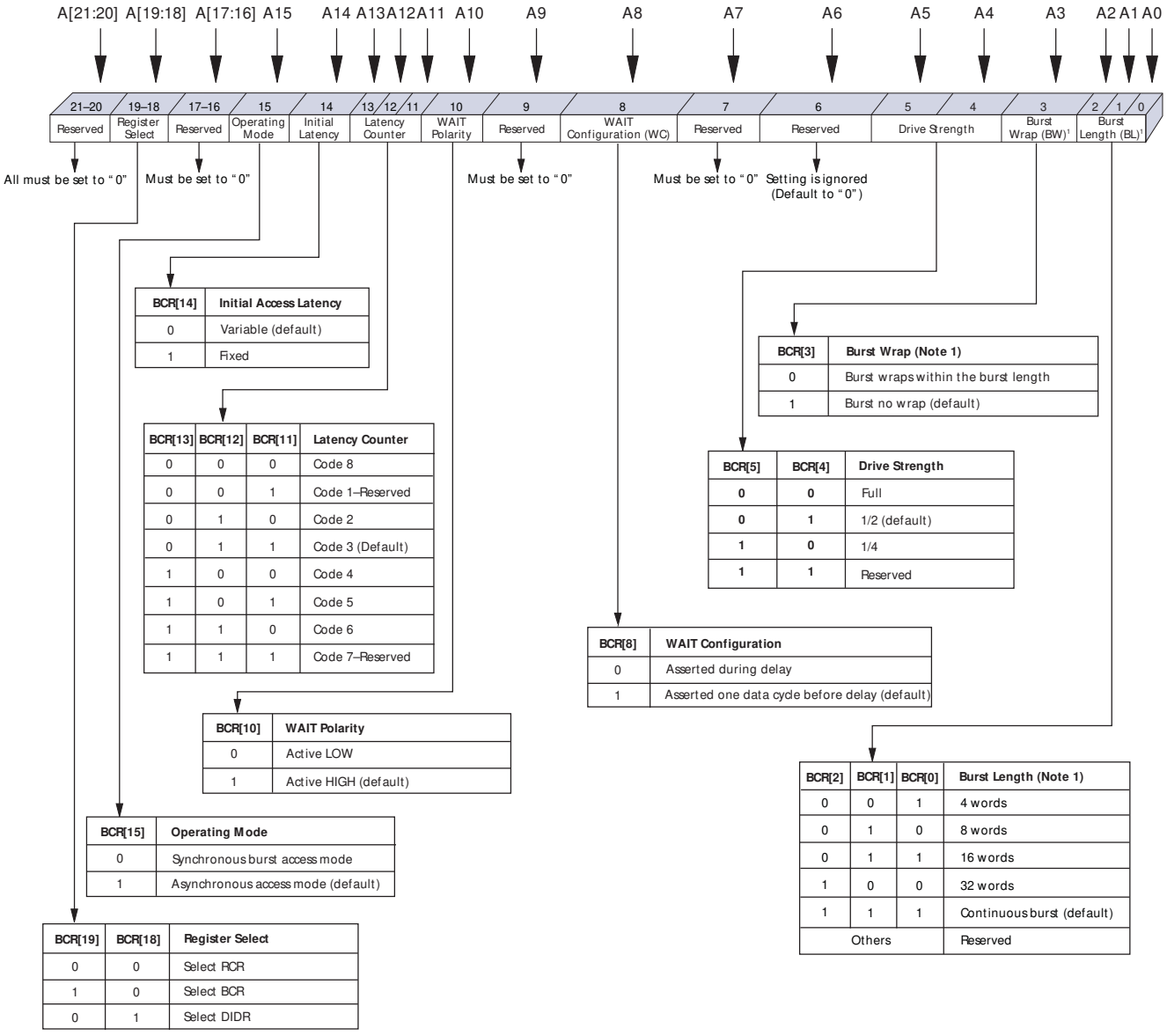


Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Figure 18 defines the control bits in the BCR. At power-up, the BCR is set to 9D1Fh.

The BCR is accessed with CRE HIGH and A[19:18] = 10b or through the register access software sequence with DQ = 0001h on the third cycle.

Figure 18: Bus Configuration Register Definition



BCR[14]	Initial Access Latency
0	Variable (default)
1	Fixed

BCR[13]	BCR[12]	BCR[11]	Latency Counter
0	0	0	Code 8
0	0	1	Code 1–Reserved
0	1	0	Code 2
0	1	1	Code 3 (Default)
1	0	0	Code 4
1	0	1	Code 5
1	1	0	Code 6
1	1	1	Code 7–Reserved

BCR[10]	WAIT Polarity
0	Active LOW
1	Active HIGH (default)

BCR[15]	Operating Mode
0	Synchronous burst access mode
1	Asynchronous access mode (default)

BCR[19]	BCR[18]	Register Select
0	0	Select RCR
1	0	Select BCR
0	1	Select DIDR

BCR[3]	Burst Wrap (Note 1)
0	Burst wraps within the burst length
1	Burst no wrap (default)

BCR[5]	BCR[4]	Drive Strength
0	0	Full
0	1	1/2 (default)
1	0	1/4
1	1	Reserved

BCR[8]	WAIT Configuration
0	Asserted during delay
1	Asserted one data cycle before delay (default)

BCR[2]	BCR[1]	BCR[0]	Burst Length (Note 1)
0	0	1	4 words
0	1	0	8 words
0	1	1	16 words
1	0	0	32 words
1	1	1	Continuous burst (default)
Others			Reserved

Notes: 1. Burst wrap and length apply both to READ and WRITE operations.