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# Async/Page/Burst CellularRAM™ 1.0 Memory

## MT45W4MW16B*

*Note: Not recommended for new designs.

For the latest data sheet, refer to Micron's Web site: http://www.micron.com/products/psram/

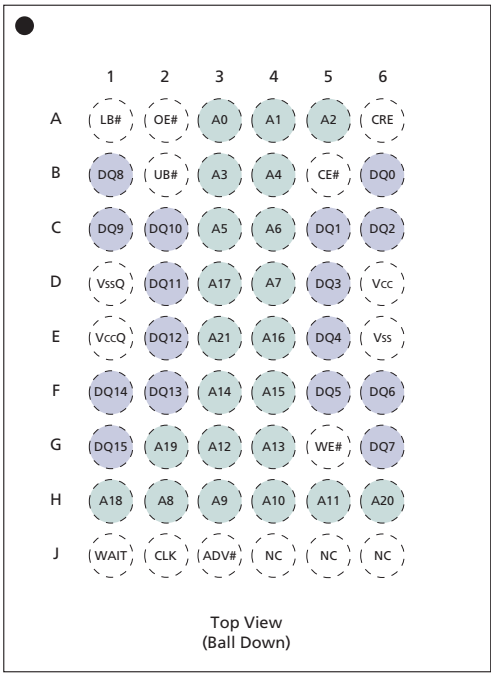
## Features

- Single device supports asynchronous, page, and burst operations
- Random access time: 70ns
- VCC, VCCQ voltages
  1.70V–1.95V VCC
  1.70V–3.30V VCCQ
- Page mode read access
  Sixteen-word page size
  Interpage read access: 70ns
  Intrapage read access: 20ns
- Burst mode write access
  Continuous burst
- Burst mode read access
  4, 8, or 16 words, or continuous burst
  MAX clock rate: 80 MHz ($^{t}$CLK = 12.5ns)
  Burst initial latency: 50ns (4 clocks) @ 80 MHz
  $^{t}$ACLK: 9ns @ 80 MHz
- Low power consumption
  Asynchronous READ: <25mA
  Intrapage READ: <15mA
  Initial access, burst READ:
  (50ns [4 clocks] @ 80 MHz) < 35mA
  Continuous burst READ: <15mA
  Standby: 120µA – standard
  100µA – low-power option
  Deep power-down: <10µA (TYP @ 25°C)
- Low-power features
  Temperature-compensated refresh (TCR)
  Partial-array refresh (PAR)
  Deep power-down (DPD) mode

## Options

| Options | Designator |
|---|---|
| • Configuration: | |
| 4 Meg x 16 | MT45W4MW16B[1] |
| • Package | |
| 54-ball VFBGA (standard) | FB |
| 54-ball VFBGA (lead-free) | BB[2] |
| • Timing | |
| 70ns access | -70 |
| 85ns access | -85 |

**Figure 1: Ball Assignment – 54-Ball VFBGA**




## Options (continued)

| Options (continued) | Designator |
|---|---|
| • Frequency | |
| 66 MHz | 6 |
| 80 MHz | 8 |
| • Standby power | |
| Standard | None |
| Low-power | L |
| • Operating temperature range | |
| Wireless (-30°C to +85°C) | WT[3] |
| Industrial (-40°C to +85°C) | IT[2] |

Notes: 1. Not recommended for new designs.

2. Contact factory.

3. -30°C exceeds the CellularRAM Working Group 1.0 specification of -25°C.

*Part Number Example:*

**MT45W4MW16BFB-708LWT**

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# General Description

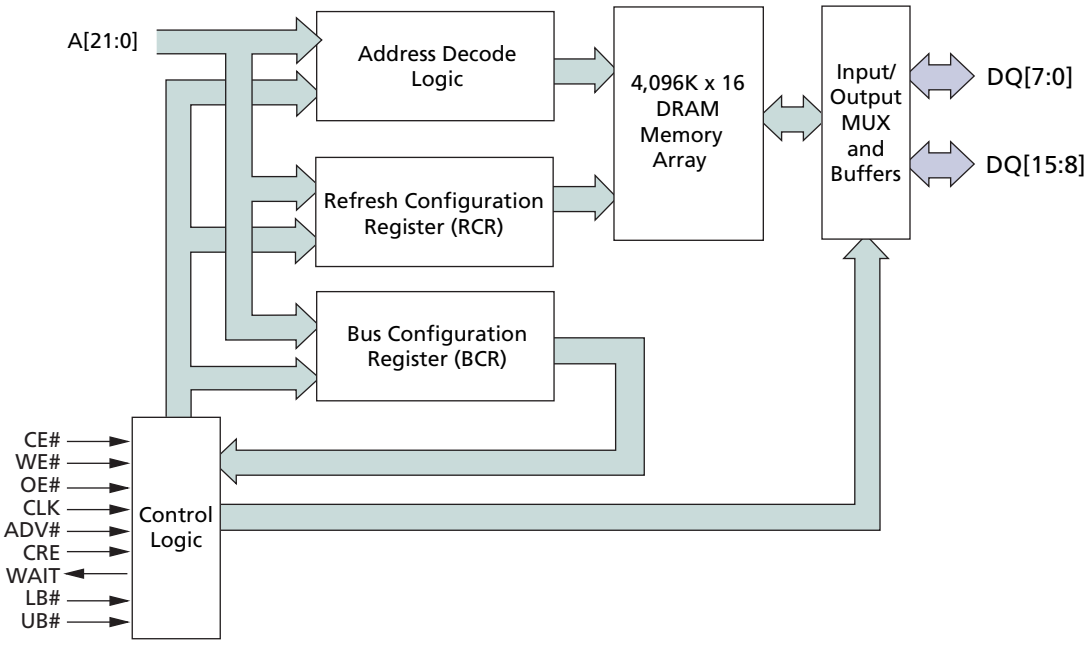
Micron® CellularRAM™ products are high-speed, CMOS PSRAM memories developed for low-power, portable applications. The MT45W4MW16BFB is a 64Mb DRAM core device organized as 4 Meg x 16 bits. This device includes an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three system-accessible mechanisms used to minimize standby current. Partial-array refresh (PAR) limits refresh to only that part of the DRAM array that contains essential data. Temperature-compensated refresh (TCR) is used to adjust the refresh rate according to the case temperature. The refresh rate can be decreased at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) halts the refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the RCR.

**Figure 2: Functional Block Diagram – 4 Meg x 16**




Note: Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.

**Table 1: VFBGA Ball Descriptions**

| VFBGA Assignment | Symbol | Type | Description |
|---|---|---|---|
| E3, H6, G2, H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3 | A[21:0] | Input | Address Inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR. |
| J2 | CLK | Input | Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static (HIGH or LOW) during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations. |
| J3 | ADV# | Input | Address Valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# may be held LOW during asynchronous READ and WRITE operations. |
| A6 | CRE | Input | Control Register Enable: When CRE is HIGH, WRITE operations load the RCR or BCR. |
| B5 | CE# | Input | Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode. |
| A2 | OE# | Input | Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled. |
| G5 | WE# | Input | Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array. |
| A1 | LB# | Input | Lower Byte Enable. DQ[7:0] |
| B2 | UB# | Input | Upper Byte Enable. DQ[15:8] |
| G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6 | DQ[15:0] | Input/ Output | Data Inputs/Outputs. |
| J1 | WAIT | Output | Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is asserted when a burst crosses a row boundary. WAIT is also used to mask the delay associated with opening a new internal page. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH. |
| J4, J5, J6 | NC | – | Not internally connected. |
| D6 | $V_{CC}$ | Supply | Device Power Supply: (1.70V–1.95V) Power supply for device core operation. |
| E1 | $V_{CCQ}$ | Supply | I/O Power Supply: (1.70V–3.30V) Power supply for input/output buffers. |
| E6 | $V_{SS}$ | Supply | $V_{SS}$ must be connected to ground. |
| D1 | $V_{SSQ}$ | Supply | $V_{SSQ}$ must be connected to ground. |

Note: The CLK and ADV# inputs can be tied to $V_{SS}$ if the device is always operating in asynchronous or page mode. WAIT will be asserted but should be ignored during asynchronous and page mode operations.

# Bus Operations

**Table 2: Bus Operations – Asynchronous Mode**

| Mode | Power | CLK[1] | ADV# | CE# | OE# | WE# | CRE | LB#/ UB# | WAIT[2] | DQ[15:0][3] | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | Active | X | L | L | L | H | L | L | Low-Z | Data-Out | 4 |
| Write | Active | X | L | L | X | L | L | L | Low-Z | Data-In | 4 |
| Standby | Standby | X | X | H | X | X | L | X | High-Z | High-Z | 5, 6 |
| No Operation | Idle | X | X | L | X | X | L | X | Low-Z | X | 4, 6 |
| Configuration Register | Active | X | L | L | H | L | H | X | Low-Z | High-Z | |
| DPD | Deep Power-Down | X | X | H | X | X | X | X | High-Z | High-Z | 7 |

**Table 3: Bus Operations – Burst Mode**

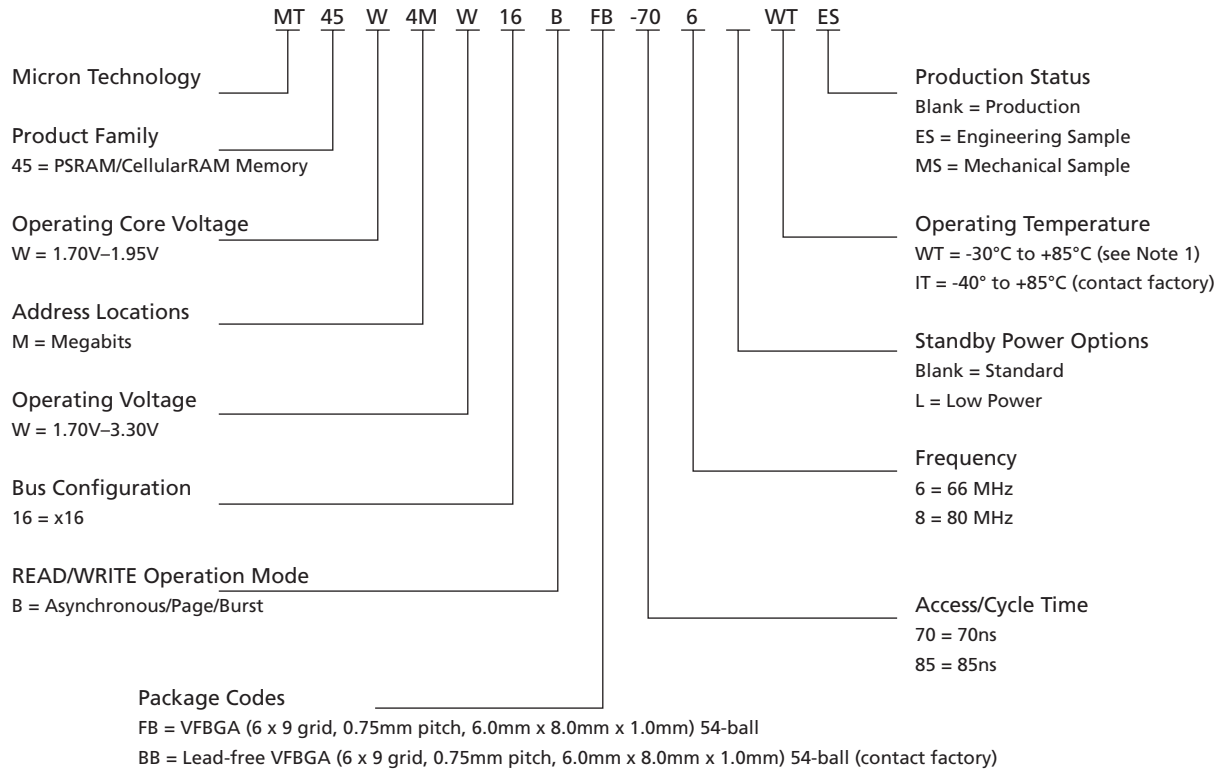
| Mode | Power | CLK[1] | ADV# | CE# | OE# | WE# | CRE | LB#/ UB# | WAIT[2] | DQ[15:0][3] | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Async Read | Active | X | L | L | L | H | L | L | Low-Z | Data-Out | 4 |
| Async Write | Active | X | L | L | X | L | L | L | Low-Z | Data-In | 4 |
| Standby | Standby | X | X | H | X | X | L | X | High-Z | High-Z | 5, 6 |
| No Operation | Idle | X | X | L | X | X | L | X | Low-Z | X | 4, 6 |
| Initial Burst Read | Active |  | L | L | X | H | L | L | Low-Z | Data-Out | 4, 8 |
| Initial Burst Write | Active |  | L | L | H | L | L | X | Low-Z | Data-In | 4, 8 |
| Burst Continue | Active |  | H | L | X | X | X | L | Low-Z | Data-In or Data-Out | 4, 8 |
| Burst Suspend | Active | X | X | L | H | X | L | X | Low-Z | High-Z | 4, 8 |
| Configuration Register | Active |  | L | L | H | L | H | X | Low-Z | High-Z | 8 |
| DPD | Deep Power-Down | X | X | H | X | X | X | X | High-Z | High-Z | 7 |

Notes:
1. CLK may be HIGH or LOW, but must be static, during async read and async write modes and to achieve standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. $V_{IN}$ = $V_{CCQ}$ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
7. DPD is maintained until RCR is reconfigured.
8. Burst mode operation is initialized through the bus configuration register (BCR[15]).

# Part-Numbering Information

Micron CellularRAM devices are available in several different configurations and densities (see Figure 3).

**Figure 3: Part Number Chart**




Note: -30°C exceeds the CellularRAM Working Group 1.0 specification of -25°C.

## Valid Part Number Combinations

After building the part number from the part numbering chart, please go to the Micron Part Marking Decoder Web site at http://www.micron.com/partsearch to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.

## Device Marking

Due to the size of the package, the Micron standard part number is not printed on the top of the device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at http://www.micron.com/partsearch. To view the location of the abbreviated mark on the device, please refer to customer service note, CSN-11, “Product Mark/Label," at http://www.micron.com/csn.

# Functional Description

In general, the MT45W4MW16BFB device is a high-density alternative to SRAM and Pseudo SRAM products, popular in low-power, portable applications.

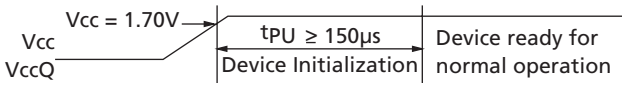
The MT45W4MW16BFB device contains a 67,108,864-bit DRAM core, organized as 4,194,304 addresses by 16 bits. The device implements the same high-speed bus interface found on burst mode Flash products.

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

## Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Table 17 on page 21 and Table 22 on page 26). VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.70V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

**Figure 4: Power-Up Initialization Timing**




# Bus Operating Modes

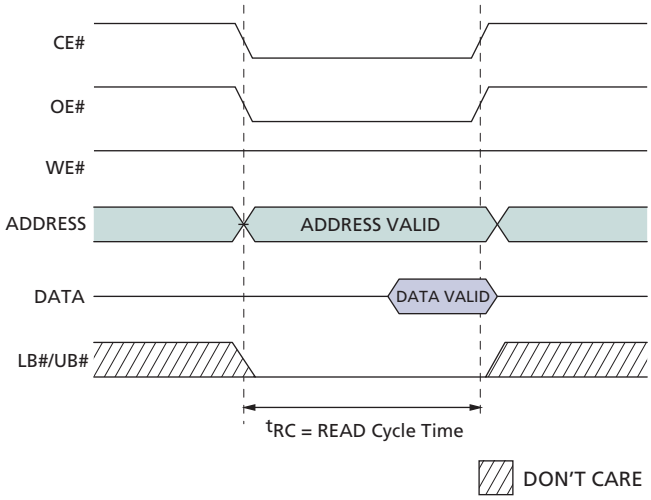
The MT45W4MW16BFB CellularRAM product incorporates a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

## Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 5) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 6) occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven LOW during the entire READ/WRITE operation.

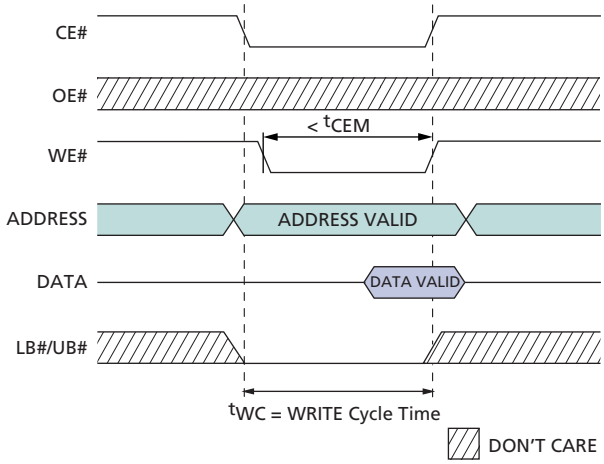
During asynchronous operation, the CLK input must be static (HIGH or LOW—no transitions). WAIT will be driven while the device is enabled and its state should be ignored. WE# LOW time must be limited to $^{t}$CEM.

**Figure 5: READ Operation (ADV = LOW)**




Note: ADV must remain LOW for page mode operation.

**Figure 6: WRITE Operation (ADV = LOW)**



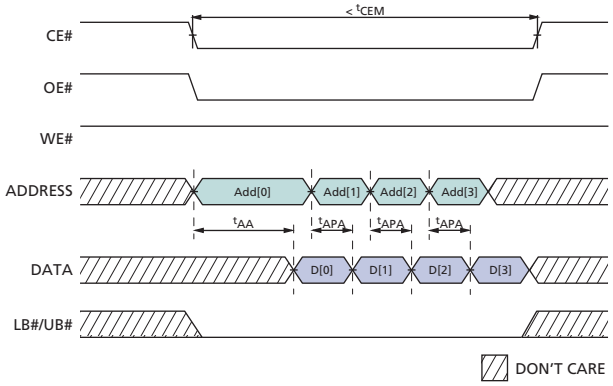

## Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new $^{t}$AA access time. Figure 7 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be static (HIGH or LOW – no transitions). CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. ADV must be driven LOW during all page mode read accesses.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than $^{t}$CEM.

**Figure 7: Page Mode READ Operation (ADV = LOW)**




## Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the next rising edge of CLK that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 8 on page 12) or WRITE (WE# = LOW, Figure 9 on page 12).

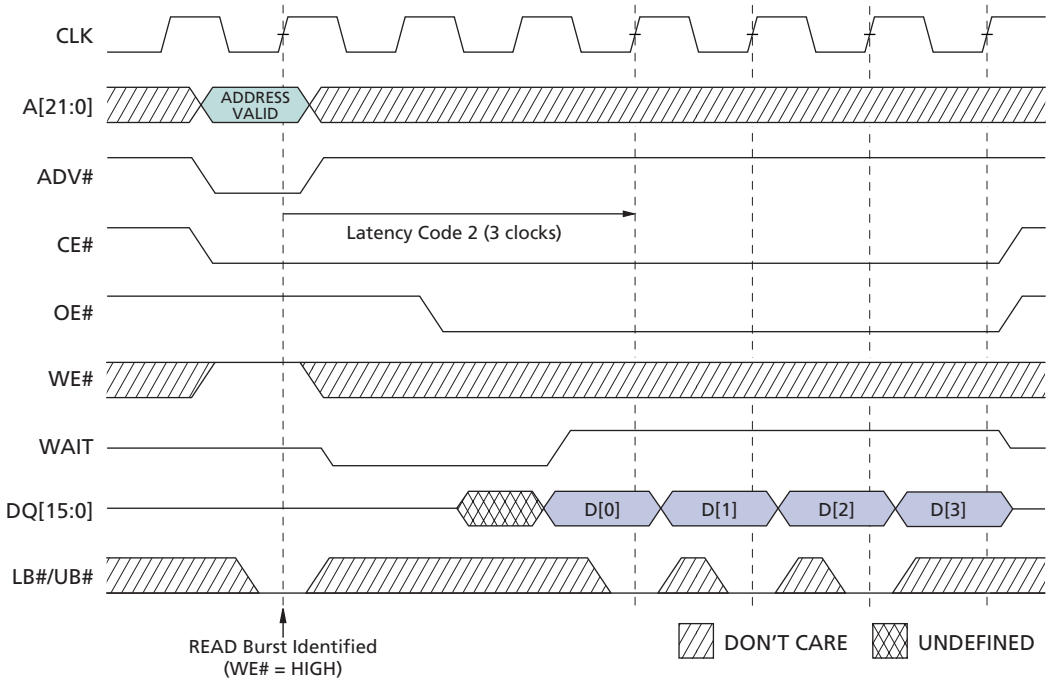
The size of a burst can be specified in the BCR as either fixed-length or continuous. Fixed-length bursts consist of four, eight, or sixteen words. Continuous bursts have the ability to start at a specified address and burst through the entire memory. The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device.

The WAIT output will be asserted as soon as CE# goes LOW and will be de-asserted to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted if the burst crosses the boundary between 128-word rows. Once the CellularRAM device has restored the previous row's data and accessed the next row, WAIT will be de-asserted and the burst can continue (see Figure 34 on page 45).

The processor can access other devices without incurring the timing penalty of the initial latency for a new burst by suspending burst mode. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, then CLK is restarted after valid data is available on the bus.

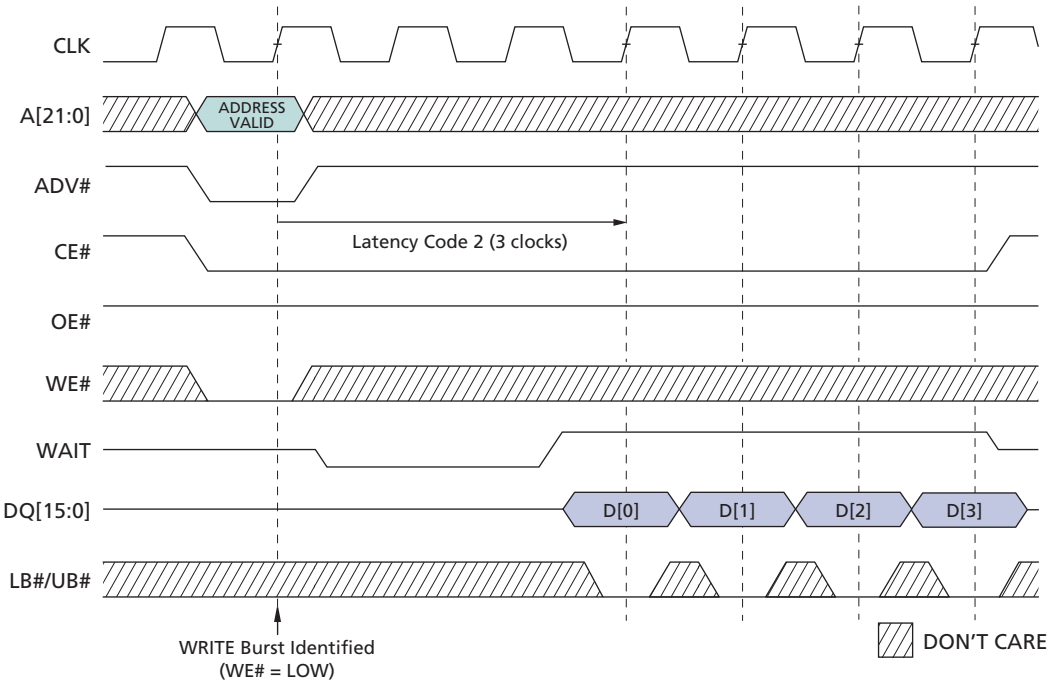
The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than $^{t}$CEM unless row boundaries are crossed at least every $^{t}$CEM. If a burst suspension will cause CE# to remain LOW for longer than $^{t}$CEM, CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

**Figure 8: Burst Mode READ (4-word Burst)**




Note: Non-default BCR settings for burst mode READ (4-word burst): Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

**Figure 9: Burst Mode WRITE (4-word Burst)**




Note: Non-default BCR settings for burst mode WRITE (4-word burst): Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

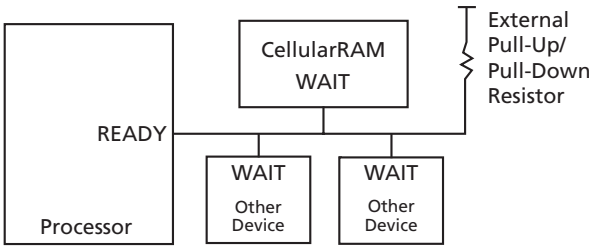
## Mixed-Mode Operation

The device can support a combination of synchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. The asynchronous READ and WRITE operations require that the clock (CLK) remain static (HIGH or LOW) during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# must return HIGH when transitioning between mixed-mode operations. Note that the $^{t}$CKA period is the same as a READ or WRITE cycle. This time is required to ensure adequate refresh. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 42 on page 53 for the "Asynchronous WRITE Followed by Burst READ" timing diagram.

## WAIT Operation

The WAIT output on a CellularRAM device is typically connected to a shared, system-level WAIT signal (see Figure 10). The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

**Figure 10: Wired or WAIT Configuration**




Once a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

CE# must remain asserted during WAIT cycles (WAIT asserted and WAIT configuration BCR[8] = 1). Bringing CE# HIGH during WAIT cycles may cause data corruption. (Note that for BCR[8] = 0, the actual WAIT cycles end one cycle after WAIT de-asserts, and for row boundary crossings, start one cycle after the WAIT signal asserts.)

The WAIT output also performs an arbitration role when a READ or WRITE operation is launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed (see Figures 11 and 12 on page 15). When the REFRESH operation has completed, the READ or WRITE operation will continue normally.

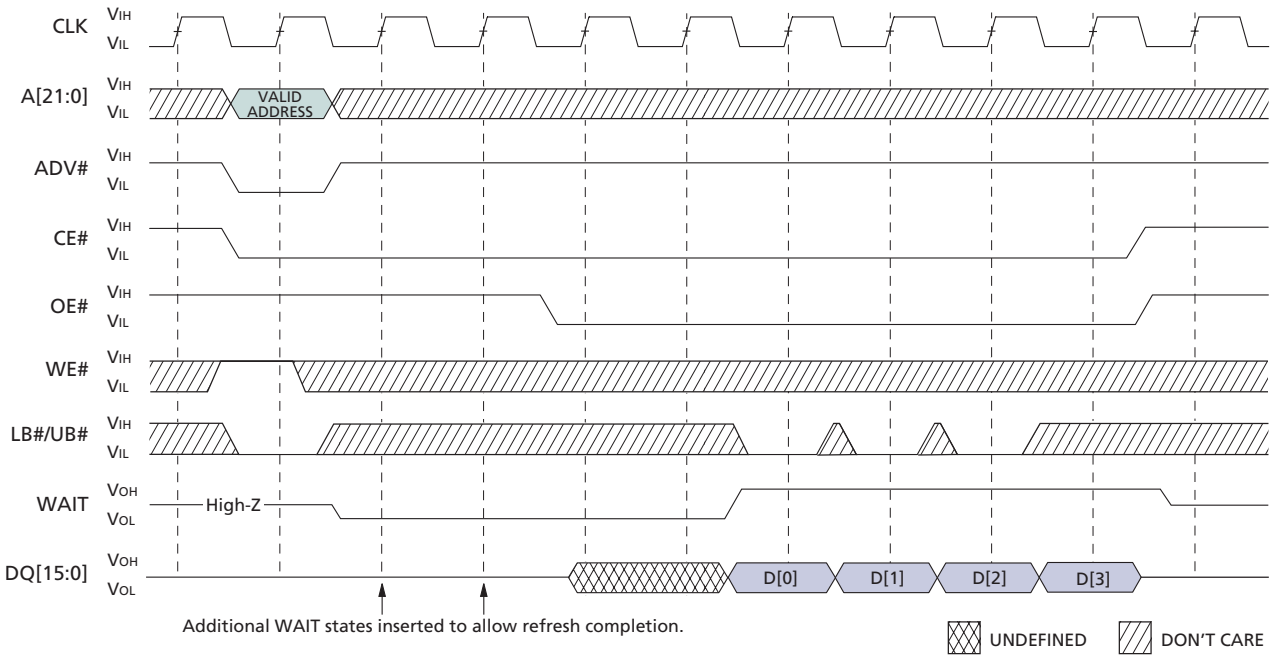
WAIT is also asserted when a continuous READ or WRITE burst crosses a row boundary. The WAIT assertion allows time for the new row to be accessed, and permits any pending REFRESH operations to be performed.

## LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data transfers. During READ operations, the enabled byte(s) are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

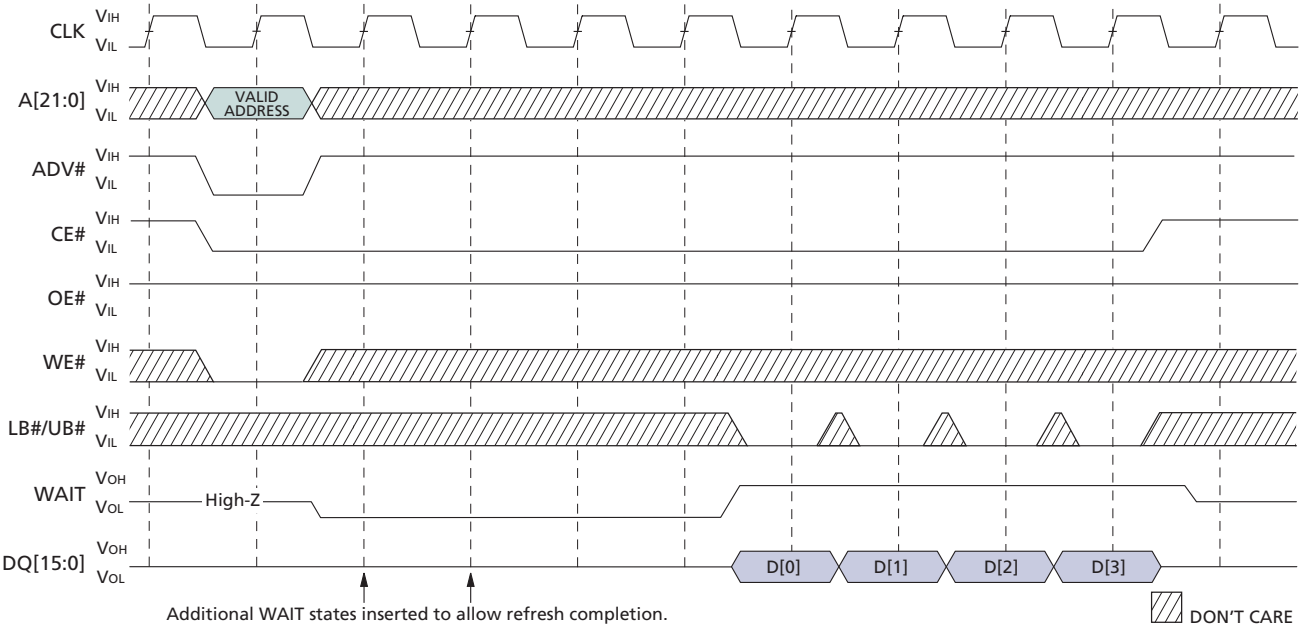
When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

**Figure 11: Refresh Collision During READ Operation**




Note: Non-default BCR settings for refresh collision during READ operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

**Figure 12: Refresh Collision During WRITE Operation**




Note: Non-default BCR settings for refresh collision during WRITE operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

# Low-Power Operation

## Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH.

The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

## Temperature-Compensated Refresh

Temperature-compensated refresh (TCR) is used to adjust the refresh rate depending on the device operating temperature. DRAM technology requires increasingly frequent REFRESH operations to maintain data integrity as temperatures increase. More frequent refresh is required due to increased leakage of the DRAM capacitive storage elements as temperatures rise. A decreased refresh rate at lower temperatures will facilitate a savings in standby current.

TCR allows for adequate refresh at four different temperature thresholds (+15°C, +45°C, +70°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. For example, if the case temperature is +50°C, the system can minimize self refresh current consumption by selecting the +70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

## Partial-Array Refresh

Partial-array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 6 on page 27). READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

## Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled by rewriting the RCR, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

DPD cannot be enabled or disabled by writing to the RCR using the software access sequence; the RCR should be accessed using CRE instead.

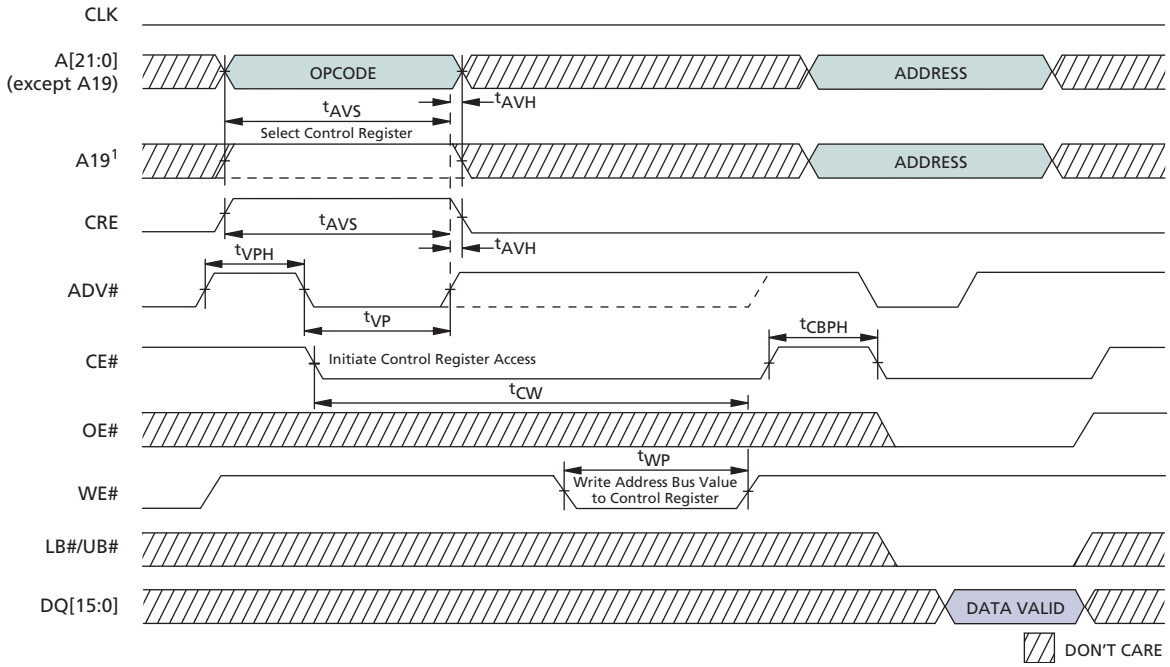
# Configuration Registers

Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

## Access Using CRE

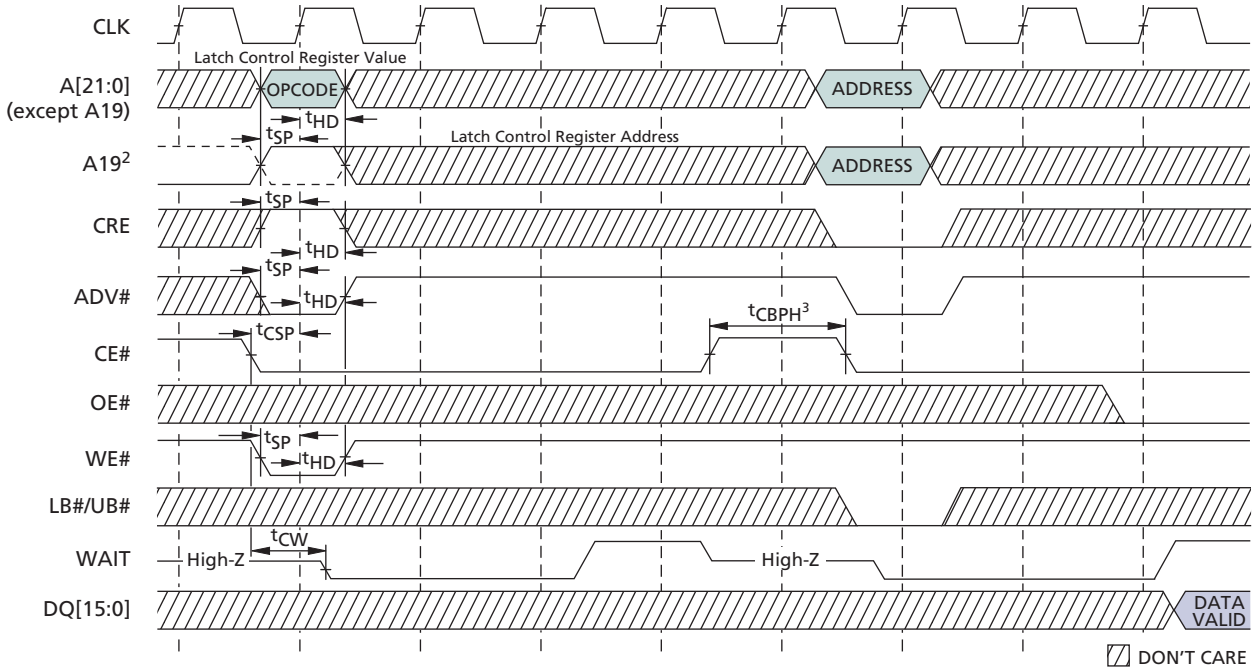
The configuration registers are loaded using either a synchronous or an asynchronous WRITE operation when the control register enable (CRE) input is HIGH (see Figure 13 below and Figure 14 on page 18). When CRE is LOW, a READ or WRITE operation will access the memory array. The register values are placed on addresses A[21:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are "Don't Care." Access using CRE is WRITE only. The BCR is accessed when A[19] is HIGH; the RCR is accessed when A[19] is LOW.

**Figure 13: Configuration Register WRITE in Asynchronous Mode Followed by READ ARRAY Operation**




Note: A[19] = LOW to load RCR; A[19] = HIGH to load BCR.

**Figure 14: Configuration Register WRITE in Synchronous Mode Followed by READ ARRAY Operation**




Notes: 1. Non-default BCR settings for configuration register WRITE in synchronous mode followed by READ ARRAY operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19] = LOW to load RCR; A[19] = HIGH to load BCR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

## Software Access

Software access of the configuration registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be read or modified using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 15). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 16 on page 20). Note that a third READ cycle of the highest address cancels the access sequence until a different address is read.

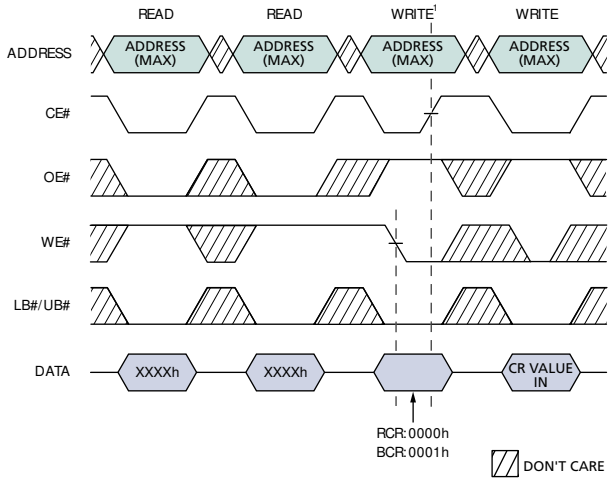
The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (3FFFFFh for 64Mb); the content at this address is changed by using this sequence (note that this is a deviation from the CellularRAM specification).

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR or the RCR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR. During the fourth operation, DQ[15:0] is used to transfer data into or out of bits 15–0 of the configuration registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for the control register enable (CRE) ball. If the software mechanism is used, the CRE ball can simply be tied to $V_{SS}$. The port line often used for CRE control purposes is no longer required.

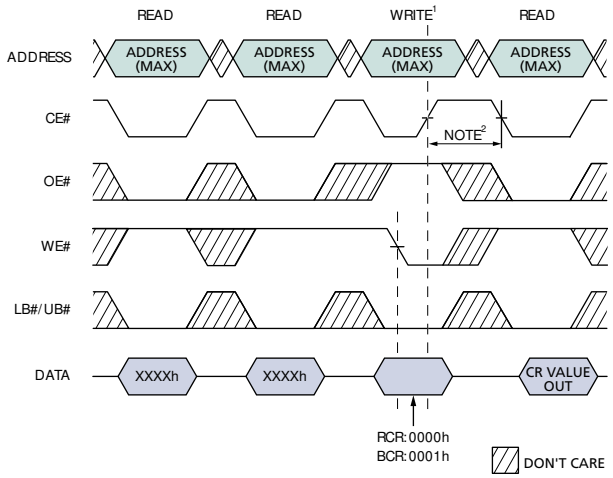
Software access of the RCR should not be used to enter or exit DPD.

**Figure 15: Load Configuration Register**




Note: The WRITE on the third cycle must be CE#-controlled.

**Figure 16: Read Configuration Register**



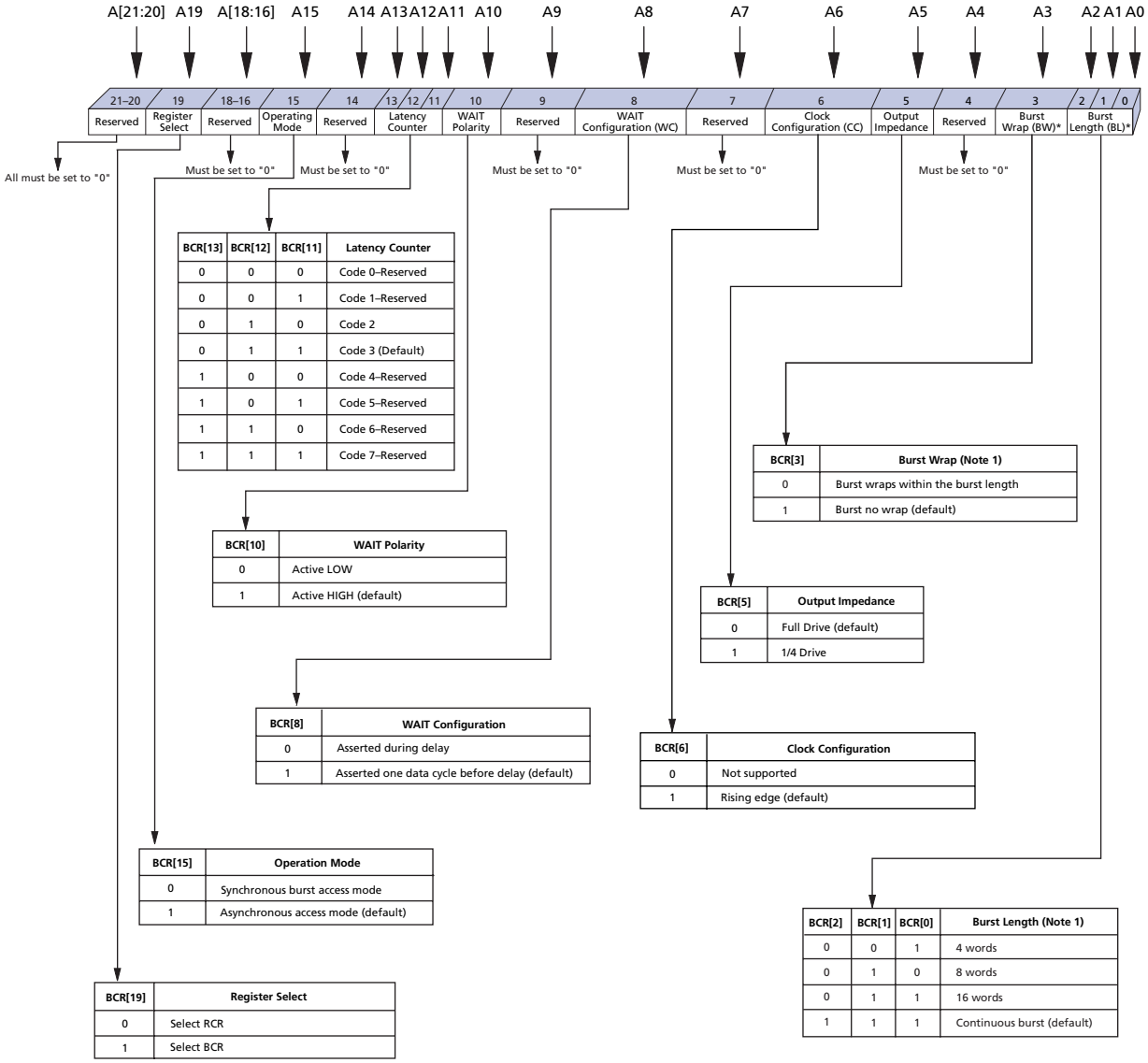

Notes: 1. The WRITE on the third cycle must be CE#-controlled.
2. CE# must be HIGH for 150ns before performing the cycle that reads a configuration register.

## Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Figure 17 describes the control bits in the BCR. At power-up, the BCR is set to 9D4Fh.

The BCR is accessed using CRE and A[19] HIGH, or through the configuration register software sequence with DQ = 0001h on the third cycle.

**Figure 17: Bus Configuration Register Definition**




| BCR[13] | BCR[12] | BCR[11] | Latency Counter |
|---|---|---|---|
| 0 | 0 | 0 | Code 0–Reserved |
| 0 | 0 | 1 | Code 1–Reserved |
| 0 | 1 | 0 | Code 2 |
| 0 | 1 | 1 | Code 3 (Default) |
| 1 | 0 | 0 | Code 4–Reserved |
| 1 | 0 | 1 | Code 5–Reserved |
| 1 | 1 | 0 | Code 6–Reserved |
| 1 | 1 | 1 | Code 7–Reserved |

| BCR[10] | WAIT Polarity |
|---|---|
| 0 | Active LOW |
| 1 | Active HIGH (default) |

| BCR[8] | WAIT Configuration |
|---|---|
| 0 | Asserted during delay |
| 1 | Asserted one data cycle before delay (default) |

| BCR[15] | Operation Mode |
|---|---|
| 0 | Synchronous burst access mode |
| 1 | Asynchronous access mode (default) |

| BCR[19] | Register Select |
|---|---|
| 0 | Select RCR |
| 1 | Select BCR |

| BCR[3] | Burst Wrap (Note 1) |
|---|---|
| 0 | Burst wraps within the burst length |
| 1 | Burst no wrap (default) |

| BCR[5] | Output Impedance |
|---|---|
| 0 | Full Drive (default) |
| 1 | 1/4 Drive |

| BCR[6] | Clock Configuration |
|---|---|
| 0 | Not supported |
| 1 | Rising edge (default) |

| BCR[2] | BCR[1] | BCR[0] | Burst Length (Note 1) |
|---|---|---|---|
| 0 | 0 | 1 | 4 words |
| 0 | 1 | 0 | 8 words |
| 0 | 1 | 1 | 16 words |
| 1 | 1 | 1 | Continuous burst (default) |

Note: All burst WRITEs are continuous.

**Table 4: Sequence and Burst Length**

| Burst Wrap | | Starting Address | 4-Word Burst Length | 8-Word Burst Length | 16-Word Burst Length | Continuous Burst |
|---|---|---|---|---|---|---|
| BCR[3] | Wrap | (Decimal) | Linear | Linear | Linear | Linear |
| 0 | Yes | 0 | 0-1-2-3 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15 | 0-1-2-3-4-5-6-… |
| | | 1 | 1-2-3-0 | 1-2-3-4-5-6-7-0 | 1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0 | 1-2-3-4-5-6-7-… |
| | | 2 | 2-3-0-1 | 2-3-4-5-6-7-0-1 | 2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1 | 2-3-4-5-6-7-8-… |
| | | 3 | 3-0-1-2 | 3-4-5-6-7-0-1-2 | 3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2 | 3-4-5-6-7-8-9-… |
| | | 4 | | 4-5-6-7-0-1-2-3 | 4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3 | 4-5-6-7-8-9-10-… |
| | | 5 | | 5-6-7-0-1-2-3-4 | 5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4 | 5-6-7-8-9-10-11-… |
| | | 6 | | 6-7-0-1-2-3-4-5 | 6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5 | 6-7-8-9-10-11-12- |
| | | 7 | | 7-0-1-2-3-4-5-6 | 7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6 | 7-8-9-10-11-12-13-… |
| | | … | | | … | … |
| | | 14 | | | 14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13 | 14-15-16-17-18-19-20-… |
| | | 15 | | | 15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14 | 15-16-17-18-19-20-21… |
| 1 | No | 0 | 0-1-2-3 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15 | 0-1-2-3-4-5-6-… |
| | | 1 | 1-2-3-4 | 1-2-3-4-5-6-7-8 | 1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16 | 1-2-3-4-5-6-7-… |
| | | 2 | 2-3-4-5 | 2-3-4-5-6-7-8-9 | 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17 | 2-3-4-5-6-7-8-… |
| | | 3 | 3-4-5-6 | 3-4-5-6-7-8-9-10 | 3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18 | 3-4-5-6-7-8-9-… |
| | | 4 | | 4-5-6-7-8-9-10-11 | 4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19 | 4-5-6-7-8-9-10-… |
| | | 5 | | 5-6-7-8-9-10-11-12 | 5-6-7-8-9-10-11-12-13-…-15-16-17-18-19-20 | 5-6-7-8-9-10-11… |
| | | 6 | | 6-7-8-9-10-11-12-13 | 6-7-8-9-10-11-12-13-14-…-16-17-18-19-20-21 | 6-7-8-9-10-11-12… |
| | | 7 | | 7-8-9-10-11-12-13-14 | 7-8-9-10-11-12-13-14-…-17-18-19-20-21-22 | 7-8-9-10-11-12-13… |
| | | … | | | … | … |
| | | 14 | | | 14-15-16-17-18-19-…-23-24-25-26-27-28-29 | 14-15-16-17-18-19-20-… |
| | | 15 | | | 15-16-17-18-19-20-…-24-25-26-27-28-29-30 | 15-16-17-18-19-20-21-… |

### Burst Length (BCR[2:0]) Default = Continuous Burst

Burst lengths define the number of words the device outputs during a burst READ operation. The device supports a burst length of 4, 8, or 16 words. The device can also be set in continuous burst mode where data is output sequentially without regard to address boundaries; the internal address wraps to 000000h if the device is read past the last address. WRITE bursts are always performed using continuous burst mode.

### Burst Wrap (BCR[3]) Default = Burst No Wrap

The burst wrap option determines if a 4-, 8-, or 16-word burst READ wraps within the burst length, or steps through sequential addresses. If the wrap option is not enabled, the device outputs data from sequential addresses without regard to burst boundaries; the internal address wraps to 000000h if the device is read past the last address.

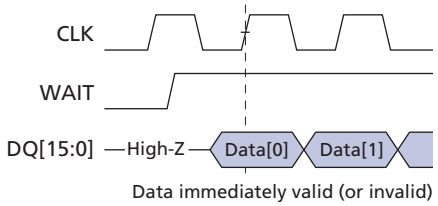
### Output Impedance (BCR[5]) Default = Outputs Use Full Drive Strength

The output driver strength can be altered to adjust for different data bus loading scenarios. The reduced-strength option will be more than adequate in stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option is included to minimize noise generated on the data bus during READ operations. Normal output impedance should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Partial drive is approximately one-quarter full drive strength. Outputs are configured at full drive strength during testing.

### WAIT Configuration (BCR[8]) Default = WAIT Transitions One Clock Before Data Valid/Invalid

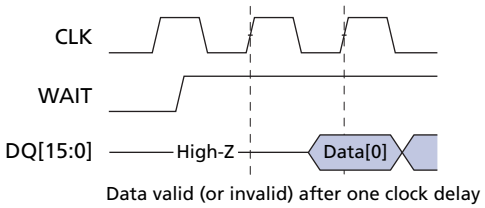
The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively (see Figure 18 and Figure 20). When A8 = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid (see Figure 19 and Figure 20).

**Figure 18: WAIT Configuration (BCR[8] = 0)**



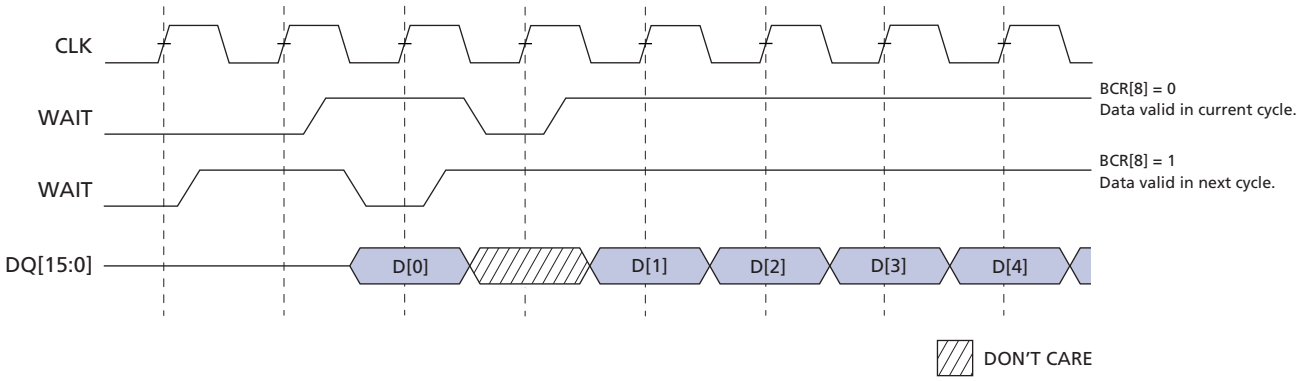

Note: Note: Data valid/invalid immediately after WAIT transitions (BCR[8] = 0). See Figure 20 on page 24.

**Figure 19: WAIT Configuration (BCR[8] = 1)**




Note: Note: Valid/invalid data delayed for one clock after WAIT transitions (BCR[8] = 1). See Figure 20 on page 24.

**Figure 20: WAIT Configuration During Burst Operation**




Note: Non-default BCR setting for WAIT configuration during burst operation: WAIT active LOW.

### WAIT Polarity (BCR[10]) Default = WAIT Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

### Latency Counter (BCR[13:11]) Default = Three-Clock Latency

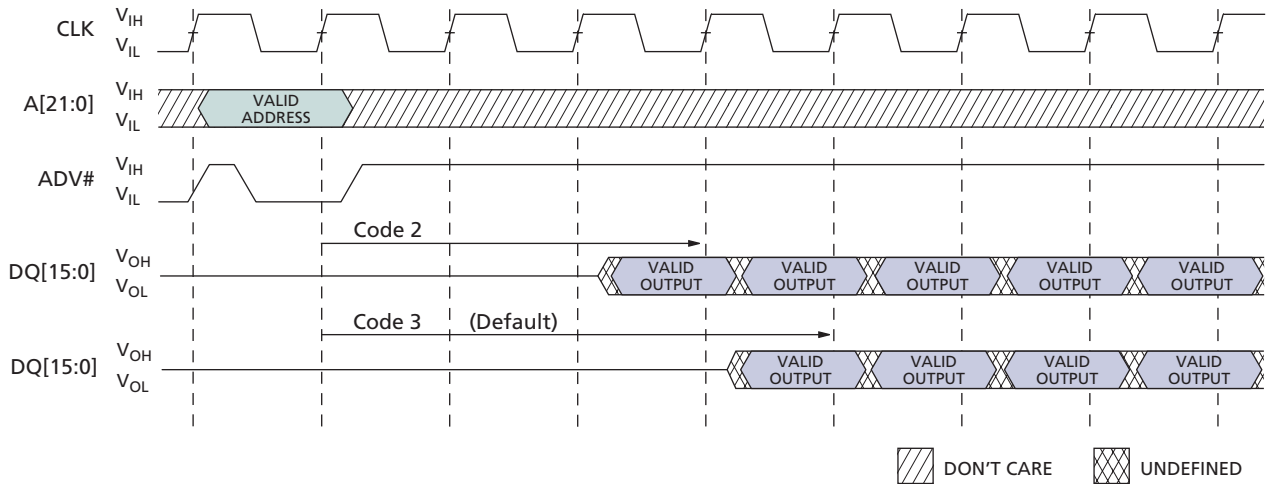
The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. Only latency code two (three clocks) or latency code three (four clocks) is allowed (see Table 5 and Figure 21)

**Table 5: Latency Configuration**

| Latency Configuration Code | Max Input CLK Frequency (MHz) | |
|---|---|---|
| | -708 | -706/-856 |
| 2 (3 clocks) | 53 (18.75ns) | 44[1] (22.7ns) |
| 3 (4 clocks) – default | 80 (12.50ns) | 66 (15.20ns) |

Notes: 1. Clock rates below 50 MHz are allowed as long as $^{t}$CSP specifications are met.

**Figure 21: Latency Counter**



### Operating Mode (BCR[15]) Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.