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Automotive LPDDR SDRAM

MT46H128M16LF – 32 Meg x 16 x 4 Banks
MT46H64M32LF – 16 Meg x 32 x 4 Banks

Features

- V_{DD}/V_{DDQ} = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- 4 internal banks for concurrent operation
- Data masks (DM) for masking write data; one mask per byte
- Programmable burst lengths (BL): 2, 4, 8, or 16
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- Temperature-compensated self refresh (TCSR)[2]
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Status read register (SRR)
- Selectable output drive strength (DS)
- Clock stop capability
- 64ms refresh; 32ms for the automotive temperature range

Options / Mark

Options	Mark
• V_{DD}/V_{DDQ}	
– 1.8V/1.8V	H
• Configuration	
– 128 Meg x 16 (32 Meg x 16 x 4 banks)	128M16
– 64 Meg x 32 (16 Meg x 32 x 4 banks)	64M32
• Addressing	
– JEDEC-standard	LF
• Plastic "green" package	
– 60-ball VFBGA (8mm x 9mm)	DD
– 90-ball VFBGA (8mm x 13mm)	BQ
• Timing – cycle time	
– 4.8ns @ CL = 3 (208 MHz)	-48
• Special Options	
– Automotive (package-level burn-in)	A
• Operating temperature range	
– From –40˚C to +85˚C	IT
– From –40˚C to +105˚C[1]	AT
• Design revision	:C

Notes: 1. Contact factory for availability.
2. Self refresh supported up to 85 °C.

Table 1: Key Timing Parameters (CL = 3)

Speed Grade	Clock Rate	Access Time
-48	208 MHz	4.8ns

Table 2: Configuration Addressing – 2Gb

Architecture	128 Meg x 16	64 Meg x 32
Configuration	32 Meg x 16 x 4 banks	16 Meg x 32 x 4 banks
Refresh count	8K	8K
Row addressing	16K A[13:0]	16K A[13:0]
Column addressing	2K A11, A[9:0]	1K A[9:0]

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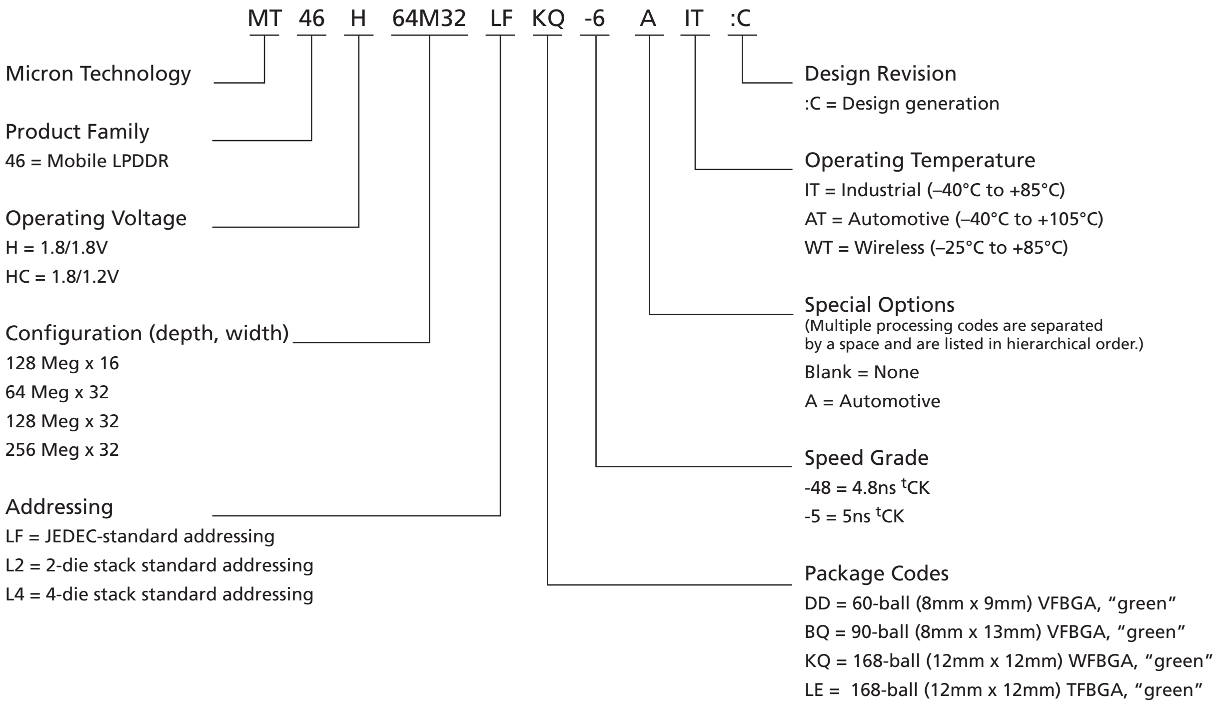
See Package Block Diagrams for descriptions of signal connections and die configurations for each respective architecture.

Figure 1: 2Gb Mobile LPDDR Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

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Contents

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List of Figures

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List of Tables

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General Description

The 2Gb Mobile low-power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 2,147,483,648 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

Note:

1. Throughout this data sheet, various figures and text refer to DQs as "DQ." DQ should be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]), DM refers to UDM and DQS refers to UDQS. The x32 is divided into 4 bytes. For DQ[7:0], DM refers to DM0 and DQS refers to DQS0. For DQ[15:8], DM refers to DM1 and DQS refers to DQS1. For DQ[23:16], DM refers to DM2 and DQS refers to DQS2. For DQ[31:24], DM refers to DM3 and DQS refers to DQS3.

2. Complete functionality is described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

3. Any specific requirement takes precedence over a general statement.

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Functional Block Diagrams

Figure 2: Functional Block Diagram (x16)

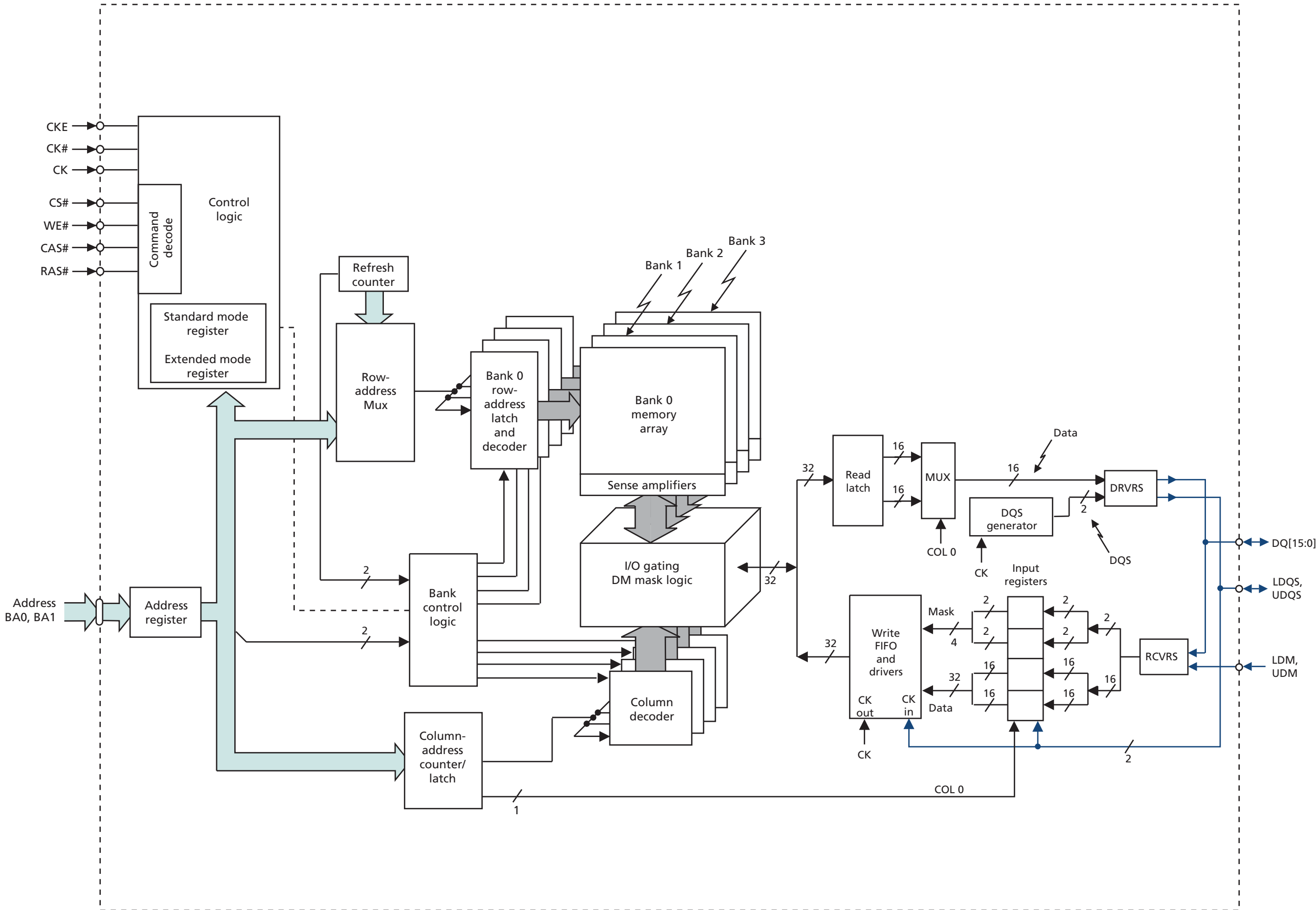

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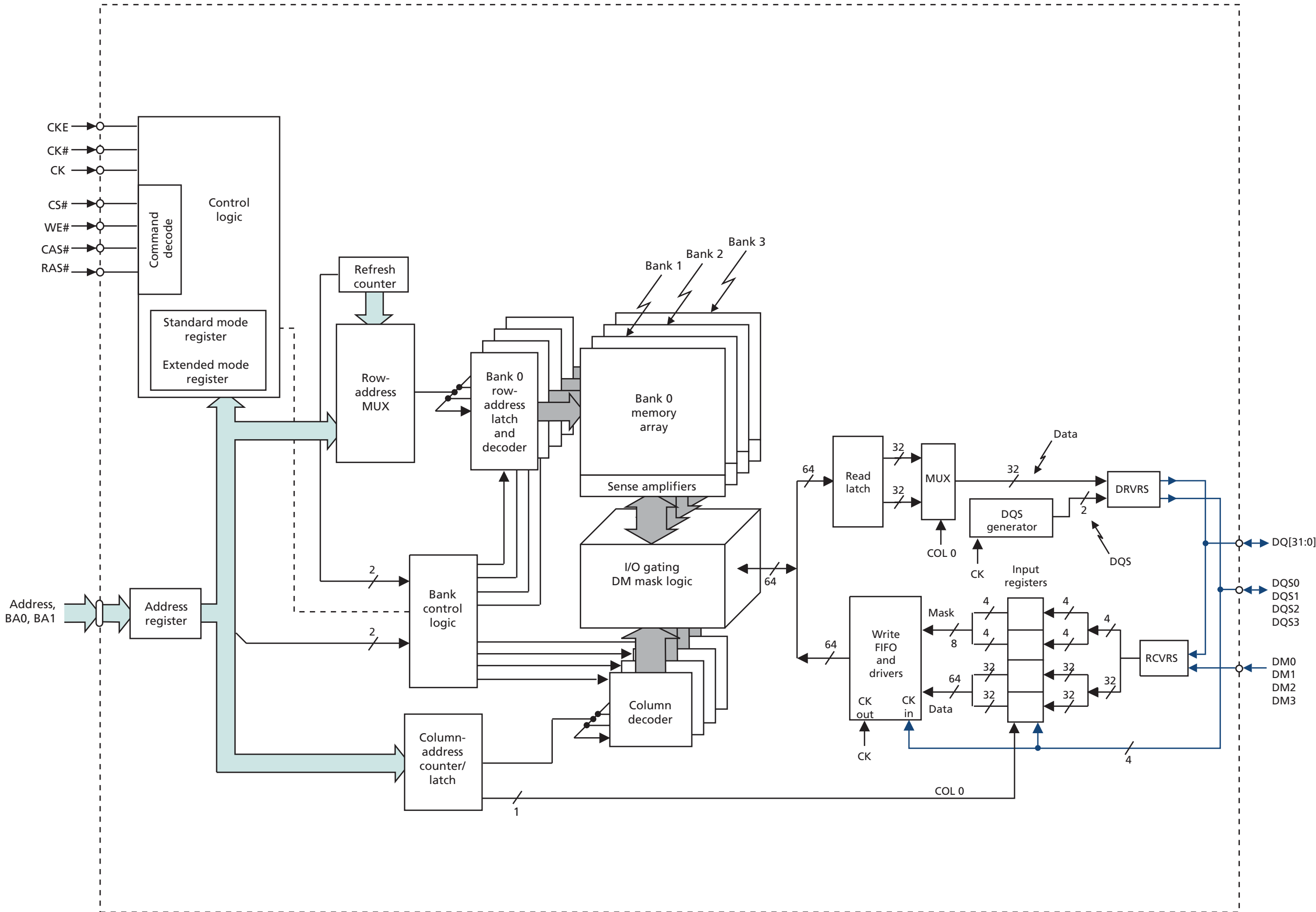
Figure 3: Functional Block Diagram (x32)



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Ball Assignments

Figure 4: 60-Ball VFBGA – Top View, x16 only

	1	2	3	4	5	6	7	8	9
A	V_{SS}	DQ15	V_{SSQ}				V_{DDQ}	DQ0	V_{DD}
B	V_{DDQ}	DQ13	DQ14				DQ1	DQ2	V_{SSQ}
C	V_{SSQ}	DQ11	DQ12				DQ3	DQ4	V_{DDQ}
D	V_{DDQ}	DQ9	DQ10				DQ5	DQ6	TEST[1]
E	V_{SSQ}	UDQS	DQ8				DQ7	LDQS	V_{DDQ}
F	V_{SS}	UDM	NC				A13	LDM	V_{DD}
G	CKE	CK	CK#				WE#	CAS#	RAS#
H	A9	A11	A12				CS#	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	V_{SS}	A4	A5				A2	A3	V_{DD}

Notes:
1. D9 is a test pin that must be tied to V_{SS} or V_{SSQ} in normal operations.
2. Unused address pins become RFU.

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Figure 5: 90-Ball VFBGA – Top View, x32 only

	1	2	3	4	5	6	7	8	9
A	V_{SS}	DQ31	V_{SSQ}				V_{DDQ}	DQ16	V_{DD}
B	V_{DDQ}	DQ29	DQ30				DQ17	DQ18	V_{SSQ}
C	V_{SSQ}	DQ27	DQ28				DQ19	DQ20	V_{DDQ}
D	V_{DDQ}	DQ25	DQ26				DQ21	DQ22	TEST[1]
E	V_{SSQ}	DQS3	DQ24				DQ23	DQS2	V_{DDQ}
F	V_{DD}	DM3	NC				A13	DM2	V_{SS}
G	CKE	CK	CK#				WE#	CAS#	RAS#
H	A9	A11	A12				CS#	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	A4	DM1	A5				A2	DM0	A3
L	V_{SSQ}	DQS1	DQ8				DQ7	DQS0	V_{DDQ}
M	V_{DDQ}	DQ9	DQ10				DQ5	DQ6	V_{SSQ}
N	V_{SSQ}	DQ11	DQ12				DQ3	DQ4	V_{DDQ}
P	V_{DDQ}	DQ13	DQ14				DQ1	DQ2	V_{SSQ}
R	V_{SS}	DQ15	V_{SSQ}				V_{DDQ}	DQ0	V_{DD}

Notes:
1. D9 is a test pin that must be tied to V_{SS} or V_{SSQ} in normal operations.
2. Unused address pins become RFU.

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Ball Descriptions

The ball descriptions table is a comprehensive list of all possible balls for all supported packages. Not all balls listed are supported for a given package.

Table 3: Ball Descriptions

Symbol	Type	Description
CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
CKE CKE0, CKE1	Input	Clock enable: CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes. CKE0 is used for a single LPDDR product. CKE1 is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
CS# CS0#, CS1#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. CS0# is used for a single LPDDR product. CS1# is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
UDM, LDM (x16) DM[3:0] (x32)	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls.
BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is loaded during a LOAD MODE REGISTER command.
A[13:0]	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. The maximum address range is dependent upon configuration. Unused address balls become RFU.
TEST	Input	Test pin: Must be tied to V_{SS} or V_{SSQ} in normal operations.
DQ[15:0] (x16) DQ[31:0] (x32)	Input/ output	Data input/output: Data bus for x16 and x32.
LDQS, UDQS (x16) DQS[3:0] (x32)	Input/ output	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned in write data. It is used to capture data.
TQ	Output	Temperature sensor output: TQ HIGH when LPDDR T_J exceeds 85°C.
V_{DDQ}	Supply	DQ power supply.

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Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
V_{SSQ}	Supply	DQ ground.
V_{DD}	Supply	Power supply.
V_{SS}	Supply	Ground.
NC	–	No connect: May be left unconnected.
RFU	–	Reserved for future use. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

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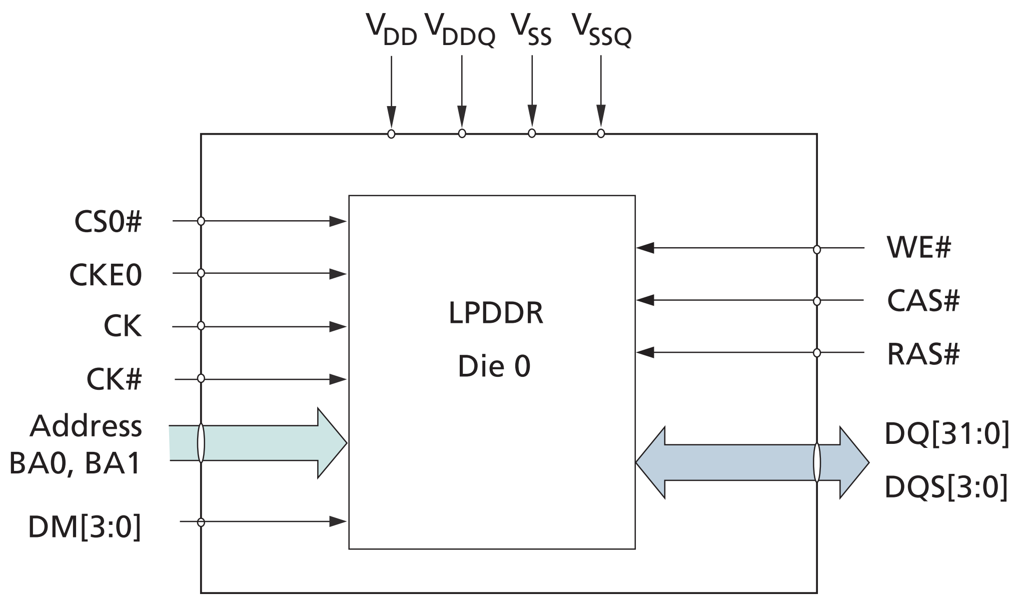
Package Block Diagrams

Figure 6: Single Rank, Single Channel (1 Die) Package Block Diagram



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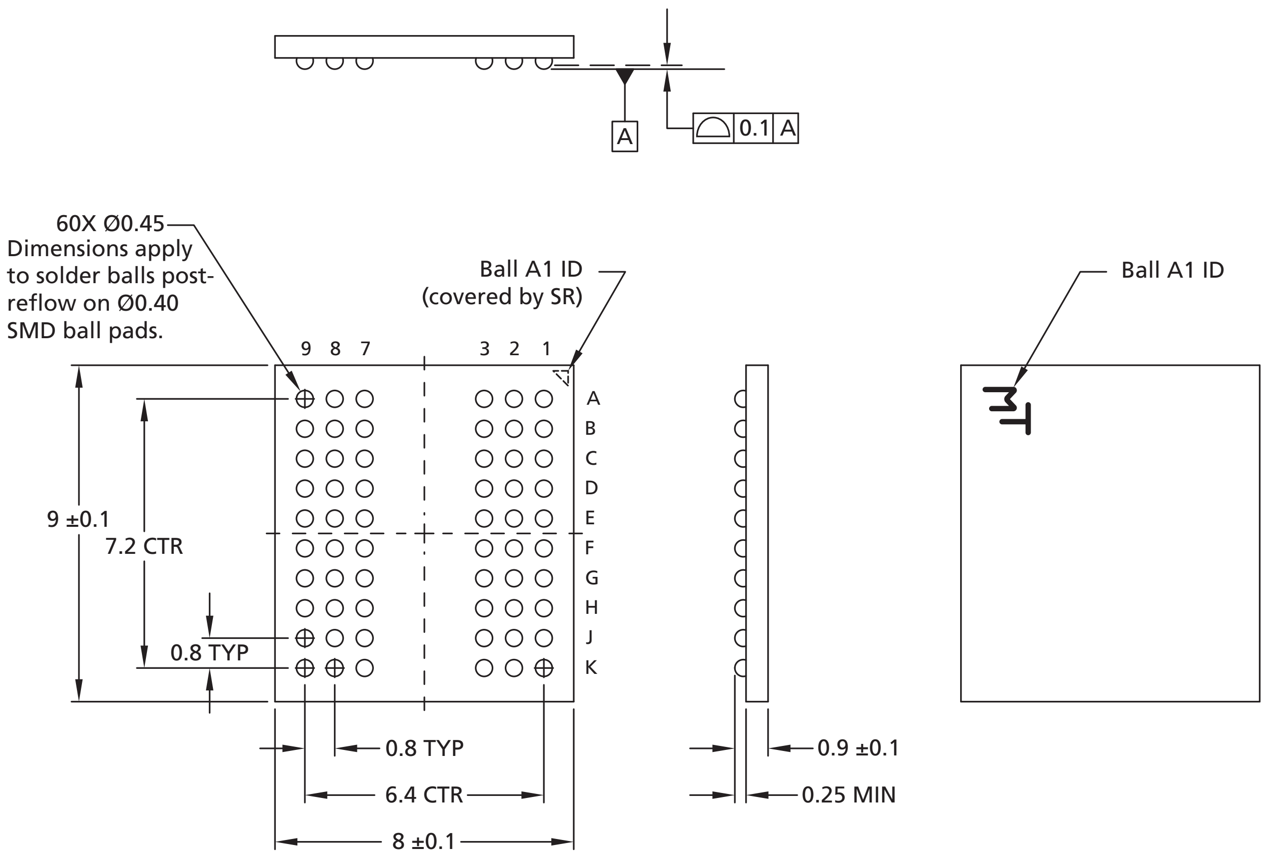
Package Dimensions

Figure 7: 60-Ball VFBGA (8mm x 9mm), Package Code: DD



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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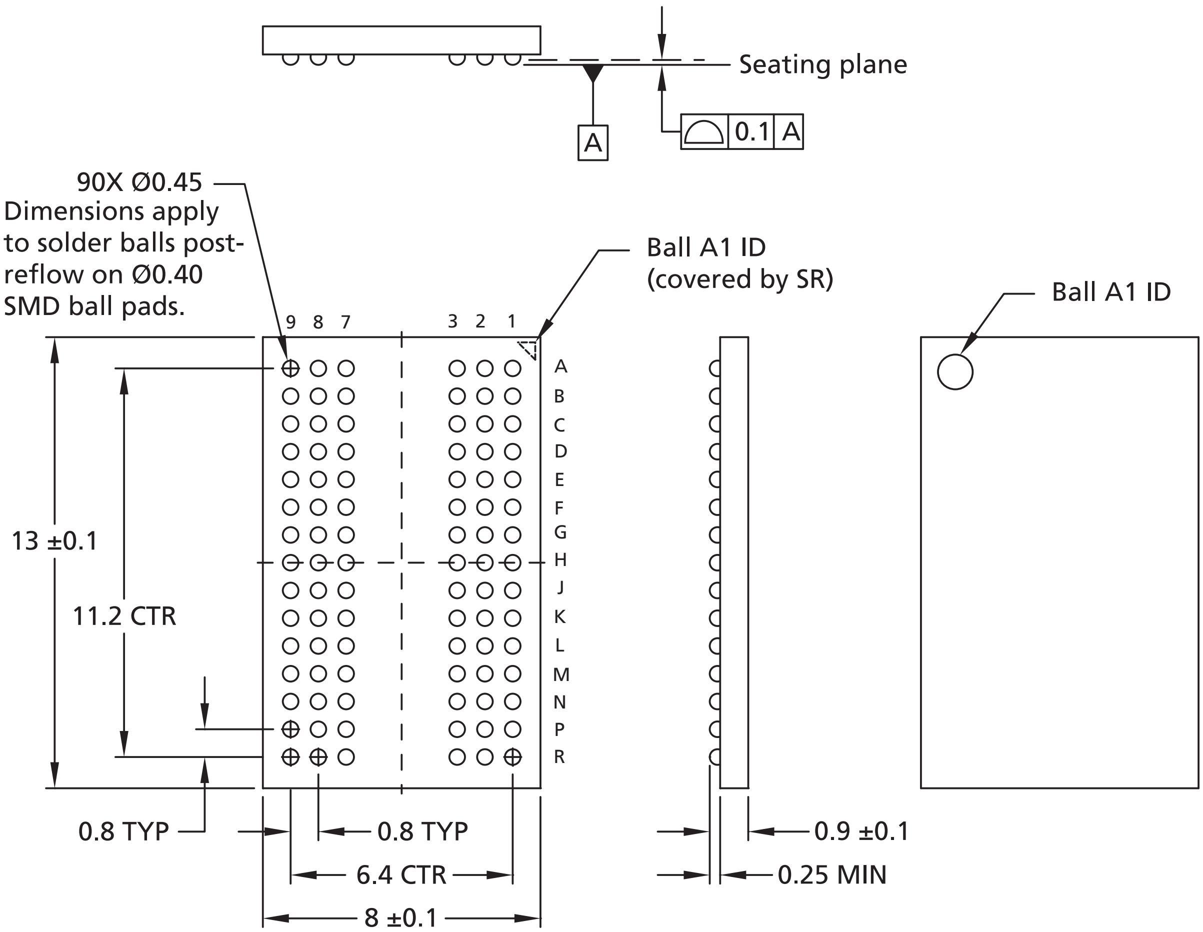
Figure 8: 90-Ball VFBGA (8mm x 13mm), Package Code: BQ



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Note 1 applies to all parameters in this table

Parameter	Symbol	Min	Max	Unit
V_{DD}/V_{DDQ} supply voltage relative to V_{SS}	V_{DD}/V_{DDQ}	–1.0	2.4	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.5	2.4 or (V_{DDQ} + 0.3V), whichever is less	V
Storage temperature (plastic)	T_{STG}	–55	150	˚C

Note: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Table 5: AC/DC Electrical Characteristics and Operating Conditions

Notes 1–5 apply to all parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{DD}	1.70	1.95	V	6, 7
I/O supply voltage	V_{DDQ}	1.70	1.95	V	6, 7
Address and command inputs					
Input voltage high	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9
Input voltage low	V_{IL}	–0.3	0.2 × V_{DDQ}	V	8, 9
Clock inputs (CK, CK#)					
DC input voltage	V_{IN}	–0.3	V_{DDQ} + 0.3	V	10
DC input differential voltage	$V_{ID(DC)}$	0.4 × V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
AC input differential voltage	$V_{ID(AC)}$	0.6 × V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
AC differential crossing voltage	V_{IX}	0.4 × V_{DDQ}	0.6 × V_{DDQ}	V	10, 12
Data inputs					
DC input high voltage	$V_{IH(DC)}$	0.7 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
DC input low voltage	$V_{IL(DC)}$	–0.3	0.3 × V_{DDQ}	V	8, 9, 13
AC input high voltage	$V_{IH(AC)}$	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
AC input low voltage	$V_{IL(AC)}$	–0.3	0.2 × V_{DDQ}	V	8, 9, 13
Data outputs					
DC output high voltage: Logic 1 (I_{OH} = –0.1mA)	V_{OH}	0.9 × V_{DDQ}	–	V	
DC output low voltage: Logic 0 (I_{OL} = 0.1mA)	V_{OL}	–	0.1 × V_{DDQ}	V	
Leakage current					
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	–1	1	µA	

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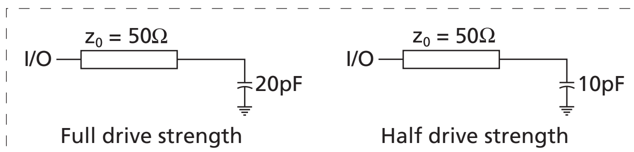
Table 5: AC/DC Electrical Characteristics and Operating Conditions (Continued)

Notes 1–5 apply to all parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current (DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	–1.5	1.5	µA	
Operating temperature					
Commercial	T_A	0	70	˚C	
Wireless	T_A	–25	85	˚C	
Industrial	T_A	–40	85	˚C	
Automotive	T_A	–40	105	˚C	

Notes:
1. All voltages referenced to V_{SS}.
2. All parameters assume proper device initialization.
3. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
4. Outputs measured with equivalent load; transmission line delay is assumed to be very small:



5. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ/2}$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ/2}$.
6. Any positive glitch must be less than one-third of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than one-third of the clock cycle and not exceed either –150mV or +1.6V, whichever is more positive.
7. V_{DD} and V_{DDQ} must track each other and V_{DDQ} must be less than or equal to V_{DD}.
8. To maintain a valid level, the transitioning edge of the input must:
   8a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ Or $V_{IH(AC)}$.
   8b. Reach at least the target AC level.
   8c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.
9. V_{IH} overshoot: V_{IHmax} = V_{DDQ} + 1.0V for a pulse width ≤3ns and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: V_{ILmin} = –1.0V for a pulse width ≤3ns and the pulse width cannot be greater than one-third of the cycle rate.
10. CK and CK# input slew rate must be ≥1 V/ns (2 V/ns if measured differentially).
11. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
12. The value of V_{IX} is expected to equal $V_{DDQ/2}$ of the transmitting device and must track variations in the DC level of the same.
13. DQ and DM input slew rates must not deviate from DQS by more than 10%. 50ps must be added to ^tDS and ^tDH for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.

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Table 6: Capacitance (x16, x32)

Notes 1 and 2 apply to all the parameters in this table

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance: CK, CK#	C_{CK}	1.0	2.0	pF	
Delta input capacitance: CK, CK#	C_{DCK}	0	0.25	pF	3
Input capacitance: command and address	C_I	1.0	2.0	pF	
Delta input capacitance: command and address	C_{DI}	– 0.5	0.5	pF	3
Input/output capacitance: DQ, DQS, DM	C_{IO}	1.25	2.5	pF	
Delta input/output capacitance: DQ, DQS, DM	C_{DIO}	– 0.6	0.6	pF	4

Notes:
1. This parameter is sampled. V_{DD}/V_{DDQ} = 1.70–1.95V, f = 100 MHz, T_A = 25˚C, $V_{OUT(DC)}$ = $V_{DDQ}/2$, V_{OUT} (peak-to-peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
2. This parameter applies to die devices only (does not include package capacitance).
3. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
4. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

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Electrical Specifications – I_{DD} Parameters

Table 7: I_{DD} Specifications and Conditions, –40°C to +85°C (x16)

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Speed -48	Unit	Notes
Operating 1 bank active precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	75	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	900	μA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	900	μA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	15	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	9	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	5	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	5	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3N}	17	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	14	mA	6
Operating burst read: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	90	mA	6
Operating burst write: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	90	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^tRFC = 138ns	I_{DD5}	170	mA	10
	$^tRFC = {}^tREFI$	I_{DD5A}	12	mA	10, 11
Deep power-down current: Address and control balls are stable; Data bus inputs are stable		I_{DD8}	10	μA	7, 13

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Table 8: I_{DD} Specifications and Conditions, –40°C to +85°C (x32)

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Speed -48	Unit	Notes
Operating 1 bank active precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	75	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	900	µA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	900	µA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	15	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	9	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	5	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	5	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3N}	17	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	14	mA	6
Operating burst read: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	90	mA	6
Operating burst write: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	90	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^tRFC = 138ns	I_{DD5}	170	mA	10
	$^tRFC = {}^tREFI$	I_{DD5A}	12	mA	10, 11
Deep power-down current: Address and control balls are stable; Data bus inputs are stable		I_{DD8}	10	µA	7, 13

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Table 9: I_{DD} Specifications and Conditions, –40°C to +105°C (x16)

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Speed -48	Unit	Notes
Operating 1 bank active precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	100	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	1500	μA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	1500	μA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	19	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	13	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	9	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	9	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stableS		I_{DD3N}	21	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	18	mA	6
Operating burst read: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	130	mA	6
Operating burst write: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	130	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^tRFC = 138ns	I_{DD5}	170	mA	10
	$^tRFC = {}^tREFI$	I_{DD5A}	13	mA	10, 11
Deep power-down current: Address and control balls are stable; Data bus inputs are stable		I_{DD8}	15	μA	7, 13

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Table 10: I_{DD} Specifications and Conditions, –40°C to +105°C (x32)

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Speed -48	Unit	Notes
Operating 1 bank active precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	100	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	1500	µA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	1500	µA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	19	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	13	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	9	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	9	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3N}	21	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	18	mA	6
Operating burst read: 1 bank active; BL = 4; CL = 3; $^tCK = {}^tCK$ (MIN); Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	150	mA	6
Operating burst write: One bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	150	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^tRFC = 138ns	I_{DD5}	170	mA	10
	$^tRFC = {}^tREFI$	I_{DD5A}	13	mA	10, 11
Deep power-down current: Address and control pins are stable; Data bus inputs are stable		I_{DD8}	15	µA	7, 13

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Table 11: $I_{DD}6$ Specifications and Conditions

Notes 1–5, 7, and 12 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Value	Units
Self refresh: CKE = LOW; ^tCK = ^tCK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full array, 105˚C	I_{DD6}	n/a[14]	µA
	Full array, 85˚C		2000	µA
	Full array, 45˚C		900	µA
	1/2 array, 85˚C		1450	µA
	1/2 array, 45˚C		700	µA
	1/4 array, 85˚C		1230	µA
	1/4 array, 45˚C		600	µA
	1/8 array, 85˚C		1090	µA
	1/8 array, 45˚C		575	µA
	1/16 array, 85˚C		1020	µA
	1/16 array, 45˚C		550	µA

Notes:
1. All voltages referenced to V_{SS}.
2. Tests for I_{DD} characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ/2}$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ/2}$.
4. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time with the outputs open.
5. I_{DD} specifications are tested after the device is properly initialized and values are averaged at the defined cycle rate.
6. MIN (^tRC or ^tRFC) for I_{DD} measurements is the smallest multiple of ^tCK that meets the minimum absolute value for the respective parameter. ^tRAS (MAX) for I_{DD} measurements is the largest multiple of ^tCK that meets the maximum absolute value for ^tRAS.
7. Measurement is taken 500ms after entering into this operating mode to provide settling time for the tester.
8. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.
9. I_{DD2N} specifies DQ, DQS, and DM to be driven to a valid high or low logic level.
10. CKE must be active (HIGH) during the entire time a REFRESH command is executed. From the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge until ^tRFC later.
11. This limit is a nominal value and does not result in a fail. CKE is HIGH during REFRESH command period (^tRFC (MIN)) else CKE is LOW (for example, during standby).
12. Values for I_{DD6} 85˚C are guaranteed for the entire temperature range. All other I_{DD6} values are estimated.
13. Typical values at 25˚C, not a maximum value.
14. Self refresh is not supported for AT (85˚C to 105˚C) operation.

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