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Automotive LPDDR SDRAM

MT46H128M16LF – 32 Meg x 16 x 4 Banks
MT46H64M32LF – 16 Meg x 32 x 4 Banks
MT46H128M32L2 – 16 Meg x 32 x 4 Banks x 2
MT46H256M32L4 – 32 Meg x 16 x 4 Banks x 4
MT46H256M32R4 - 32 Meg x 16 x 4 Banks x 4

Features

- V_{DD}/V_{DDQ} = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- 4 internal banks for concurrent operation
- Data masks (DM) for masking write data; one mask per byte
- Programmable burst lengths (BL): 2, 4, 8, or 16
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- Temperature-compensated self refresh (TCSR)
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Status read register (SRR)
- Selectable output drive strength (DS)
- Clock stop capability
- 64ms refresh; 32ms for the automotive temperature range

Table 1: Key Timing Parameters (CL = 3)

Speed Grade	Clock Rate	Access Time
-5	200 MHz	5.0ns
-54	185 MHz	5.0ns
-6	166 MHz	5.0ns
-75	133 MHz	6.0ns

Options — Mark

- V_{DD}/V_{DDQ}
  - 1.8V/1.8V — H
- Configuration
  - 128 Meg x 16 (32 Meg x 16 x 4 banks) — 128M16
  - 64 Meg x 32 (16 Meg x 32 x 4 banks) — 64M32
- Addressing
  - JEDEC-standard — LF
  - Reduced page-size[1] — LG
  - 4-die stack reduced page-size[2] — R4
  - 2-die stack standard — L2
  - 4-die stack standard — L4
- Plastic "green" package
  - 60-ball VFBGA (10mm x 10mm)[3] — B7
  - 90-ball VFBGA (9mm x 13mm)[4] — CX
- PoP (plastic "green" package)
  - 168-ball VFBGA (12mm x 12mm)[4] — JV
  - 168-ball WFBGA (12mm x 12mm)[4] — KQ
  - 168-ball WFBGA (12mm x 12mm)[4] — MA
  - 240-ball WFBGA (14mm x 14mm)[4] — MC
- Timing – cycle time
  - 5ns @ CL = 3 (200 MHz) — -5
  - 5.4ns @ CL = 3 (185 MHz) — -54
  - 6ns @ CL = 3 (166 MHz) — -6
  - 7.5ns @ CL = 3 (133 MHz) — -75
- Power
  - Standard I_{DD2}/I_{DD6} — None
- Product grade
  - Automotive (package-level burn-in) — A
- Operating temperature range
  - From –40°C to +85°C — IT
  - From –40°C to +105°C[1] — AT
- Design revision — :B

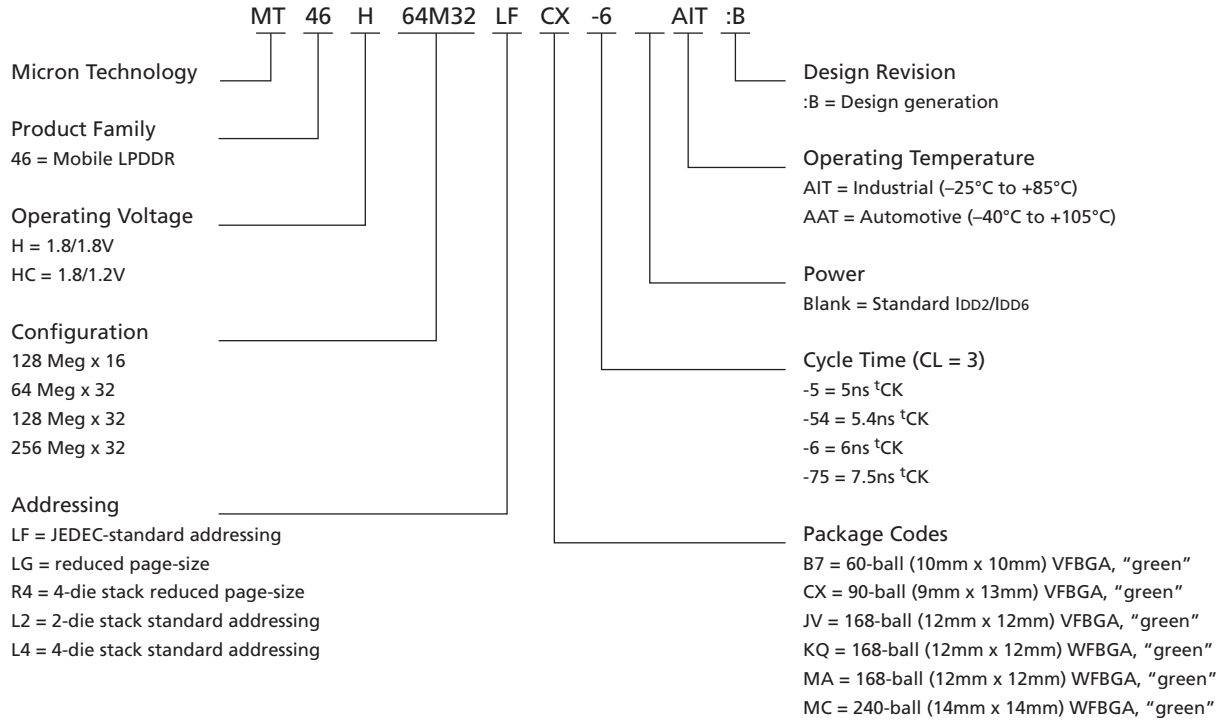
Notes:
1. Contact factory for availability.
2. Available in the 168-ball JV package only.
3. Available only for x16 configuration.
4. Available only for x32 configuration.

Table 2: Configuration Addressing – 2Gb

Architecture	128 Meg x 16	64 Meg x 32	Reduced Page-Size Option 128 Meg x 16	Reduced Page-Size Option 64 Meg x 32
Configuration	32 Meg x 16 x 4 banks	16 Meg x 32 x 4 banks	32 Meg x 16 x 4 banks	16 Meg x 32 x 4 banks
Refresh count	8K	8K	8K	8K
Row addressing	16K A[13:0]	16K A[13:0]	32K A[14:0]	32K A[14:0]
Column addressing	2K A11, A[9:0]	1K A[9:0]	1K A[9:0]	512 A[8:0]

See Package Block Diagrams (page 16) for descriptions of signal connections and die configurations for each respective architecture.

Figure 1: 2Gb Mobile LPDDR Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Contents

List of Figures

List of Tables

General Description

The 2Gb Mobile low-power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 2,147,483,648 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits. In the reduced page-size (LG) option, each of the x32's 536,870,912-bit banks is organized as 32,768 rows by 512 columns by 32 bits. In the reduced page-size (R4) option, each of the x16's 536,870,912-bit banks is organized as 32,768 rows by 1024 columns x 16 bits.

Note:

1. Throughout this data sheet, various figures and text refer to DQs as "DQ." DQ should be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]), DM refers to UDM and DQS refers to UDQS. The x32 is divided into 4 bytes. For DQ[7:0], DM refers to DM0 and DQS refers to DQS0. For DQ[15:8], DM refers to DM1 and DQS refers to DQS1. For DQ[23:16], DM refers to DM2 and DQS refers to DQS2. For DQ[31:24], DM refers to DM3 and DQS refers to DQS3.

2. Complete functionality is described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

3. Any specific requirement takes precedence over a general statement.

Functional Block Diagrams

Figure 2: Functional Block Diagram (x16)

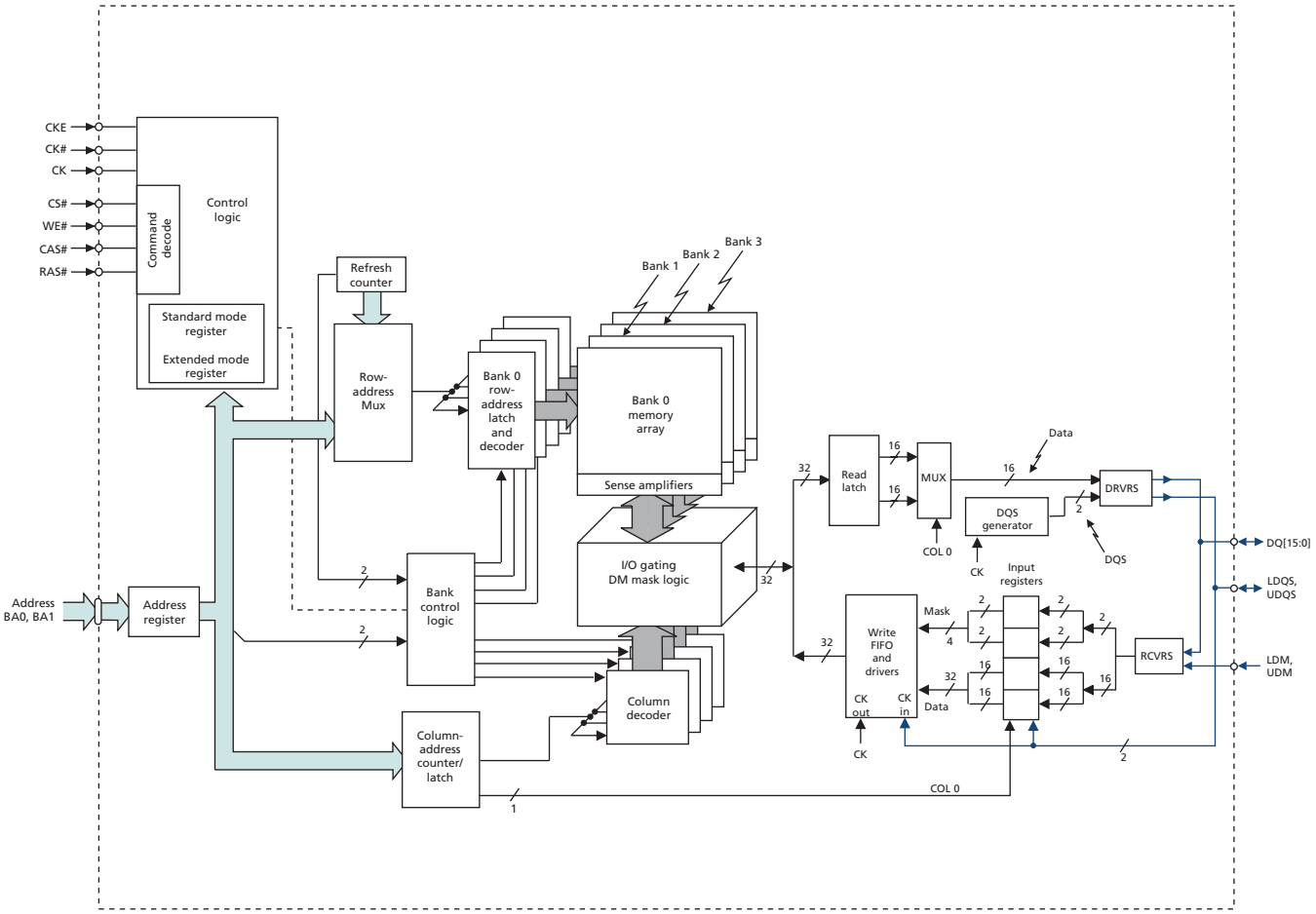
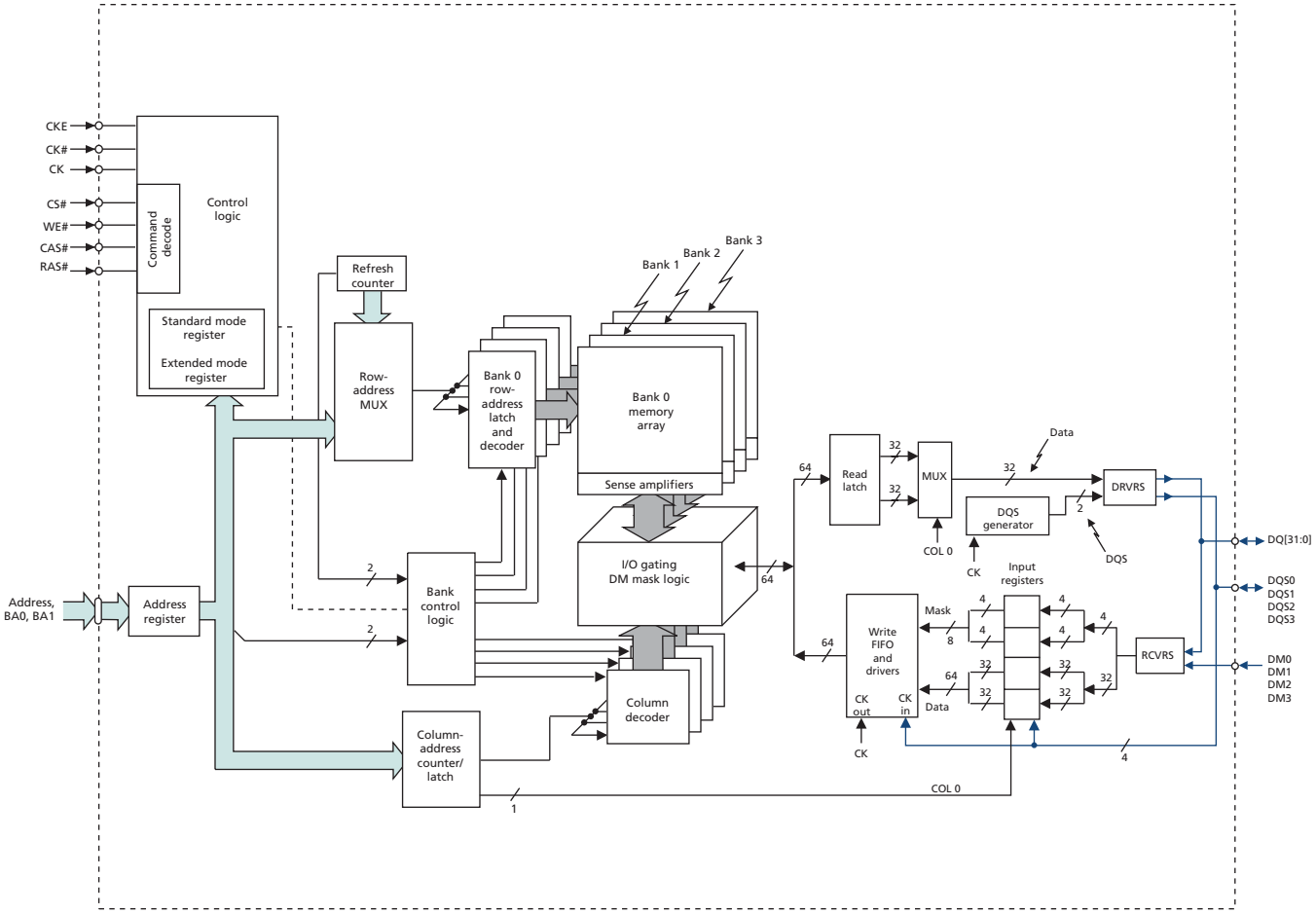
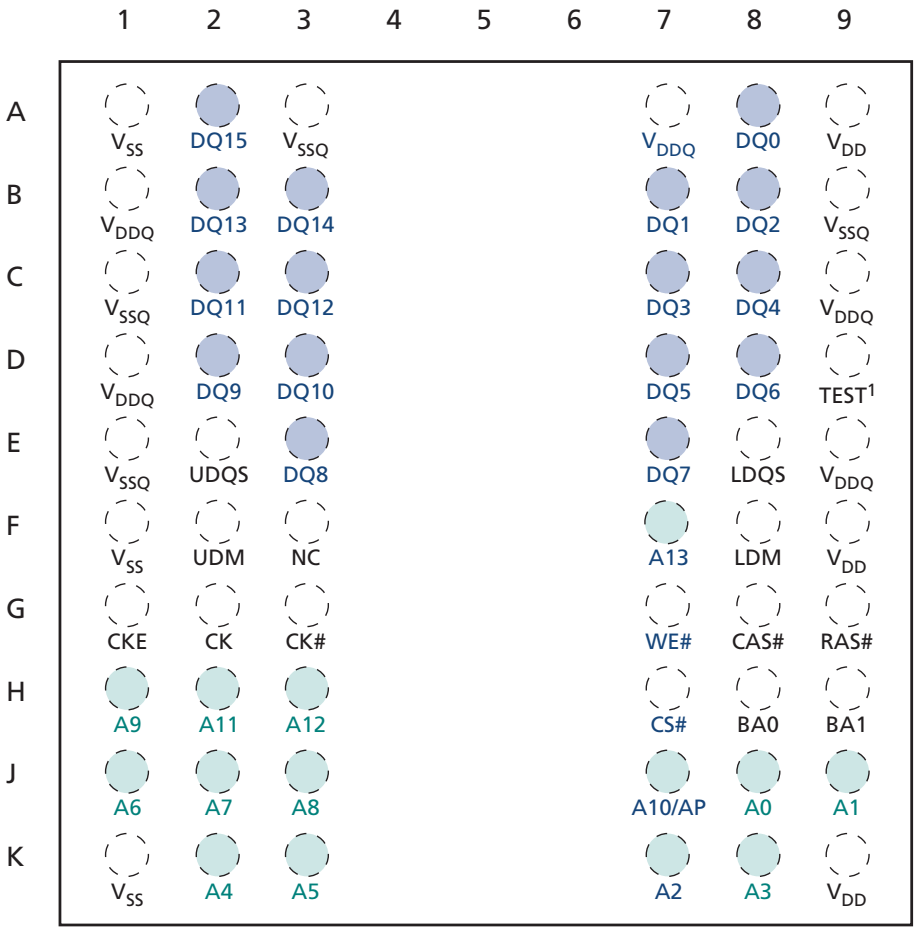


Figure 3: Functional Block Diagram (x32)



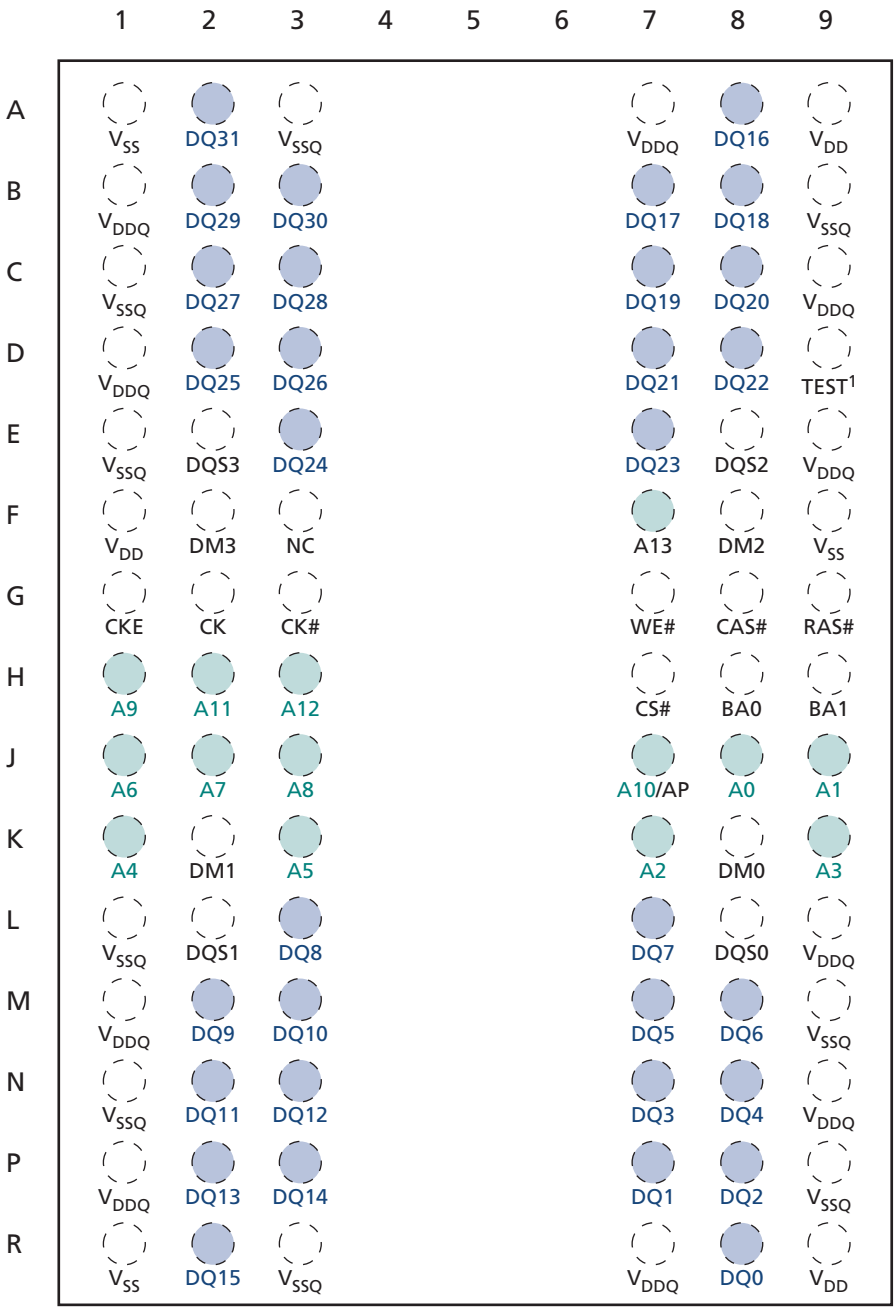
Ball Assignments

Figure 4: 60-Ball VFBGA – Top View, x16 only



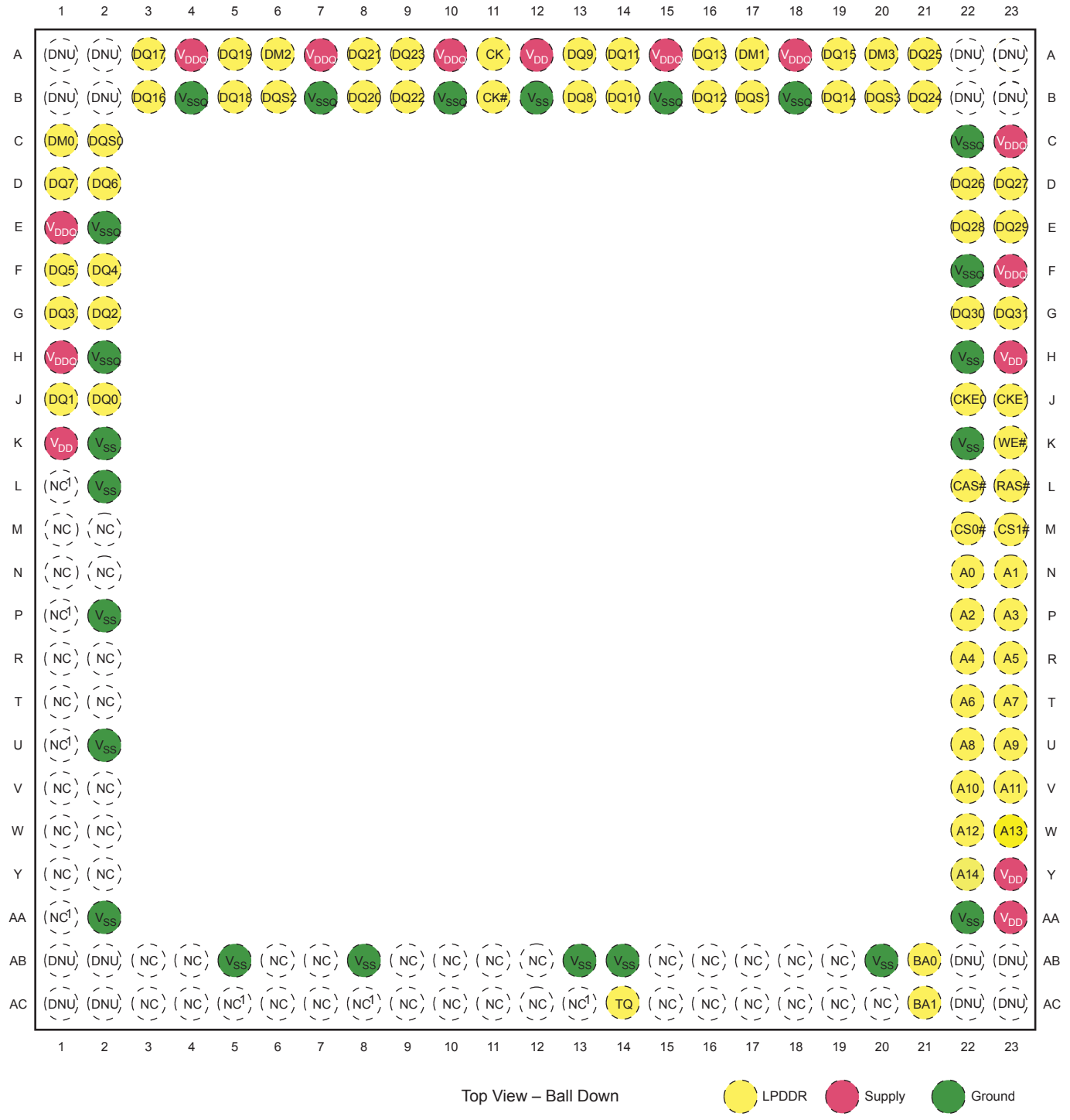
Notes:
1. D9 is a test pin that must be tied to V_{SS} or V_{SSQ} in normal operations.
2. Unused address pins become RFU.

Figure 5: 90-Ball VFBGA – Top View, x32 only



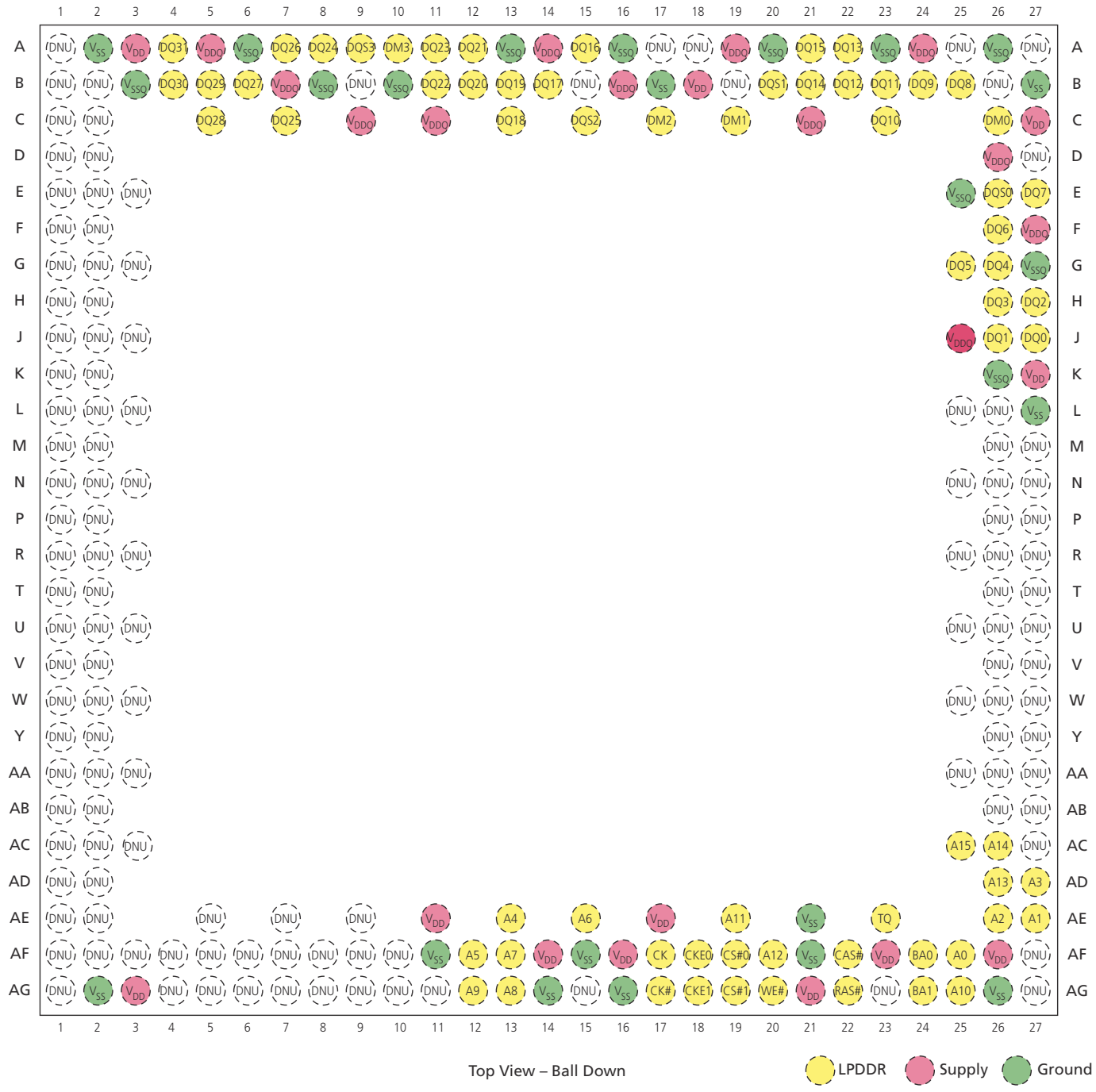
Notes:
1. D9 is a test pin that must be tied to V_{SS} or V_{SSQ} in normal operations.
2. Unused address pins become RFU.

Figure 6: 168-Ball FBGA – 12mm x 12mm (Top View), x32 only



Note: 1. Although not bonded to the die, these pins may be connected on the package substrate.

Figure 7: 240-Ball FBGA – 14mm x 14mm (Top View), x32 only



Ball Descriptions

The ball descriptions table is a comprehensive list of all possible balls for all supported packages. Not all balls listed are supported for a given package.

Table 3: Ball Descriptions

Symbol	Type	Description
CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
CKE CKE0, CKE1	Input	Clock enable: CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes. CKE0 is used for a single LPDDR product. CKE1 is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
CS# CS0#, CS1#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. CS0# is used for a single LPDDR product. CS1# is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
UDM, LDM (x16) DM[3:0] (x32)	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls.
BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is loaded during a LOAD MODE REGISTER command.
A[13:0]	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. The maximum address range is dependent upon configuration. Unused address balls become RFU.
TEST	Input	Test pin: Must be tied to V_{SS} or V_{SSQ} in normal operations.
DQ[15:0] (x16) DQ[31:0] (x32)	Input/ output	Data input/output: Data bus for x16 and x32.
LDQS, UDQS (x16) DQS[3:0] (x32)	Input/ output	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned in write data. It is used to capture data.
TQ	Output	Temperature sensor output: TQ HIGH when LPDDR T_J exceeds 85°C.
V_{DDQ}	Supply	DQ power supply.

Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
V_{SSQ}	Supply	DQ ground.
V_{DD}	Supply	Power supply.
V_{SS}	Supply	Ground.
NC	–	No connect: May be left unconnected.
RFU	–	Reserved for future use. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Package Block Diagrams

Figure 8: Single Rank, Single Channel (1 Die) Package Block Diagram

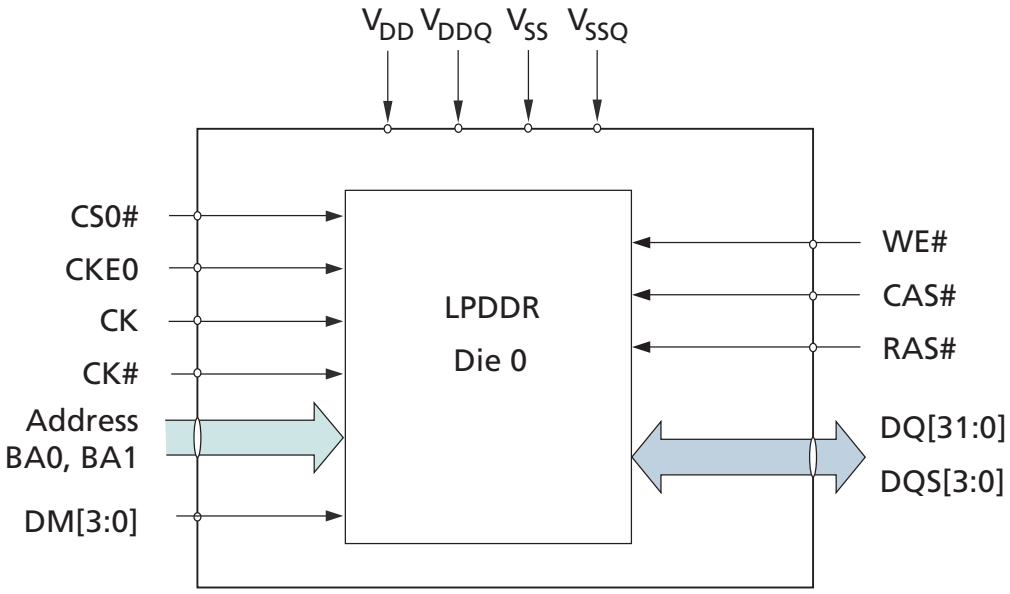


Figure 9: Dual Rank, Single Channel (2 Die) Package Block Diagram

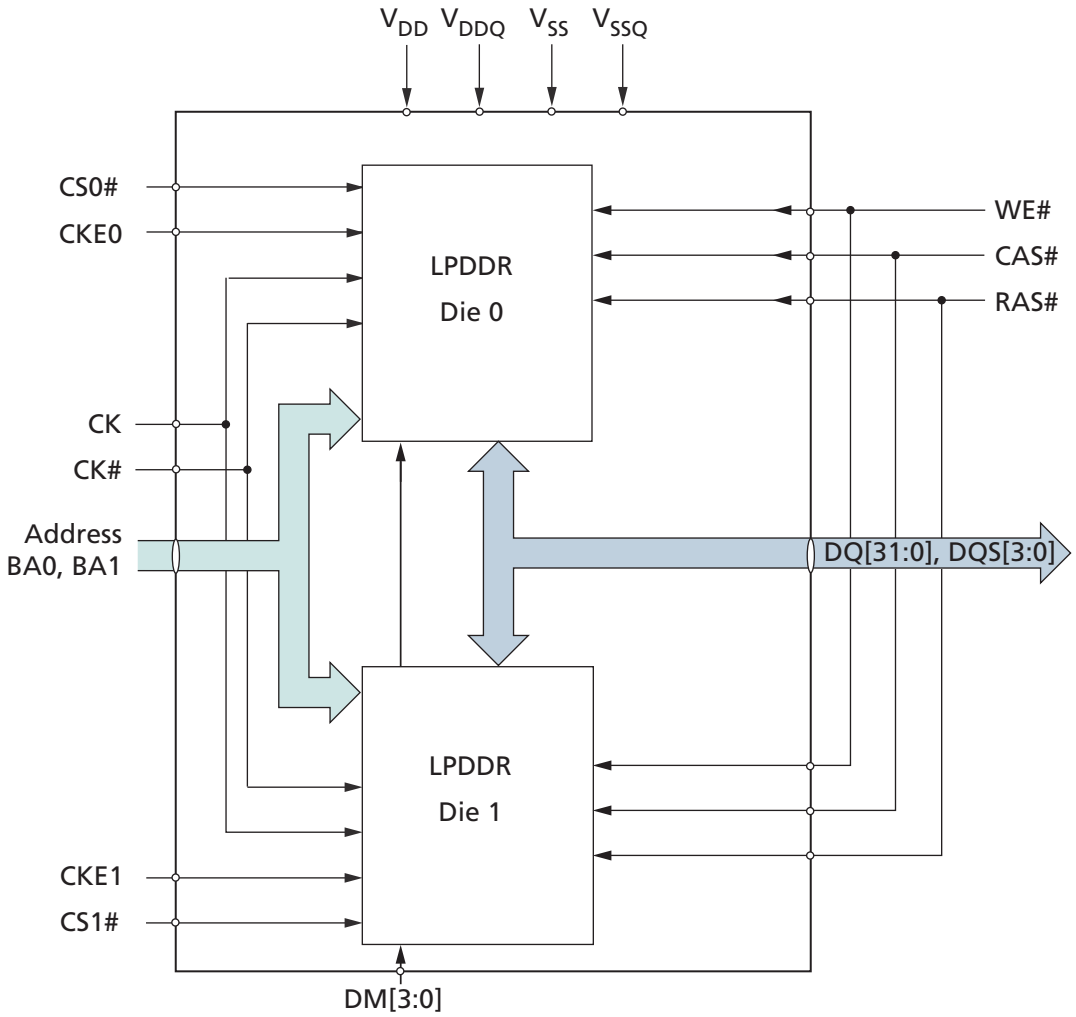
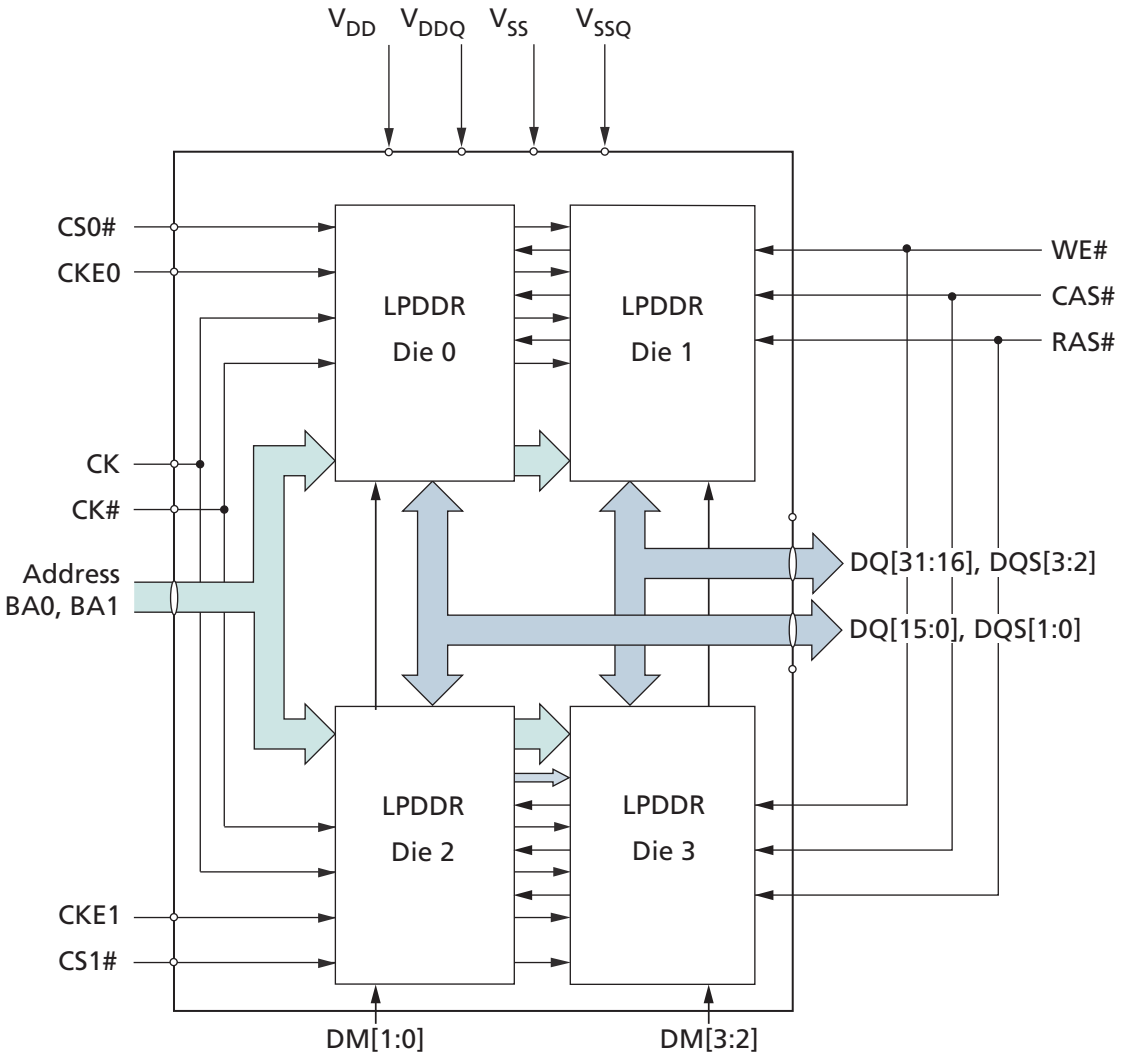
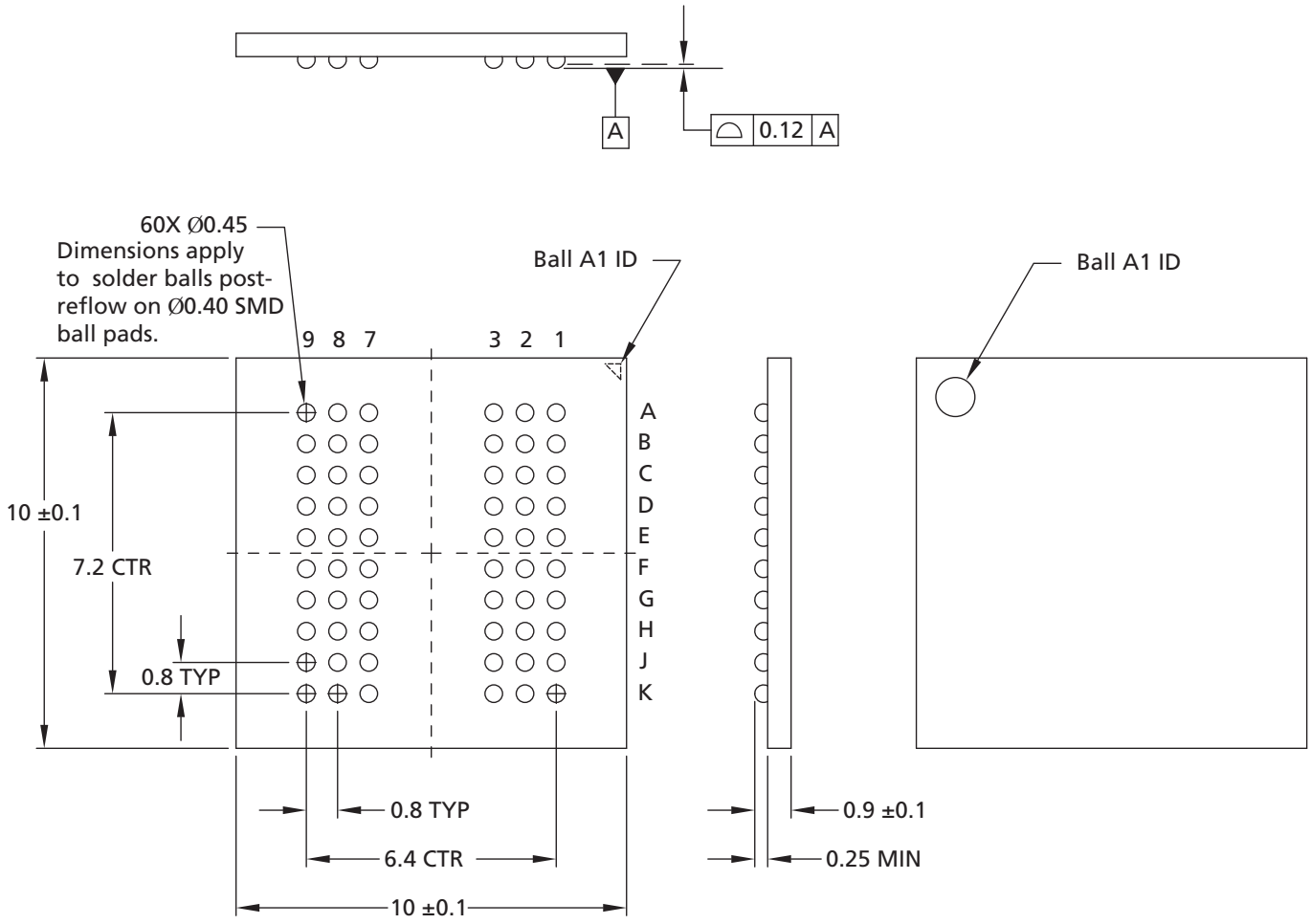


Figure 10: Dual Rank, Single Channel (4 Die) Package Block Diagram



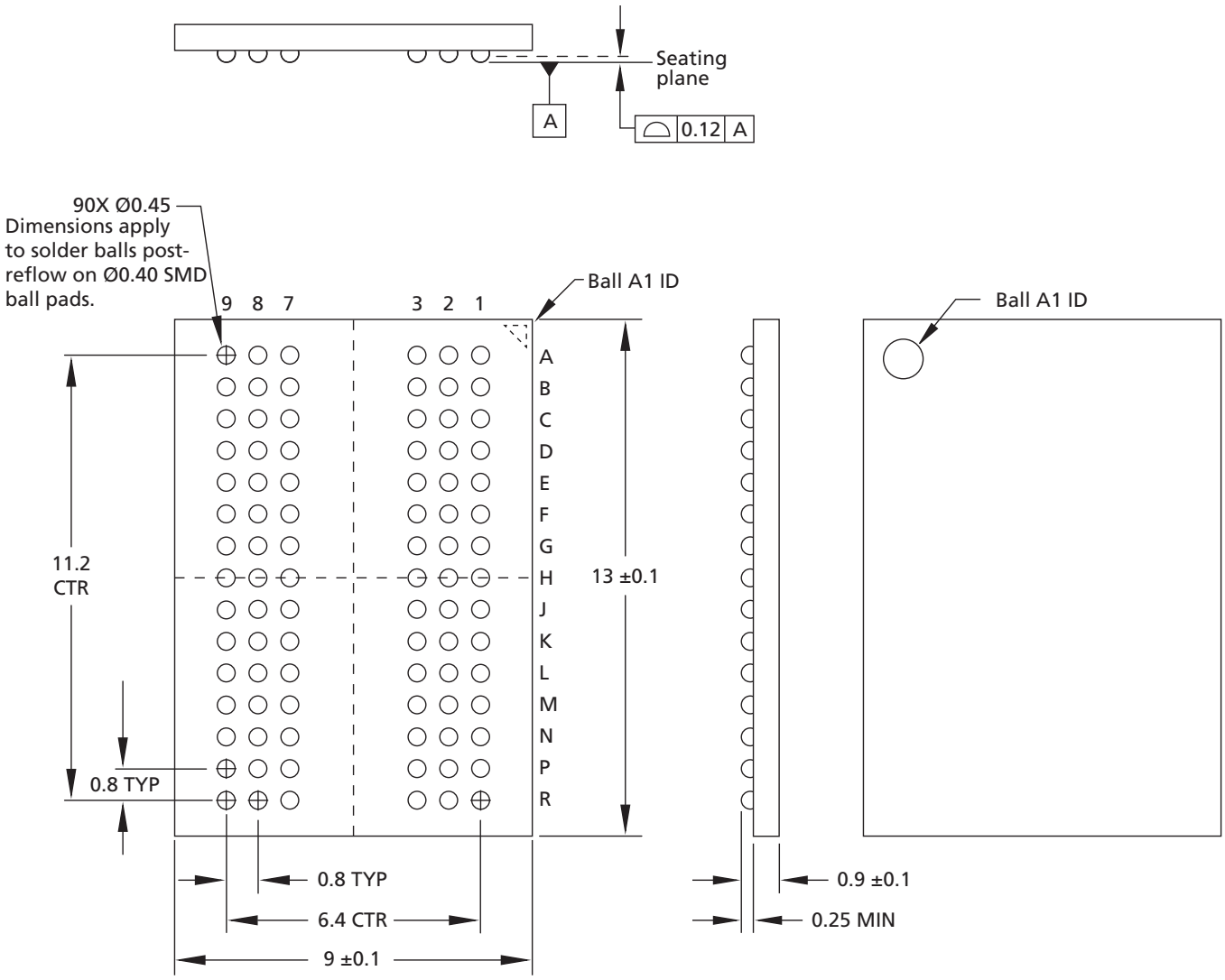
Package Dimensions

Figure 11: 60-Ball FBGA (10mm x 10mm), Package Code: B7



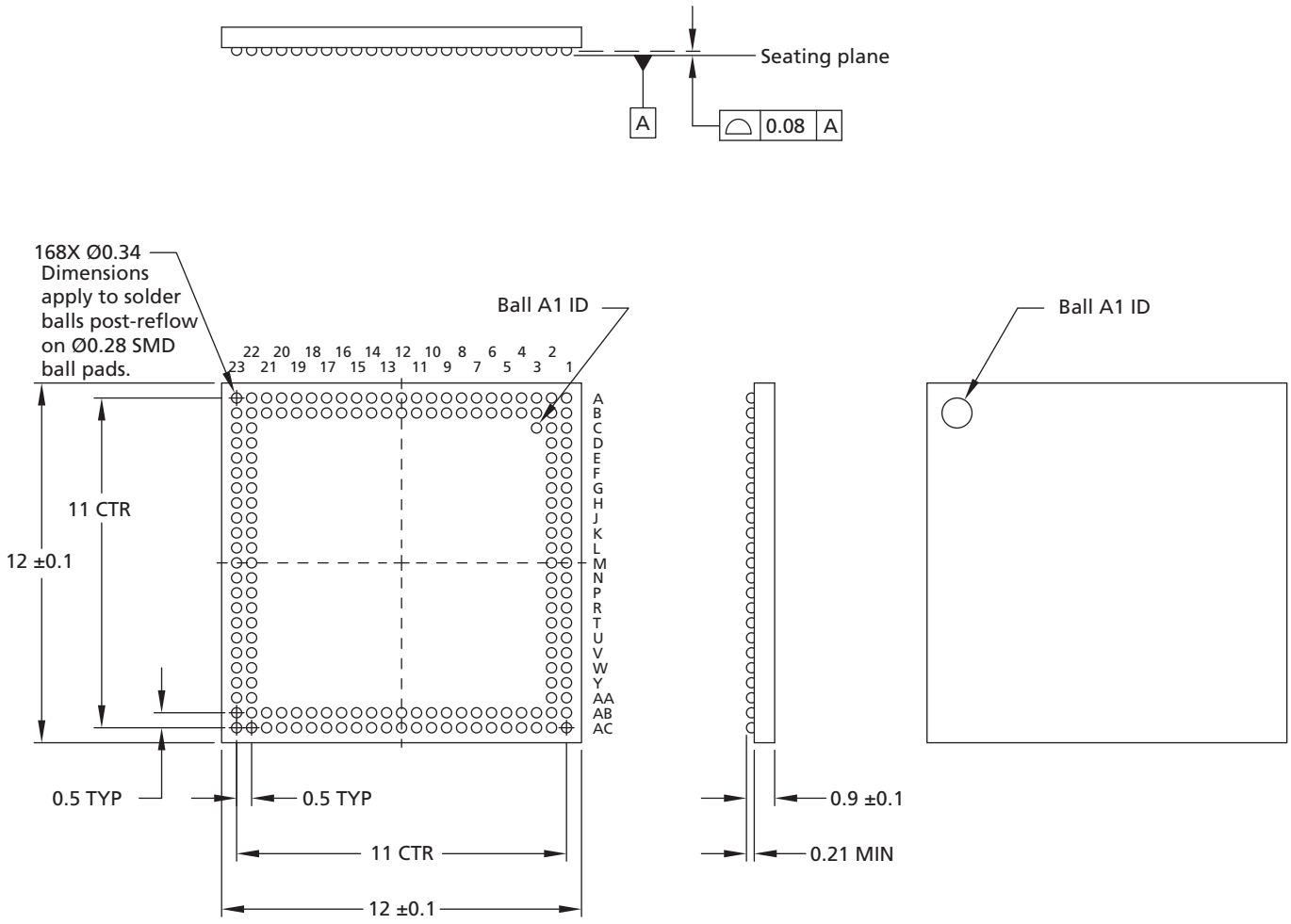
Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu).

Figure 12: 90-Ball FBGA (9mm x 13mm), Package Code: CX



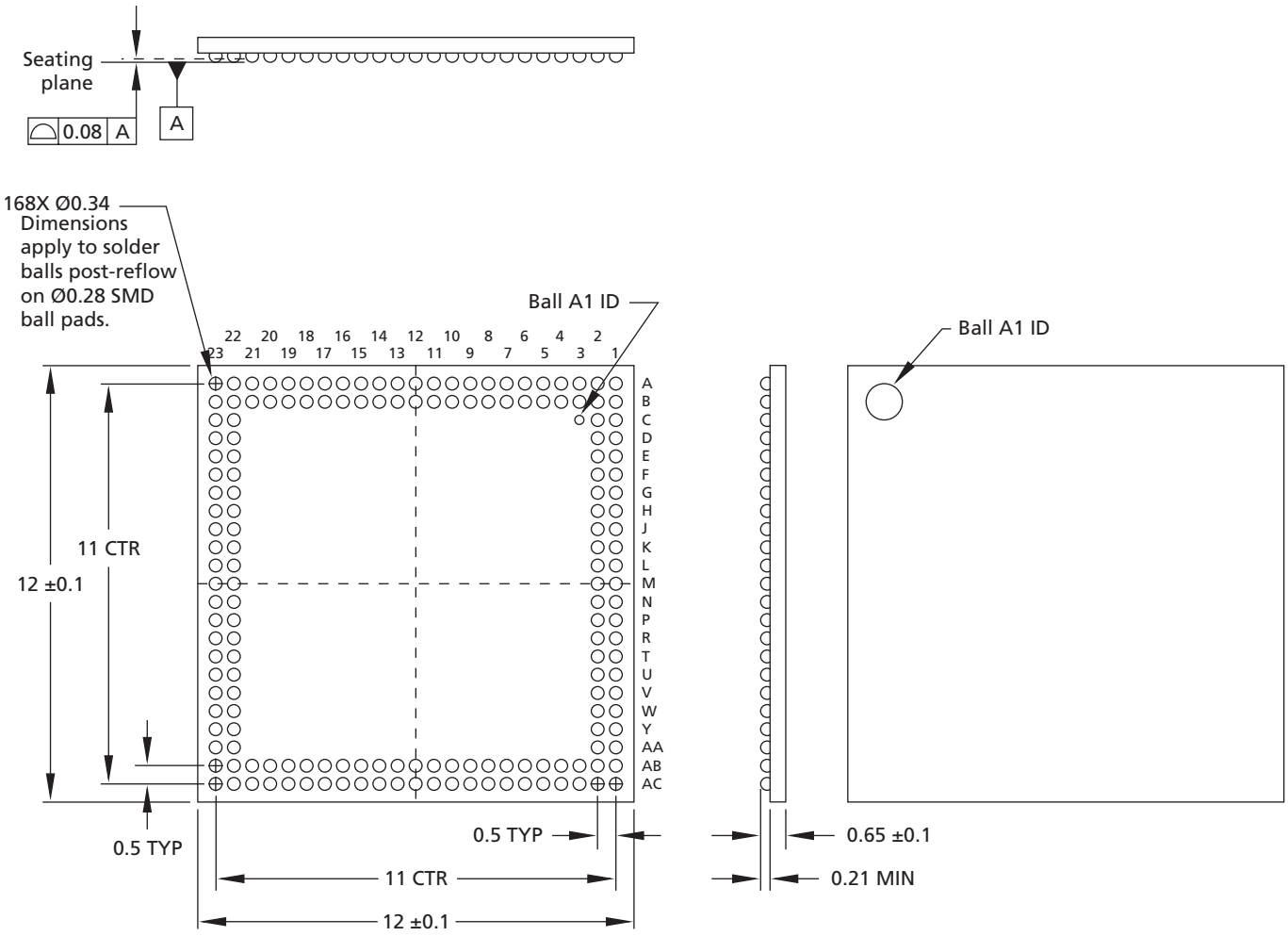
Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu).

Figure 13: 168-Ball FBGA (12mm x 12mm), Package Code: JV



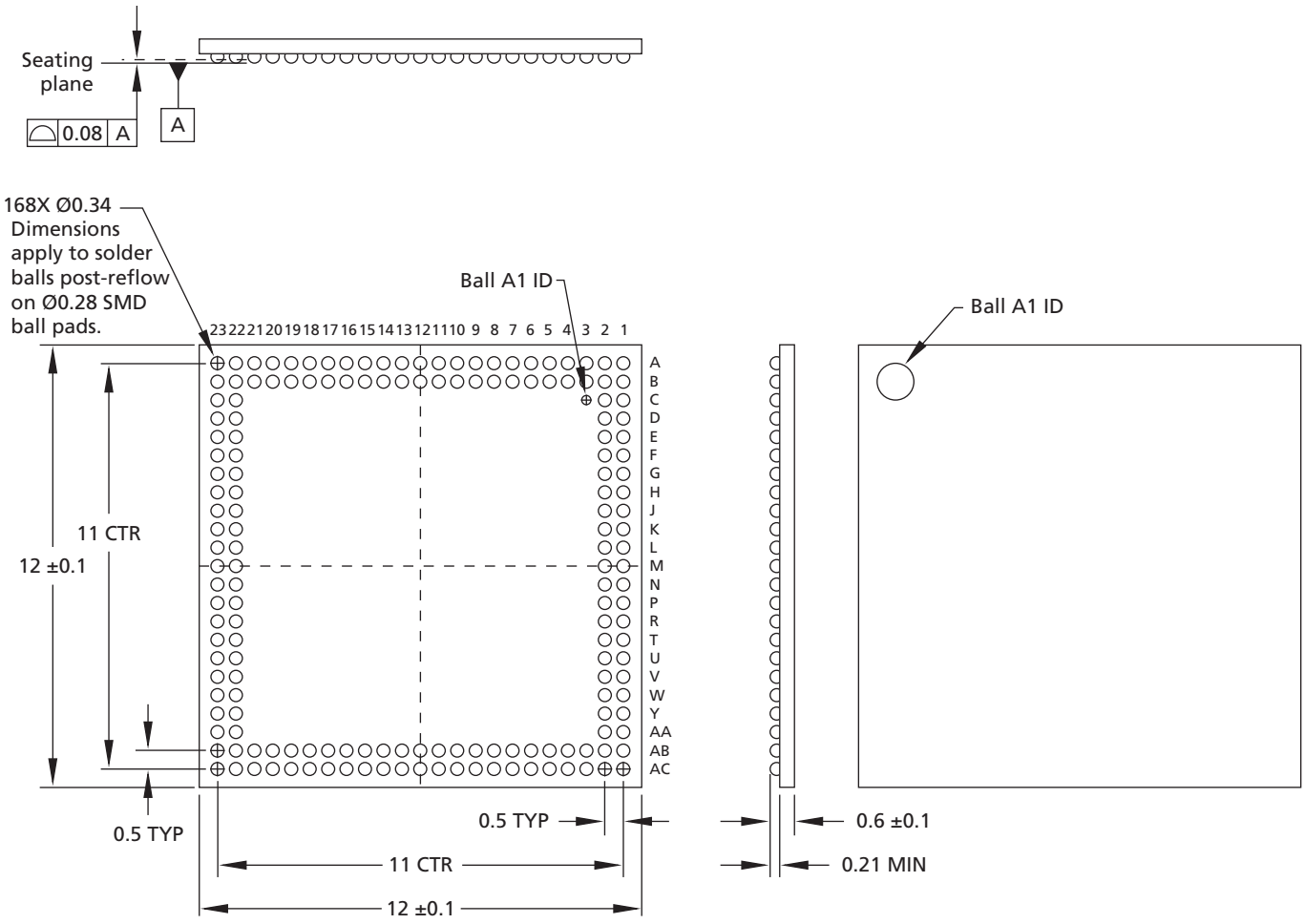
Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu).

Figure 14: 168-Ball FBGA (12mm x 12mm), Package Code: KQ



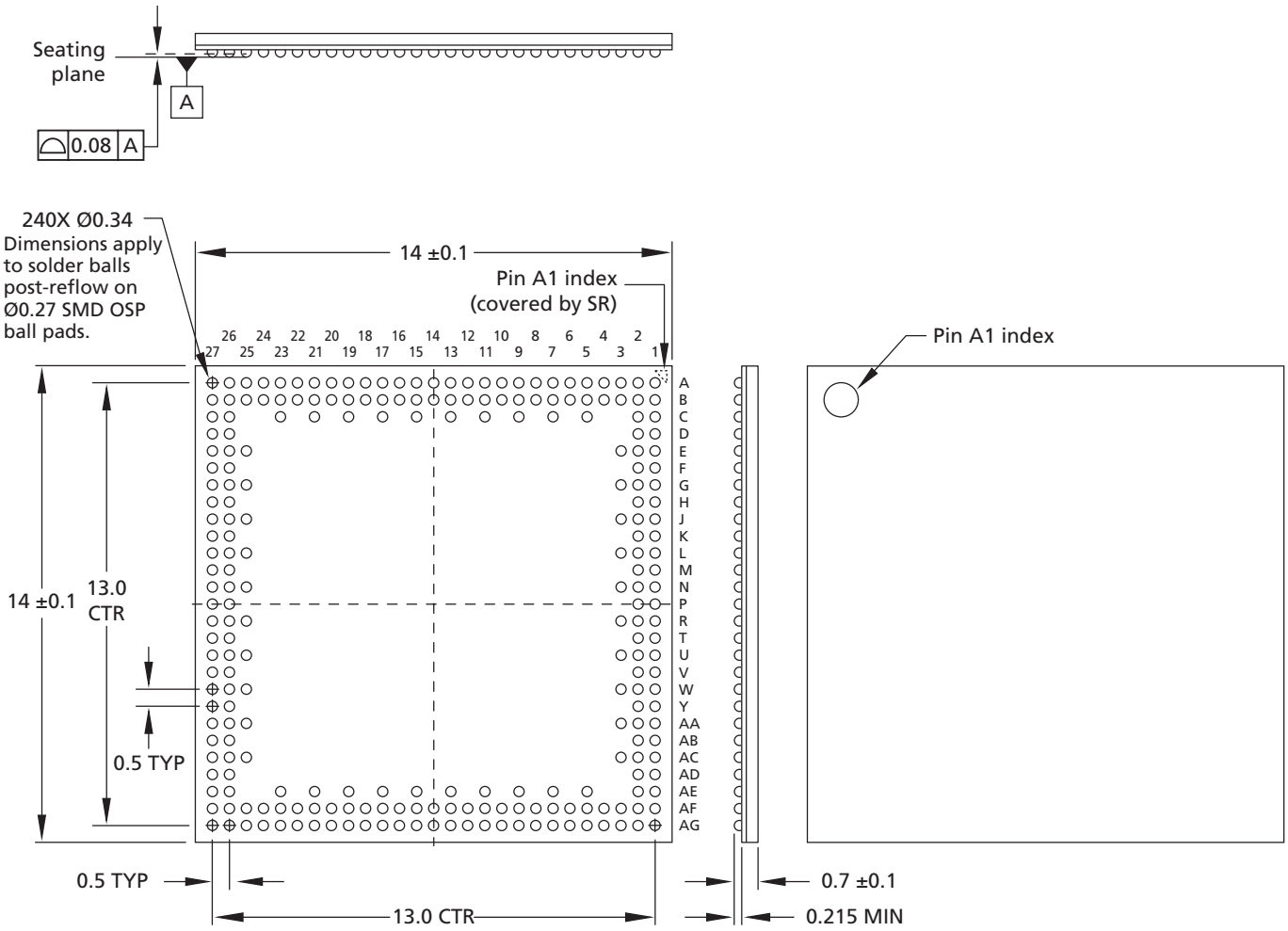
Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu).

Figure 15: 168-Ball FBGA (12mm x 12mm), Package Code: MA



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu).

Figure 16: 240-Ball FBGA (14mm x 14mm), Package Code: MC



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: LF35 with OSP plating (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Note 1 applies to all parameters in this table

Parameter	Symbol	Min	Max	Unit
V_{DD}/V_{DDQ} supply voltage relative to V_{SS}	V_{DD}/V_{DDQ}	–1.0	2.4	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.5	2.4 or (V_{DDQ} + 0.3V), whichever is less	V
Storage temperature (plastic)	T_{STG}	–55	150	°C

Note: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Table 5: AC/DC Electrical Characteristics and Operating Conditions

Notes 1–5 apply to all parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{DD}	1.70	1.95	V	6, 7
I/O supply voltage	V_{DDQ}	1.70	1.95	V	6, 7
Address and command inputs					
Input voltage high	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9
Input voltage low	V_{IL}	–0.3	0.2 × V_{DDQ}	V	8, 9
Clock inputs (CK, CK#)					
DC input voltage	V_{IN}	–0.3	V_{DDQ} + 0.3	V	10
DC input differential voltage	$V_{ID(DC)}$	0.4 × V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
AC input differential voltage	$V_{ID(AC)}$	0.6 × V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
AC differential crossing voltage	V_{IX}	0.4 × V_{DDQ}	0.6 × V_{DDQ}	V	10, 12
Data inputs					
DC input high voltage	$V_{IH(DC)}$	0.7 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
DC input low voltage	$V_{IL(DC)}$	–0.3	0.3 × V_{DDQ}	V	8, 9, 13
AC input high voltage	$V_{IH(AC)}$	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
AC input low voltage	$V_{IL(AC)}$	–0.3	0.2 × V_{DDQ}	V	8, 9, 13
Data outputs					
DC output high voltage: Logic 1 (I_{OH} = –0.1mA)	V_{OH}	0.9 × V_{DDQ}	–	V	
DC output low voltage: Logic 0 (I_{OL} = 0.1mA)	V_{OL}	–	0.1 × V_{DDQ}	V	
Leakage current					
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	–1	1	µA	