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# Automotive LPDDR SDRAM

**MT46H32M16LF – 8 Meg x 16 x 4 banks**

**MT46H16M32LF – 4 Meg x 32 x 4 banks**

**MT46H16M32LG – 4 Meg x 32 x 4 banks**

## Features

- $V_{DD}/V_{DDQ} = 1.70\text{--}1.95\text{V}$
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- 4 internal banks for concurrent operation
- Data masks (DM) for masking write data; one mask per byte
- Programmable burst lengths (BL): 2, 4, 8, or 16
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- Temperature-compensated self refresh (TCSR)
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Status read register (SRR)
- Selectable output drive strength (DS)
- Clock stop capability
- 64ms refresh, 32ms for automotive temperature

## Options

- $V_{DD}/V_{DDQ}$ 
  - 1.8V/1.8V H
- Configuration
  - 32 Meg x 16 (8 Meg x 16 x 4 banks) 32M16
  - 16 Meg x 32 (4 Meg x 32 x 4 banks) 16M32
- Addressing
  - JEDEC-standard addressing LF
- Plastic "green" package
  - 60-ball VFBGA (8mm x 9mm)<sup>1</sup> BF
  - 90-ball VFBGA (8mm x 13mm)<sup>2</sup> B5
  - 90-ball VFBGA (8mm x 13mm)<sup>2</sup> BQ
- Timing – cycle time
  - 5ns @ CL = 3 (200 MHz) -5
  - 6ns @ CL = 3 (166 MHz) -6
- Power
  - Standard  $I_{DD2}/I_{DD6}$  None
  - Low-power  $I_{DD2}/I_{DD6}$  L
- Product certification
  - Automotive A
- Operating temperature range
  - Industrial (–40°C to +85°C) IT
  - Automotive (–40°C to +105°C) AT
- Design revision :C

Notes: 1. Only available for x16 configuration.  
2. Only available for x32 configuration.

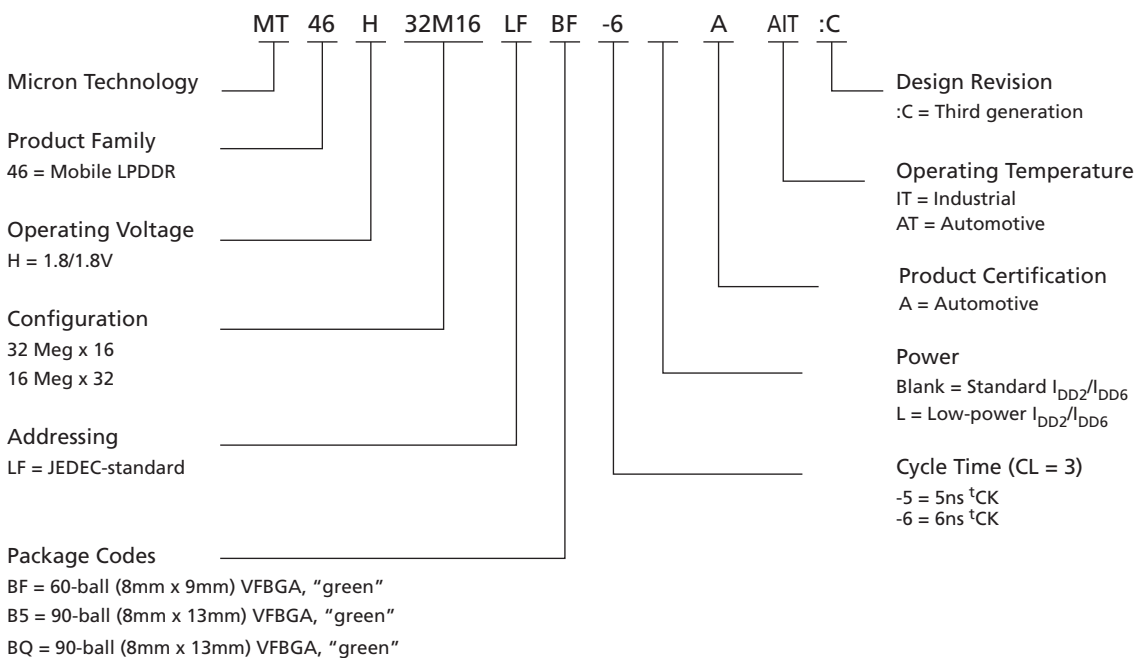
**Table 1: Key Timing Parameters (CL = 3)**

| Speed Grade | Clock Rate | Access Time |
|-------------|------------|-------------|
| -5          | 200 MHz    | 5.0ns       |
| -6          | 166 MHz    | 5.0ns       |

**Table 2: Configuration Addressing**

| Architecture      | 32 Meg x 16          | 16 Meg x 32          |
|-------------------|----------------------|----------------------|
| Configuration     | 8 Meg x 16 x 4 banks | 4 Meg x 32 x 4 banks |
| Refresh count     | 8K                   | 8K                   |
| Row addressing    | 8K A[12:0]           | 8K A[12:0]           |
| Column addressing | 1K A[9:0]            | 512 A[8:0]           |

**Figure 1: 512Mb Mobile LPDDR Part Numbering**



## FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at [www.micron.com/decoder](http://www.micron.com/decoder).



## Contents

|  |    |
|--|----|
| General Description .....                                    | 8  |
| Functional Block Diagrams .....                              | 9  |
| Ball Assignments .....                                       | 11 |
| Ball Descriptions .....                                      | 13 |
| Package Dimensions .....                                     | 15 |
| Electrical Specifications .....                              | 17 |
| Electrical Specifications – I <sub>DD</sub> Parameters ..... | 21 |
| Electrical Specifications – AC Operating Conditions .....    | 27 |
| Output Drive Characteristics .....                           | 31 |
| Functional Description .....                                 | 34 |
| Commands .....   | 35 |
| DESELECT .....   | 36 |
| NO OPERATION .....   | 36 |
| LOAD MODE REGISTER .....                                     | 36 |
| ACTIVE .....   | 36 |
| READ .....   | 37 |
| WRITE .....  | 38 |
| PRECHARGE .....  | 39 |
| BURST TERMINATE .....  | 40 |
| AUTO REFRESH .....   | 40 |
| SELF REFRESH .....   | 41 |
| DEEP POWER-DOWN .....  | 41 |
| Truth Tables .....   | 42 |
| State Diagram .....  | 47 |
| Initialization .....   | 48 |
| Standard Mode Register .....                                 | 51 |
| Burst Length .....   | 52 |
| Burst Type .....   | 52 |
| CAS Latency .....  | 53 |
| Operating Mode .....   | 54 |
| Extended Mode Register .....                                 | 55 |
| Temperature-Compensated Self Refresh .....                   | 55 |
| Partial-Array Self Refresh .....                             | 56 |
| Output Drive Strength .....                                  | 56 |
| Status Read Register .....                                   | 57 |
| Bank/Row Activation .....                                    | 59 |
| READ Operation .....   | 60 |
| WRITE Operation .....  | 71 |
| PRECHARGE Operation .....                                    | 83 |
| Auto Precharge .....   | 83 |
| Concurrent Auto Precharge .....                              | 84 |
| AUTO REFRESH Operation .....                                 | 89 |
| SELF REFRESH Operation .....                                 | 90 |
| Power-Down .....   | 91 |
| Deep Power-Down .....  | 93 |
| Clock Change Frequency .....                                 | 95 |
| Revision History .....                                       | 96 |
| Rev. D – 02/14 .....   | 96 |
| Rev. C – 11/13 .....   | 96 |
| Rev. B – 03/13 .....   | 96 |



# 512Mb: x16, x32 Automotive LPDDR SDRAM Features

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Rev. A – 12/12 ..... 96

## List of Figures

|   |    |
|---|----|
| Figure 1: 512Mb Mobile LPDDR Part Numbering .....   | 2  |
| Figure 2: Functional Block Diagram (x16) .....  | 9  |
| Figure 3: Functional Block Diagram (x32) .....  | 10 |
| Figure 4: 60-Ball VFPGA – Top View, x16 only .....  | 11 |
| Figure 5: 90-Ball VFPGA – Top View, x32 only .....  | 12 |
| Figure 6: 60-Ball VFPGA (8mm x 9mm); Package Code: BF .....                               | 15 |
| Figure 7: 90-Ball VFPGA (8mm x 13mm); Package Codes: B5 (SAC105), BQ (SAC305) .....       | 16 |
| Figure 8: SSTL Clock Input .....  | 19 |
| Figure 9: Differential Clock Amplitude .....  | 19 |
| Figure 10: Typical Self Refresh Current vs. Temperature .....                             | 26 |
| Figure 11: ACTIVE Command .....   | 37 |
| Figure 12: READ Command .....   | 38 |
| Figure 13: WRITE Command .....  | 39 |
| Figure 14: PRECHARGE Command .....  | 40 |
| Figure 15: DEEP POWER-DOWN Command .....  | 41 |
| Figure 16: Simplified State Diagram .....   | 47 |
| Figure 17: Initialize and Load Mode Registers .....                                       | 49 |
| Figure 18: Alternate Initialization with CKE LOW .....                                    | 50 |
| Figure 19: Standard Mode Register Definition .....  | 51 |
| Figure 20: CAS Latency .....  | 54 |
| Figure 21: Extended Mode Register .....   | 55 |
| Figure 22: Status Read Register Timing .....  | 57 |
| Figure 23: Status Register Definition .....   | 58 |
| Figure 24: READ Burst .....   | 61 |
| Figure 25: Consecutive READ Bursts .....  | 62 |
| Figure 26: Nonconsecutive READ Bursts .....   | 63 |
| Figure 27: Random Read Accesses .....   | 64 |
| Figure 28: Terminating a READ Burst .....   | 65 |
| Figure 29: READ-to-WRITE .....  | 66 |
| Figure 30: READ-to-PRECHARGE .....  | 67 |
| Figure 31: Data Output Timing – $t_{DQSQ}$ , $t_{QH}$ , and Data Valid Window (x16) ..... | 68 |
| Figure 32: Data Output Timing – $t_{DQSQ}$ , $t_{QH}$ , and Data Valid Window (x32) ..... | 69 |
| Figure 33: Data Output Timing – $t_{AC}$ and $t_{DQSK}$ .....                             | 70 |
| Figure 34: Data Input Timing .....  | 72 |
| Figure 35: Write – DM Operation .....   | 73 |
| Figure 36: WRITE Burst .....  | 74 |
| Figure 37: Consecutive WRITE-to-WRITE .....   | 75 |
| Figure 38: Nonconsecutive WRITE-to-WRITE .....  | 75 |
| Figure 39: Random WRITE Cycles .....  | 76 |
| Figure 40: WRITE-to-READ – Uninterrupting .....   | 77 |
| Figure 41: WRITE-to-READ – Interrupting .....   | 78 |
| Figure 42: WRITE-to-READ – Odd Number of Data, Interrupting .....                         | 79 |
| Figure 43: WRITE-to-PRECHARGE – Uninterrupting .....                                      | 80 |
| Figure 44: WRITE-to-PRECHARGE – Interrupting .....  | 81 |
| Figure 45: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting .....                    | 82 |
| Figure 46: Bank Read – With Auto Precharge .....  | 85 |
| Figure 47: Bank Read – Without Auto Precharge .....                                       | 86 |
| Figure 48: Bank Write – With Auto Precharge .....   | 87 |
| Figure 49: Bank Write – Without Auto Precharge .....                                      | 88 |
| Figure 50: Auto Refresh Mode .....  | 89 |



Figure 51: Self Refresh Mode ..... 91  
Figure 52: Power-Down Entry (in Active or Precharge Mode) ..... 92  
Figure 53: Power-Down Mode (Active or Precharge) ..... 93  
Figure 54: Deep Power-Down Mode ..... 94  
Figure 55: Clock Stop Mode ..... 95

## List of Tables

|  |    |
|--|----|
| Table 1: Key Timing Parameters (CL = 3) .....  | 1  |
| Table 2: Configuration Addressing .....  | 2  |
| Table 3: Ball Descriptions .....   | 13 |
| Table 4: Absolute Maximum Ratings .....  | 17 |
| Table 5: AC/DC Electrical Characteristics and Operating Conditions .....             | 17 |
| Table 6: Capacitance (x16, x32) .....  | 20 |
| Table 7: I <sub>DD</sub> Specifications and Conditions, -40°C to +85°C (x16) .....   | 21 |
| Table 8: I <sub>DD</sub> Specifications and Conditions, -40°C to +85°C (x32) .....   | 22 |
| Table 9: I <sub>DD</sub> Specifications and Conditions, -40°C to +105°C (x16) .....  | 23 |
| Table 10: I <sub>DD</sub> Specifications and Conditions, -40°C to +105°C (x32) ..... | 24 |
| Table 11: I <sub>DD6</sub> Specifications and Conditions .....                       | 25 |
| Table 12: Electrical Characteristics and Recommended AC Operating Conditions .....   | 27 |
| Table 13: Target Output Drive Characteristics (Full Strength) .....                  | 31 |
| Table 14: Target Output Drive Characteristics (Three-Quarter Strength) .....         | 32 |
| Table 15: Target Output Drive Characteristics (One-Half Strength) .....              | 33 |
| Table 16: Truth Table – Commands .....   | 35 |
| Table 17: DM Operation Truth Table .....   | 36 |
| Table 18: Truth Table – Current State Bank <i>n</i> – Command to Bank <i>n</i> ..... | 42 |
| Table 19: Truth Table – Current State Bank <i>n</i> – Command to Bank <i>m</i> ..... | 44 |
| Table 20: Truth Table – CKE .....  | 46 |
| Table 21: Burst Definition Table .....   | 52 |



## General Description

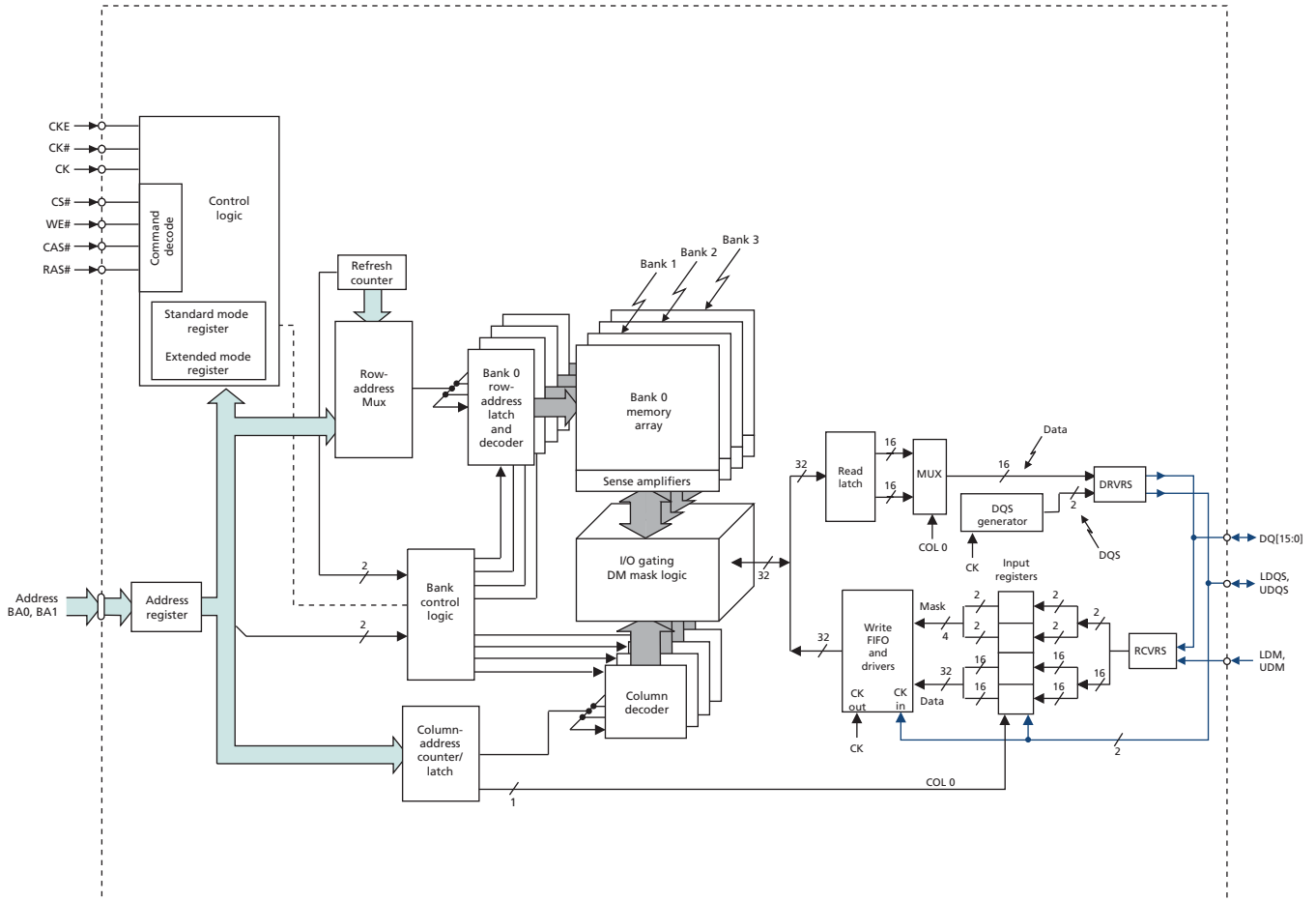
The 512Mb Mobile low-power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

**Note:**

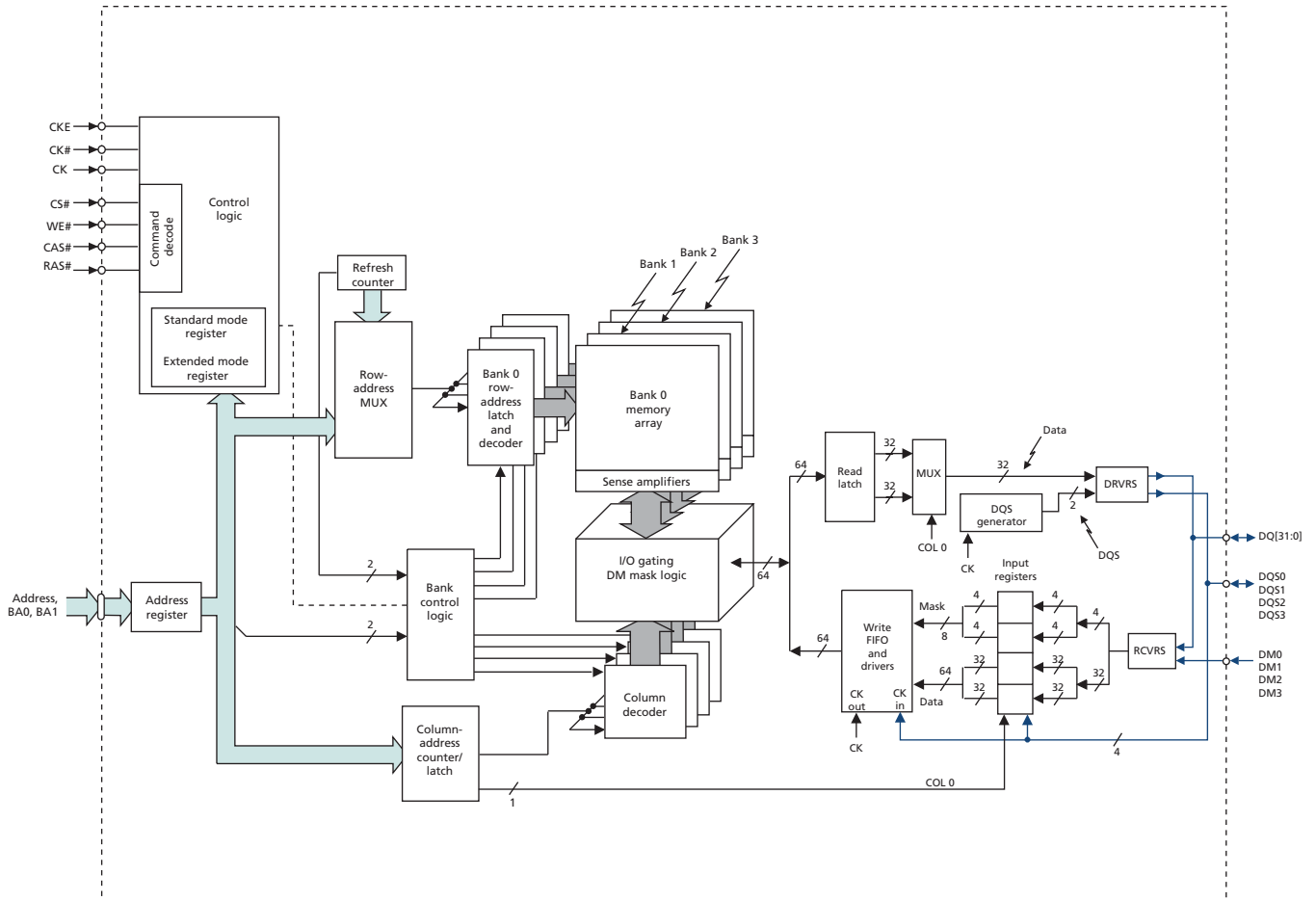
1. Throughout this data sheet, various figures and text refer to DQs as "DQ." DQ should be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]), DM refers to UDM and DQS refers to UDQS. The x32 is divided into 4 bytes. For DQ[7:0], DM refers to DM0 and DQS refers to DQS0. For DQ[15:8], DM refers to DM1 and DQS refers to DQS1. For DQ[23:16], DM refers to DM2 and DQS refers to DQS2. For DQ[31:24], DM refers to DM3 and DQS refers to DQS3.
2. Complete functionality is described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.

## Functional Block Diagrams

Figure 2: Functional Block Diagram (x16)

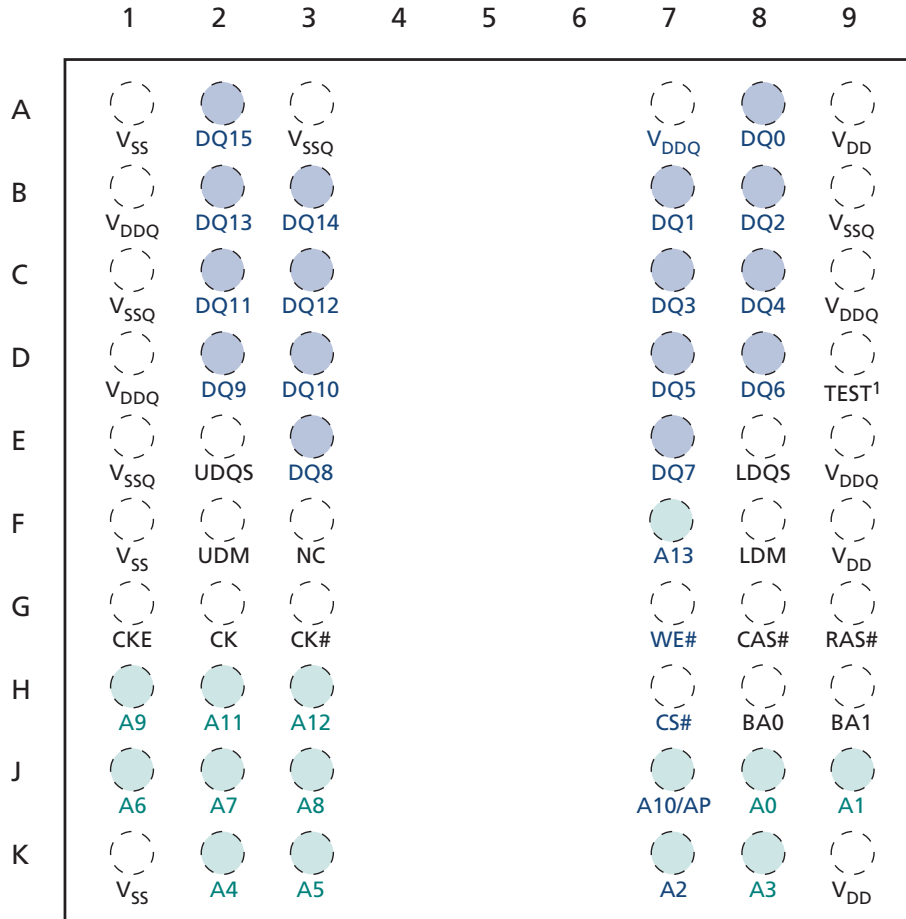


**Figure 3: Functional Block Diagram (x32)**



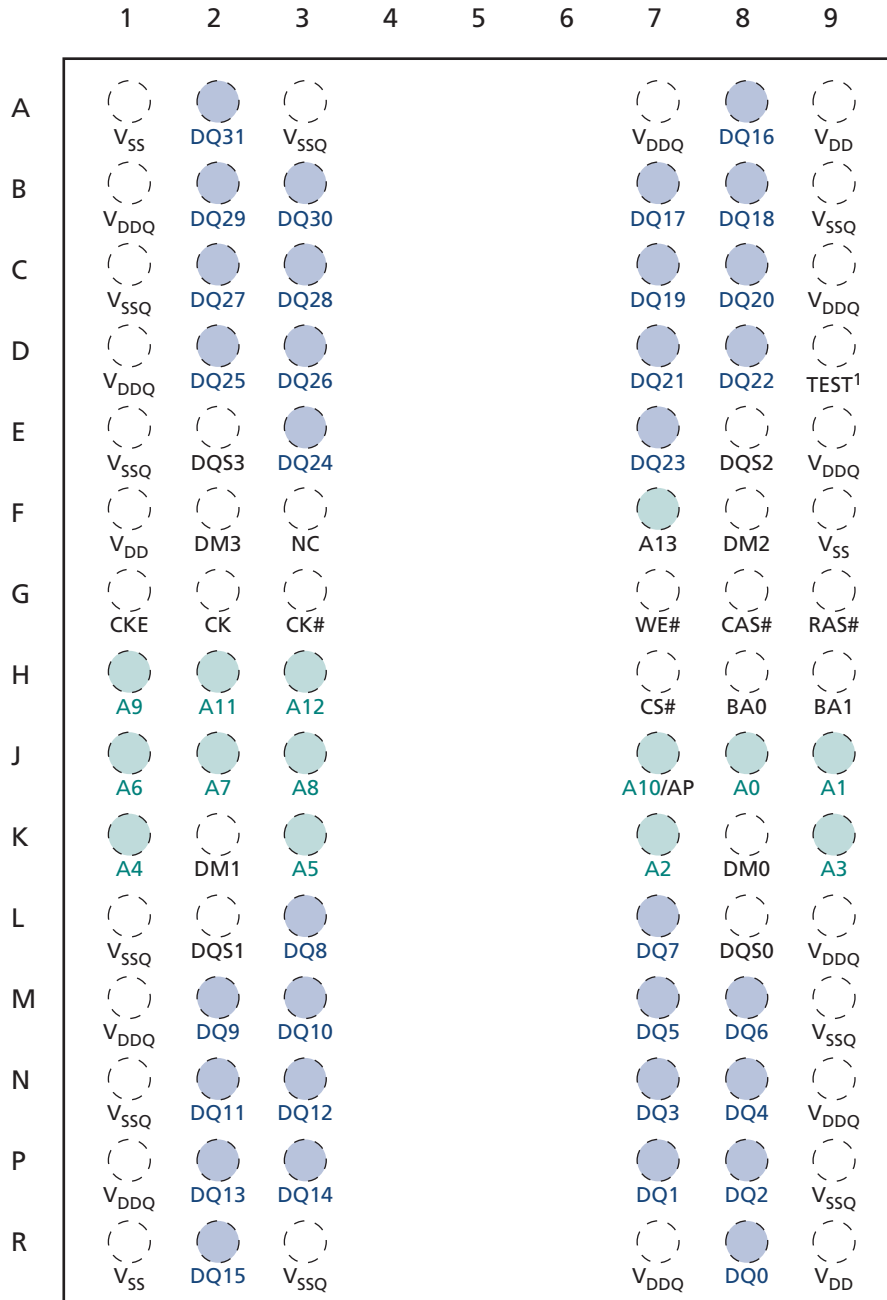
## Ball Assignments

Figure 4: 60-Ball VFBGA – Top View, x16 only



- Notes:
1. D9 is a test pin that must be tied to V<sub>SS</sub> or V<sub>SSQ</sub> in normal operations.
  2. Unused address pins become RFU.

Figure 5: 90-Ball VFBGA – Top View, x32 only



- Notes:
1. D9 is a test pin that must be tied to V<sub>SS</sub> or V<sub>SSQ</sub> in normal operations.
  2. Unused address pins become RFU.

### Ball Descriptions

The ball descriptions table is a comprehensive list of all possible balls for all supported packages. Not all balls listed are supported for a given package.

**Table 3: Ball Descriptions**

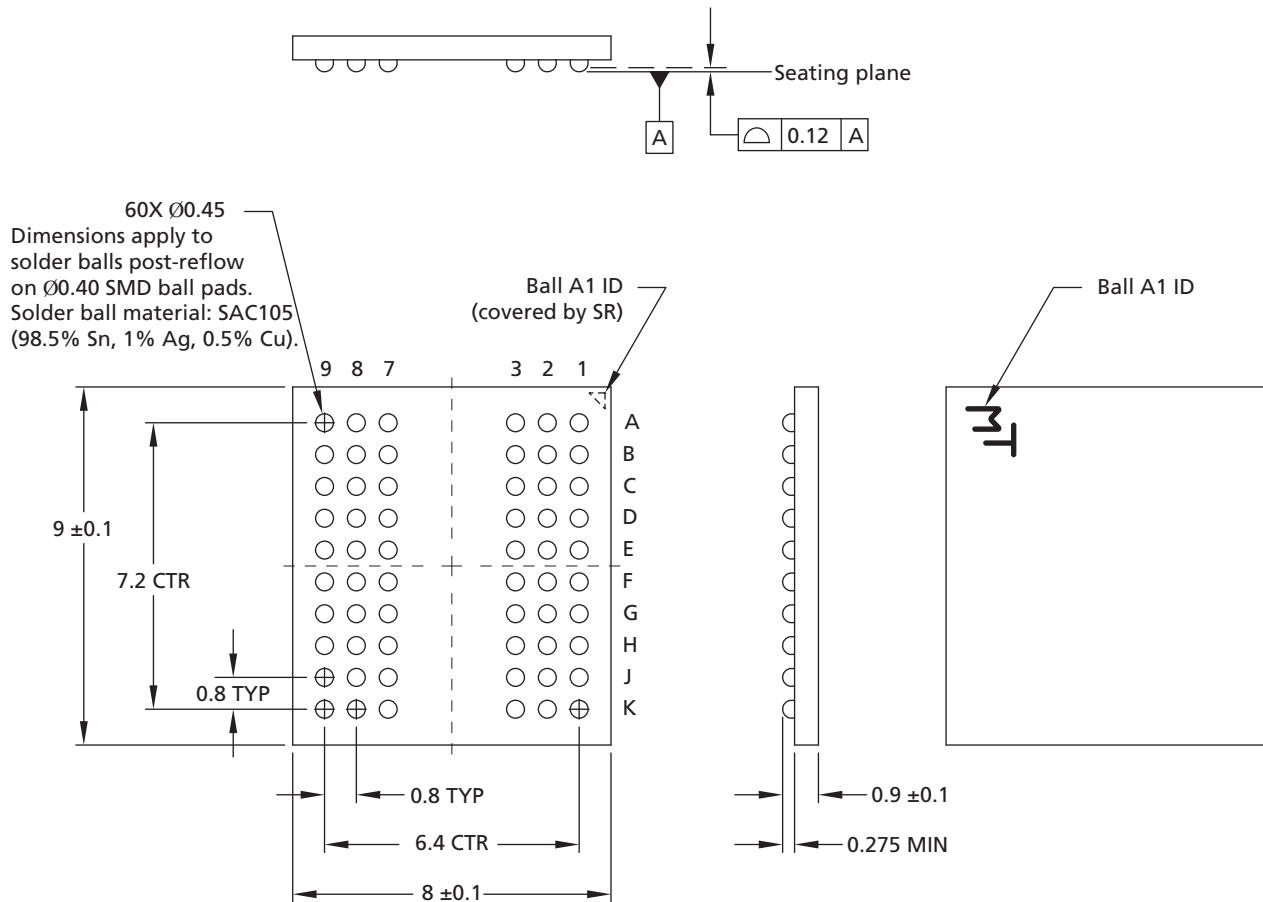
| Symbol                             | Type             | Description   |
|------------------------------------|------------------|---|
| CK, CK#                            | Input            | Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).  |
| CKE<br>CKE0, CKE1                  | Input            | Clock enable: CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes. CKE0 is used for a single LPDDR product. CKE1 is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.  |
| CS#<br>CS0#, CS1#                  | Input            | Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. CS0# is used for a single LPDDR product. CS1# is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.  |
| RAS#, CAS#, WE#                    | Input            | Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.  |
| UDM, LDM (x16)<br>DM[3:0] (x32)    | Input            | Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls.  |
| BA0, BA1                           | Input            | Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is loaded during a LOAD MODE REGISTER command.  |
| A[13:0]                            | Input            | Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. The maximum address range is dependent upon configuration. Unused address balls become RFU. |
| TEST                               | Input            | Test pin: Must be tied to V <sub>SS</sub> or V <sub>SSQ</sub> in normal operations.   |
| DQ[15:0] (x16)<br>DQ[31:0] (x32)   | Input/<br>output | Data input/output: Data bus for x16 and x32.  |
| LDQS, UDQS (x16)<br>DQS[3:0] (x32) | Input/<br>output | Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned in write data. It is used to capture data.  |
| TQ                                 | Output           | Temperature sensor output: TQ HIGH when LPDDR T <sub>J</sub> exceeds 85°C.  |
| V <sub>DDQ</sub>                   | Supply           | DQ power supply.  |

**Table 3: Ball Descriptions (Continued)**

| Symbol           | Type   | Description  |
|------------------|--------|--|
| V <sub>SSQ</sub> | Supply | DQ ground.   |
| V <sub>DD</sub>  | Supply | Power supply.  |
| V <sub>SS</sub>  | Supply | Ground.  |
| NC               | –      | No connect: May be left unconnected.   |
| RFU              | –      | Reserved for future use. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details. |

## Package Dimensions

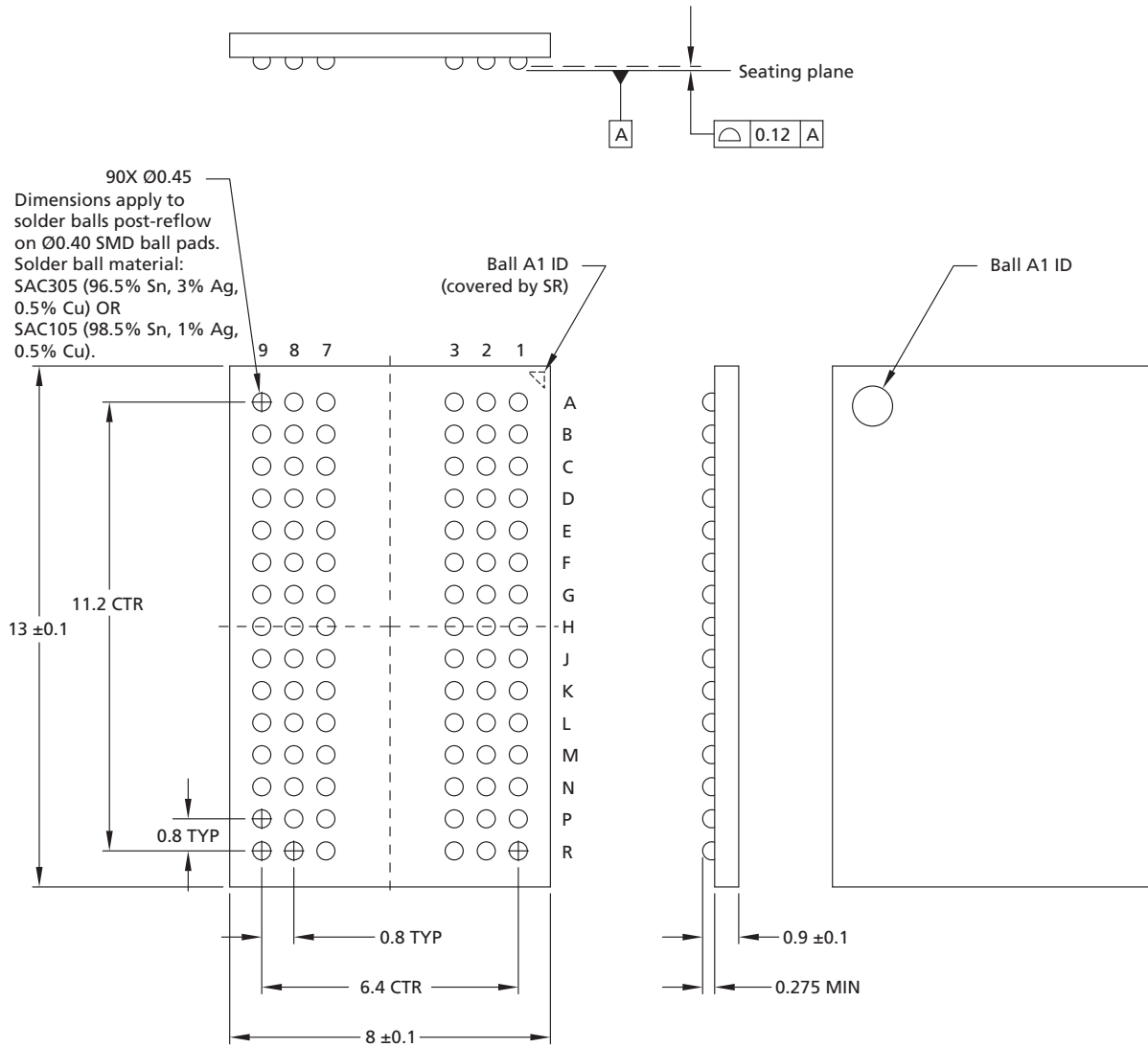
Figure 6: 60-Ball VFBGA (8mm x 9mm); Package Code: BF



Note: 1. All dimensions are in millimeters.



**Figure 7: 90-Ball VFBGA (8mm x 13mm); Package Codes: B5 (SAC105), BQ (SAC305)**



Note: 1. All dimensions are in millimeters.

## Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 4: Absolute Maximum Ratings**

Note 1 applies to all parameters in this table

| Parameter  | Symbol           | Min  | Max   | Unit |
|--|------------------|------|---|------|
| $V_{DD}/V_{DDQ}$ supply voltage relative to $V_{SS}$ | $V_{DD}/V_{DDQ}$ | -1.0 | 2.4   | V    |
| Voltage on any pin relative to $V_{SS}$              | $V_{IN}$         | -0.5 | 2.4 or ( $V_{DDQ} + 0.3V$ ),<br>whichever is less | V    |
| Storage temperature (plastic)                        | $T_{STG}$        | -55  | 150   | °C   |

Note: 1.  $V_{DD}$  and  $V_{DDQ}$  must be within 300mV of each other at all times.  $V_{DDQ}$  must not exceed  $V_{DD}$ .

**Table 5: AC/DC Electrical Characteristics and Operating Conditions**

Notes 1–5 apply to all parameters/conditions in this table;  $V_{DD}/V_{DDQ} = 1.70\text{--}1.95V$

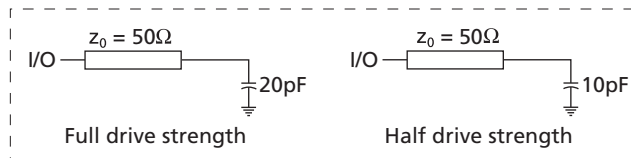
| Parameter/Condition   | Symbol       | Min                  | Max                  | Unit    | Notes      |
|---|--------------|----------------------|----------------------|---------|------------|
| Supply voltage  | $V_{DD}$     | 1.70                 | 1.95                 | V       | 6, 7       |
| I/O supply voltage  | $V_{DDQ}$    | 1.70                 | 1.95                 | V       | 6, 7       |
| <b>Address and command inputs</b>   |              |                      |                      |         |            |
| Input voltage high  | $V_{IH}$     | $0.8 \times V_{DDQ}$ | $V_{DDQ} + 0.3$      | V       | 8, 9       |
| Input voltage low   | $V_{IL}$     | -0.3                 | $0.2 \times V_{DDQ}$ | V       | 8, 9       |
| <b>Clock inputs (CK, CK#)</b>   |              |                      |                      |         |            |
| DC input voltage  | $V_{IN}$     | -0.3                 | $V_{DDQ} + 0.3$      | V       | 10         |
| DC input differential voltage   | $V_{ID(DC)}$ | $0.4 \times V_{DDQ}$ | $V_{DDQ} + 0.6$      | V       | 10, 11, 14 |
| AC input differential voltage   | $V_{ID(AC)}$ | $0.6 \times V_{DDQ}$ | $V_{DDQ} + 0.6$      | V       | 10, 11, 14 |
| AC differential crossing voltage  | $V_{IX}$     | $0.4 \times V_{DDQ}$ | $0.6 \times V_{DDQ}$ | V       | 10, 12     |
| <b>Data inputs</b>  |              |                      |                      |         |            |
| DC input high voltage   | $V_{IH(DC)}$ | $0.7 \times V_{DDQ}$ | $V_{DDQ} + 0.3$      | V       | 8, 9, 13   |
| DC input low voltage  | $V_{IL(DC)}$ | -0.3                 | $0.3 \times V_{DDQ}$ | V       | 8, 9, 13   |
| AC input high voltage   | $V_{IH(AC)}$ | $0.8 \times V_{DDQ}$ | $V_{DDQ} + 0.3$      | V       | 8, 9, 13   |
| AC input low voltage  | $V_{IL(AC)}$ | -0.3                 | $0.2 \times V_{DDQ}$ | V       | 8, 9, 13   |
| <b>Data outputs</b>   |              |                      |                      |         |            |
| DC output high voltage: Logic 1 ( $I_{OH} = -0.1mA$ )   | $V_{OH}$     | $0.9 \times V_{DDQ}$ | -                    | V       |            |
| DC output low voltage: Logic 0 ( $I_{OL} = 0.1mA$ )   | $V_{OL}$     | -                    | $0.1 \times V_{DDQ}$ | V       |            |
| <b>Leakage current</b>  |              |                      |                      |         |            |
| Input leakage current<br>Any input $0V \leq V_{IN} \leq V_{DD}$<br>(All other pins not under test = 0V) | $I_I$        | -1                   | 1                    | $\mu A$ |            |

**Table 5: AC/DC Electrical Characteristics and Operating Conditions (Continued)**

Notes 1–5 apply to all parameters/conditions in this table;  $V_{DD}/V_{DDQ} = 1.70\text{--}1.95V$

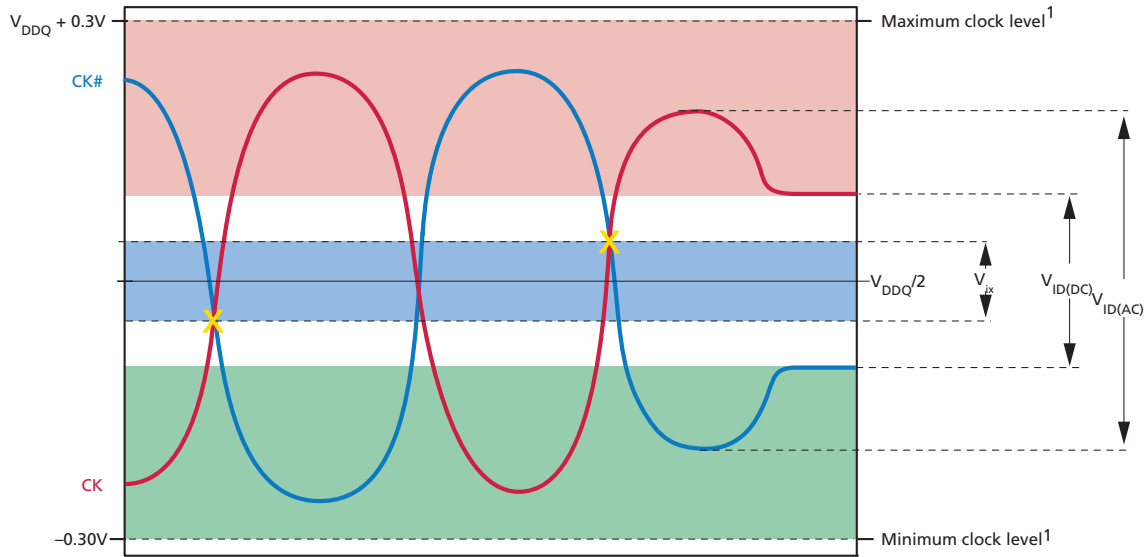
| Parameter/Condition  | Symbol   | Min | Max  | Unit        | Notes |
|--|----------|-----|------|-------------|-------|
| Output leakage current<br>(DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ ) | $I_{OZ}$ | -5  | 5    | $\mu A$     |       |
| <b>Operating temperature</b>   |          |     |      |             |       |
| Industrial   | $T_A$    | -40 | +85  | $^{\circ}C$ |       |
| Automotive   | $T_A$    | -40 | +105 | $^{\circ}C$ |       |

- Notes:
- All voltages referenced to  $V_{SS}$ .
  - All parameters assume proper device initialization.
  - Tests for AC timing,  $I_{DD}$ , and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
  - Outputs measured with equivalent load; transmission line delay is assumed to be very small:

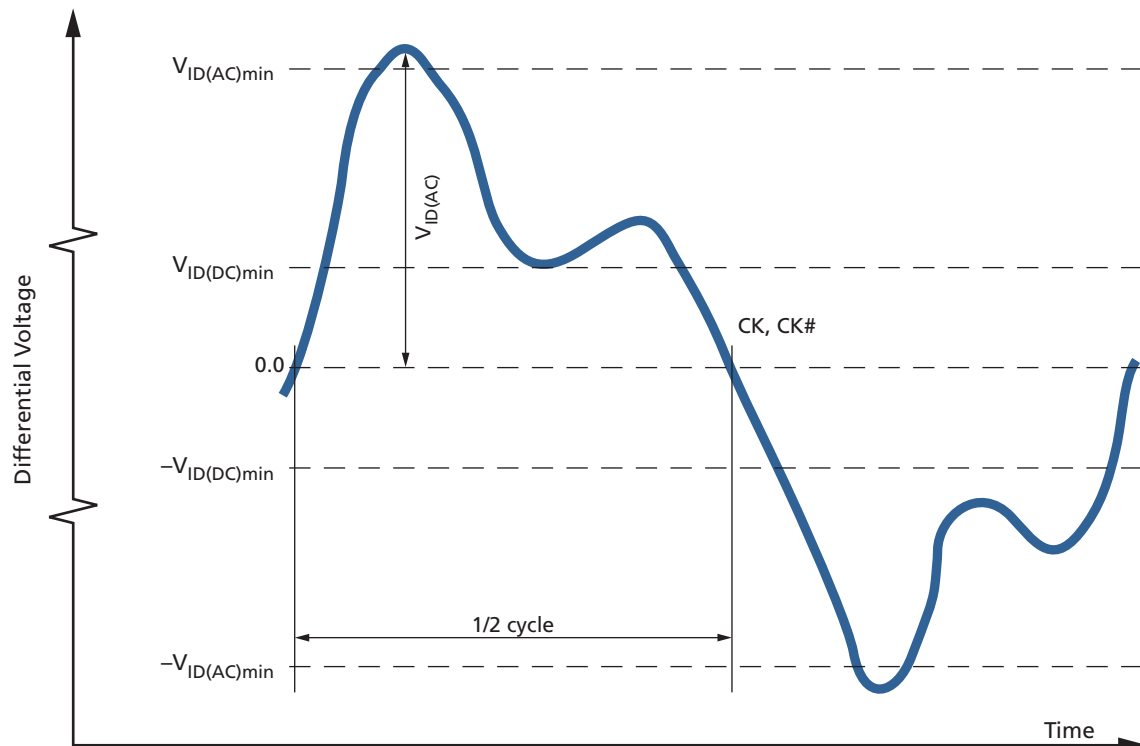


- Timing and  $I_{DD}$  tests may use a  $V_{IL}$ -to- $V_{IH}$  swing of up to 1.5V in the test environment, but input timing is still referenced to  $V_{DDQ}/2$  (or to the crossing point for CK/CK#). The output timing reference voltage level is  $V_{DDQ}/2$ .
- Any positive glitch must be less than one-third of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than one-third of the clock cycle and not exceed either -150mV or +1.6V, whichever is more positive.
- $V_{DD}$  and  $V_{DDQ}$  must track each other and  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .
- To maintain a valid level, the transitioning edge of the input must:
  - Sustain a constant slew rate from the current AC level through to the target AC level,  $V_{IL(AC)}$  Or  $V_{IH(AC)}$ .
  - Reach at least the target AC level.
  - After the AC target level is reached, continue to maintain at least the target DC level,  $V_{IL(DC)}$  or  $V_{IH(DC)}$ .
- $V_{IH}$  overshoot:  $V_{IHmax} = V_{DDQ} + 1.0V$  for a pulse width  $\leq 3ns$  and the pulse width cannot be greater than one-third of the cycle rate.  $V_{IL}$  undershoot:  $V_{ILmin} = -1.0V$  for a pulse width  $\leq 3ns$  and the pulse width cannot be greater than one-third of the cycle rate.
- CK and CK# input slew rate must be  $\geq 1 V/ns$  (2 V/ns if measured differentially).
- $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on CK#.
- The value of  $V_{IX}$  is expected to equal  $V_{DDQ}/2$  of the transmitting device and must track variations in the DC level of the same.
- DQ and DM input slew rates must not deviate from DQS by more than 10%. 50ps must be added to  $t_{DS}$  and  $t_{DH}$  for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.
- $V_{ID(AC)}$  specifies the input differential voltage  $|VTR - VCP|$  required for switching, where VTR is the true input level of CK and VCP is the complementary input level of CK (CK#).

**Figure 8: SSTL Clock Input**



**Figure 9: Differential Clock Amplitude**



**Table 6: Capacitance (x16, x32)**

Note 1 applies to all the parameters in this table

| Parameter                                    | Symbol    | Min | Max  | Unit | Notes |
|--|-----------|-----|------|------|-------|
| Input capacitance: CK, CK#                   | $C_{CK}$  | 1.5 | 3.0  | pF   |       |
| Delta input capacitance: CK, CK#             | $C_{DCK}$ | –   | 0.25 | pF   | 2     |
| Input capacitance: command and address       | $C_I$     | 1.5 | 3.0  | pF   |       |
| Delta input capacitance: command and address | $C_{DI}$  | –   | 0.5  | pF   | 2     |
| Input/output capacitance: DQ, DQS, DM        | $C_{IO}$  | 2.0 | 4.5  | pF   |       |
| Delta input/output capacitance: DQ, DQS, DM  | $C_{DIO}$ | –   | 0.5  | pF   | 3     |

- Notes:
1. This parameter is sampled.  $V_{DD}/V_{DDQ} = 1.70\text{--}1.95V$ ,  $f = 100\text{ MHz}$ ,  $T_A = 25^\circ C$ ,  $V_{OUT(DC)} = V_{DDQ}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
  2. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
  3. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

## Electrical Specifications – I<sub>DD</sub> Parameters

**Table 7: I<sub>DD</sub> Specifications and Conditions, –40°C to +85°C (x16)**

 Notes 1–5 apply to all the parameters/conditions in this table; V<sub>DD</sub>/V<sub>DDQ</sub> = 1.70–1.95V

| Parameter/Condition  | Symbol                   | Max               |     | Unit | Notes |        |
|--|--------------------------|-------------------|-----|------|-------|--------|
|  |                          | -5                | -6  |      |       |        |
| Operating 1 bank active precharge current: $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable | I <sub>DD0</sub>         | 70                | 60  | mA   | 6     |        |
| Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD2P</sub>        | 300               | 300 | μA   | 7, 8  |        |
| Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD2PS</sub>       | 300               | 300 | μA   | 7     |        |
| Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD2N</sub>        | 15                | 15  | mA   | 9     |        |
| Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD2NS</sub>       | 8                 | 8   | mA   | 9     |        |
| Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD3P</sub>        | 3                 | 3   | mA   | 8     |        |
| Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD3PS</sub>       | 2                 | 2   | mA   |       |        |
| Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD3N</sub>        | 15                | 15  | mA   | 6     |        |
| Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD3NS</sub>       | 8                 | 8   | mA   | 6     |        |
| Operating burst read: 1 bank active; BL = 4; $t_{CK} = t_{CK}(\text{MIN})$ ; Continuous READ bursts; I <sub>out</sub> = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst                             | I <sub>DD4R</sub>        | 115               | 105 | mA   | 6     |        |
| Operating burst write: 1 bank active; BL = 4; $t_{CK} = t_{CK}(\text{MIN})$ ; Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst  | I <sub>DD4W</sub>        | 115               | 105 | mA   | 6     |        |
| Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable  | $t_{RFC} = 138\text{ns}$ | I <sub>DD5</sub>  | 95  | 95   | mA    | 10     |
|  | $t_{RFC} = t_{REFI}$     | I <sub>DD5A</sub> | 3   | 3    | mA    | 10, 11 |
| Deep power-down current: Address and control balls are stable; Data bus inputs are stable  | I <sub>DD8</sub>         | 10                | 10  | μA   | 7, 13 |        |

**Table 8: I<sub>DD</sub> Specifications and Conditions, –40°C to +85°C (x32)**

 Notes 1–5 apply to all the parameters/conditions in this table; V<sub>DD</sub>/V<sub>DDQ</sub> = 1.70–1.95V

| Parameter/Condition  | Symbol                   | Max               |     | Unit | Notes |        |
|--|--------------------------|-------------------|-----|------|-------|--------|
|  |                          | -5                | -6  |      |       |        |
| Operating 1 bank active precharge current: $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable | I <sub>DD0</sub>         | 70                | 60  | mA   | 6     |        |
| Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD2P</sub>        | 300               | 300 | μA   | 7, 8  |        |
| Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD2PS</sub>       | 300               | 300 | μA   | 7     |        |
| Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD2N</sub>        | 15                | 15  | mA   | 9     |        |
| Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD2NS</sub>       | 8                 | 8   | mA   | 9     |        |
| Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD3P</sub>        | 3                 | 3   | mA   | 8     |        |
| Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD3PS</sub>       | 2                 | 2   | mA   |       |        |
| Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD3N</sub>        | 15                | 15  | mA   | 6     |        |
| Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD3NS</sub>       | 8                 | 8   | mA   | 6     |        |
| Operating burst read: 1 bank active; BL = 4; CL = 3; $t_{CK} = t_{CK}(\text{MIN})$ ; Continuous READ bursts; I <sub>out</sub> = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst                     | I <sub>DD4R</sub>        | 115               | 105 | mA   | 6     |        |
| Operating burst write: One bank active; BL = 4; $t_{CK} = t_{CK}(\text{MIN})$ ; Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst  | I <sub>DD4W</sub>        | 115               | 105 | mA   | 6     |        |
| Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable  | $t_{RFC} = 138\text{ns}$ | I <sub>DD5</sub>  | 95  | 95   | mA    | 10     |
|  | $t_{RFC} = t_{REFI}$     | I <sub>DD5A</sub> | 3   | 3    | mA    | 10, 11 |
| Deep power-down current: Address and control pins are stable; Data bus inputs are stable   | I <sub>DD8</sub>         | 10                | 10  | μA   | 7, 13 |        |

**Table 9: I<sub>DD</sub> Specifications and Conditions, –40°C to +105°C (x16)**

 Notes 1–5 apply to all the parameters/conditions in this table; V<sub>DD</sub>/V<sub>DDQ</sub> = 1.70–1.95V

| Parameter/Condition  | Symbol                   | Max               |     | Unit | Notes |        |
|--|--------------------------|-------------------|-----|------|-------|--------|
|  |                          | -5                | -6  |      |       |        |
| Operating 1 bank active precharge current: $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable | I <sub>DD0</sub>         | 70                | 60  | mA   | 6     |        |
| Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD2P</sub>        | 600               | 600 | μA   | 7, 8  |        |
| Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD2PS</sub>       | 600               | 600 | μA   | 7     |        |
| Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD2N</sub>        | 16                | 16  | mA   | 9     |        |
| Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD2NS</sub>       | 9                 | 9   | mA   | 9     |        |
| Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD3P</sub>        | 4                 | 4   | mA   | 8     |        |
| Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD3PS</sub>       | 3                 | 3   | mA   |       |        |
| Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD3N</sub>        | 16                | 16  | mA   | 6     |        |
| Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD3NS</sub>       | 9                 | 9   | mA   | 6     |        |
| Operating burst read: 1 bank active; BL = 4; $t_{CK} = t_{CK}(\text{MIN})$ ; Continuous READ bursts; I <sub>out</sub> = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst                             | I <sub>DD4R</sub>        | 115               | 105 | mA   | 6     |        |
| Operating burst write: 1 bank active; BL = 4; $t_{CK} = t_{CK}(\text{MIN})$ ; Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst  | I <sub>DD4W</sub>        | 115               | 105 | mA   | 6     |        |
| Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable  | $t_{RFC} = 138\text{ns}$ | I <sub>DD5</sub>  | 95  | 95   | mA    | 10     |
|  | $t_{RFC} = t_{REFI}$     | I <sub>DD5A</sub> | 8   | 8    | mA    | 10, 11 |
| Deep power-down current: Address and control balls are stable; Data bus inputs are stable  | I <sub>DD8</sub>         | 15                | 15  | μA   | 7, 13 |        |



**Table 10: I<sub>DD</sub> Specifications and Conditions, –40°C to +105°C (x32)**

 Notes 1–5 apply to all the parameters/conditions in this table; V<sub>DD</sub>/V<sub>DDQ</sub> = 1.70–1.95V

| Parameter/Condition  | Symbol                   | Max               |     | Unit | Notes |        |
|--|--------------------------|-------------------|-----|------|-------|--------|
|  |                          | -5                | -6  |      |       |        |
| Operating 1 bank active precharge current: $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable | I <sub>DD0</sub>         | 70                | 60  | mA   | 6     |        |
| Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD2P</sub>        | 600               | 600 | μA   | 7, 8  |        |
| Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD2PS</sub>       | 600               | 600 | μA   | 7     |        |
| Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD2N</sub>        | 16                | 16  | mA   | 9     |        |
| Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD2NS</sub>       | 9                 | 9   | mA   | 9     |        |
| Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD3P</sub>        | 4                 | 4   | mA   | 8     |        |
| Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD3PS</sub>       | 3                 | 3   | mA   |       |        |
| Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs are switching; Data bus inputs are stable   | I <sub>DD3N</sub>        | 16                | 16  | mA   | 6     |        |
| Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable  | I <sub>DD3NS</sub>       | 9                 | 9   | mA   | 6     |        |
| Operating burst read: 1 bank active; BL = 4; CL = 3; $t_{CK} = t_{CK}(\text{MIN})$ ; Continuous READ bursts; I <sub>out</sub> = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst                     | I <sub>DD4R</sub>        | 115               | 105 | mA   | 6     |        |
| Operating burst write: One bank active; BL = 4; $t_{CK} = t_{CK}(\text{MIN})$ ; Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst  | I <sub>DD4W</sub>        | 115               | 105 | mA   | 6     |        |
| Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable  | $t_{RFC} = 138\text{ns}$ | I <sub>DD5</sub>  | 95  | 95   | mA    | 10     |
|  | $t_{RFC} = t_{REFI}$     | I <sub>DD5A</sub> | 8   | 8    | mA    | 10, 11 |
| Deep power-down current: Address and control pins are stable; Data bus inputs are stable   | I <sub>DD8</sub>         | 15                | 15  | μA   | 7, 13 |        |

**Table 11: I<sub>DD6</sub> Specifications and Conditions**

Notes 1–5, 7, and 12 apply to all the parameters/conditions in this table; V<sub>DD</sub>/V<sub>DDQ</sub> = 1.70–1.95V

| Parameter/Condition   |                   | Symbol           | Standard          | Unit |
|---|-------------------|------------------|-------------------|------|
| Self refresh<br>CKE = LOW; t <sup>CK</sup> = t <sup>CK</sup> (MIN); Address and control inputs are stable; Data bus inputs are stable | Full array, 105°C | I <sub>DD6</sub> | n/a <sup>14</sup> | μA   |
|   | Full array, 85°C  |                  | 700               | μA   |
|   | Full array, 45°C  |                  | 390               | μA   |
|   | 1/2 array, 85°C   |                  | 520               | μA   |
|   | 1/2 array, 45°C   |                  | 310               | μA   |
|   | 1/4 array, 85°C   |                  | 430               | μA   |
|   | 1/4 array, 45°C   |                  | 275               | μA   |
|   | 1/8 array, 85°C   |                  | 430               | μA   |
|   | 1/8 array, 45°C   |                  | 275               | μA   |
|   | 1/16 array, 85°C  |                  | 375               | μA   |
|   | 1/16 array, 45°C  |                  | 250               | μA   |

- Notes:
1. All voltages referenced to V<sub>SS</sub>.
  2. Tests for I<sub>DD</sub> characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
  3. Timing and I<sub>DD</sub> tests may use a V<sub>IL</sub>-to-V<sub>IH</sub> swing of up to 1.5V in the test environment, but input timing is still referenced to V<sub>DDQ/2</sub> (or to the crossing point for CK/CK#). The output timing reference voltage level is V<sub>DDQ/2</sub>.
  4. I<sub>DD</sub> is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time with the outputs open.
  5. I<sub>DD</sub> specifications are tested after the device is properly initialized and values are averaged at the defined cycle rate.
  6. MIN (t<sup>RC</sup> or t<sup>RFC</sup>) for I<sub>DD</sub> measurements is the smallest multiple of t<sup>CK</sup> that meets the minimum absolute value for the respective parameter. t<sup>RASmax</sup> for I<sub>DD</sub> measurements is the largest multiple of t<sup>CK</sup> that meets the maximum absolute value for t<sup>RAS</sup>.
  7. Measurement is taken 500ms after entering into this operating mode to provide settling time for the tester.
  8. V<sub>DD</sub> must not vary more than 4% if CKE is not active while any bank is active.
  9. I<sub>DD2N</sub> specifies DQ, DQS, and DM to be driven to a valid high or low logic level.
  10. CKE must be active (HIGH) during the entire time a REFRESH command is executed. From the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge until t<sup>RFC</sup> later.
  11. This limit is a nominal value and does not result in a fail. CKE is HIGH during REFRESH command period (t<sup>RFC</sup> (MIN)) else CKE is LOW (for example, during standby).
  12. Values for I<sub>DD6</sub> 85°C are guaranteed for the entire temperature range. All other I<sub>DD6</sub> values are estimated.
  13. Typical values at 25°C, not a maximum value.
  14. Self refresh is not supported for AT (85°C to 105°C) operation.