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Mobile DDR SDRAM

MT46H8M16LF – 2 Meg x 16 x 4 Banks

For the latest data sheet, refer to Micron's Web site: www.micron.com

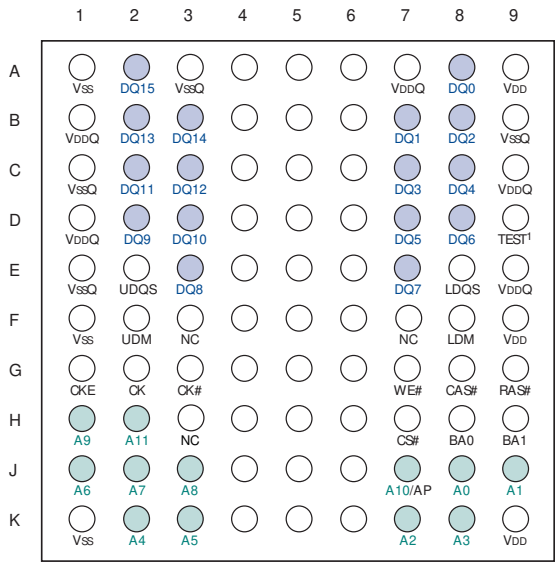
Features

- VDD/VDDQ = +1.8V ±0.1V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data–one mask per byte
- Programmable burst lengths: 2, 4, or 8
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- On-chip temperature sensor to control refresh rate
- Partial array self refresh (PASR)
- Selectable output drive (DS)
- Clock stop capability

Options

Options	Marking
• VDD/VDDQ	
– 1.8V/1.8V	H
• Configuration	
– 8 Meg x 16 (2 Meg x 16 x 4 banks)	8M16
• Plastic package	
– 60-Ball VFBGA (lead-free) 8mm x 10mm	CF
• Timing – cycle time	
– 7.5ns @ CL = 3	-75
– 10ns @ CL = 3	-10
• Operating temperature range	
– Commercial (0° to +70°C)	None
– Industrial (-40°C to +85°C)	IT

Figure 1: 60-Ball VFBGA Assignment (Top View)



Notes: 1. D9 should be connected to VSS or VSSQ in normal operations.

Table 1: Configuration Addressing

Architecture	8 Meg x 16
Configuration	2 Meg x 16 x 4
Refresh count	4K
Row addressing	4K (A0–A11)
Bank addressing	4 (BA0, BA1)
Column addressing	512K (A0–A8)

Table 2: Key Timing Parameters

Speed Grade	Clock Rate		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-75	83 MHz	133 MHz	6.5ns	6.0ns
-10	67 MHz	104 MHz	7.0ns	7.0ns

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Table 3: 128Mb Mobile DDR SDRAM Part Numbers

Part Number	Configuration	I/O Drive Level	Temperature Option
MT46H8M16LFCF-75	8 Meg x 16	Programmable drive	0°C to +70°C
MT46H8M16LFCF-75IT	8 Meg x 16	Programmable drive	-40°C to +85°C
MT46H8M16LFCF-10	8 Meg x 16	Programmable drive	0°C to +70°C
MT46H8M16LFCF-10IT	8 Meg x 16	Programmable drive	-40°C to +85°C

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's new FBGA Part Marking Decoder makes it easier to understand this part marking. Visit the Web site at www.micron.com/decoder.

General Description

The 128Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,271,728 bits. It is internally configured as a quad-bank DRAM. Each of the 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

The 128Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 128Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Mobile DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The 128Mb Mobile DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

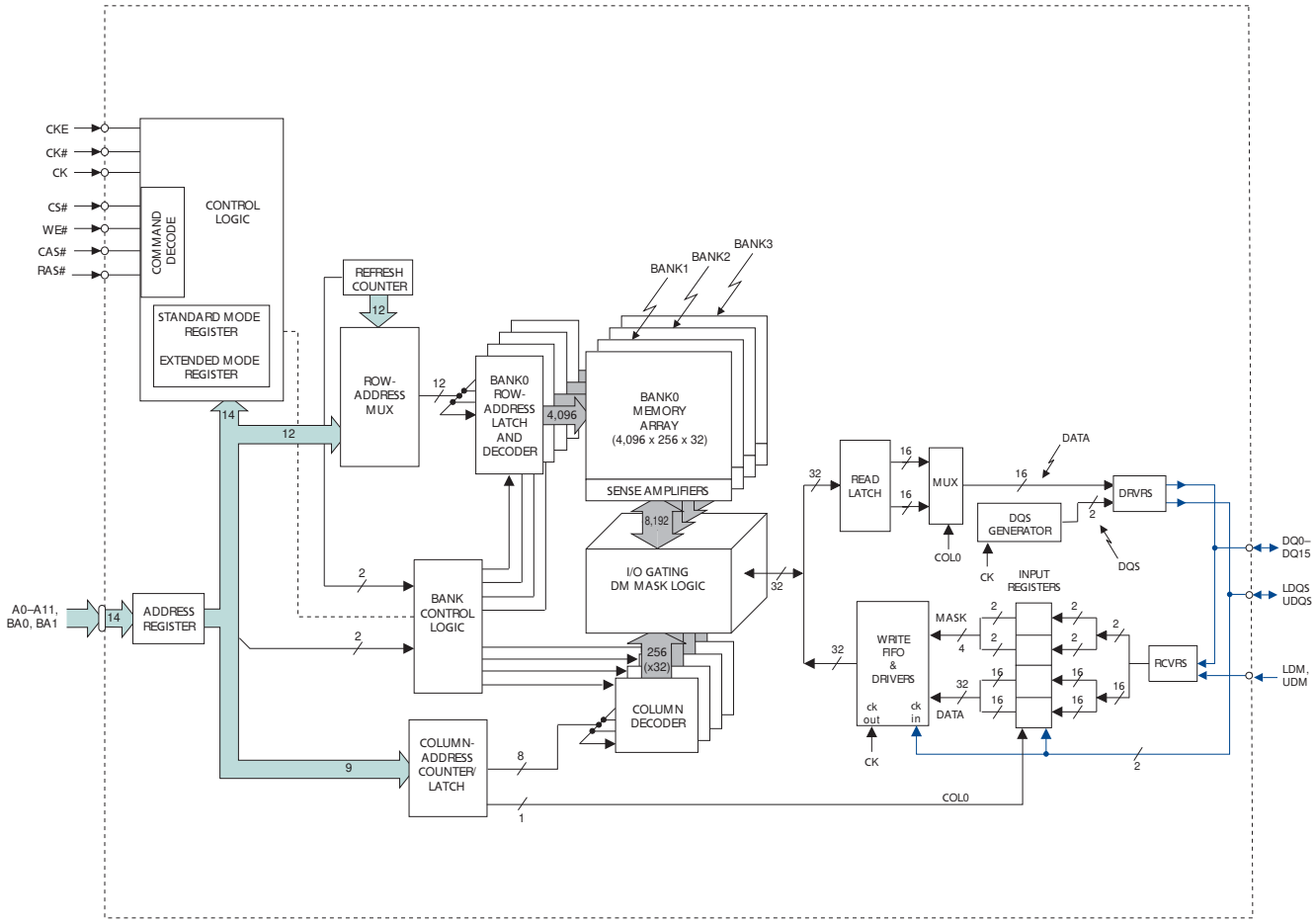
The Mobile DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of Mobile DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto-refresh mode is provided, along with a power saving power-down mode. Self refresh mode offers temperature compensation through an on-chip temperature sensor and partial array self refresh, which allow users to achieve additional power saving. The temperature sensor is enabled by default and the partial array self refresh can be programmed through the extended mode register.

Notes:
1. Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes—the lower byte and upper byte. For the lower byte (DQ0–DQ7) DM refers to LDM and DQS refers to LDQS; and for the upper byte (DQ8–DQ15) DM refers to UDM and DQS refers to UDQS.
2. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.

Figure 2: Functional Block Diagram (8 Meg x 16)



Ball Description

Table 4: 60-Ball VFBGA Ball Description

Ball Numbers	Symbol	Type	Description
G2, G3	CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
G1	CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW allows PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions expect SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
H7	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
G9, G8, G7	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F2, F8	UDM, LDM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x16, LDM is DM for DQ0–DQ7 and UDM is DM for DQ8–DQ15.
H8, H9	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
J8, J9, K7, K8, K2, K3, J1, J2, J3, J7, H1, H2	A0–A11	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A8, B7, B8, C7, C8, D7, D8, E7 E3, D2, D3, C2, C3, B2, B3, A2	DQ0–DQ15	I/O	Data input/output: Data bus for x16.
E2, E7	UDQS, LDQS	I/O	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data.
A7, B1, C9, D1, E9	$V_{DD}Q$	Supply	DQ power supply.
A3, B9, C1, E1	$V_{SS}Q$	Supply	DQ ground: Isolated on the die for improved noise immunity.
A9, F9, K9	V_{DD}	Supply	Power supply.
A1, F1, K1	V_{SS}	Supply	Ground.
F3, F7, H3	NC	Input	No connect. These pins should be left unconnected.
D9	TEST	Input	Test pin: Must be tied to V_{SS} or $V_{SS}Q$ in normal operations.

Functional Description

The 128Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,271,728-bits. It is internally configured as a quad-bank DRAM. Each of the 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

The 128Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. single read or write access for the 128Mb Mobile DDR SDRAM consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

It should be noted that the DLL that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Mobile DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine should be followed to ensure proper functionality of the Mobile DDR SDRAM.

To properly initialize the Mobile DDR SDRAM, the following sequence must be followed:

1. It is recommended the core power (V_{DD}) and I/O power (V_{DDQ}) be from the same power source and brought up simultaneously. If separate power sources are used, V_{DD} must lead V_{DDQ}.
2. Once power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. Once the clock is stable, a 200µs minimum delay is required by the Mobile DDR SDRAM prior to applying an executable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least ^{t}RP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least ^{t}RFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least ^{t}RFC time. As part of the individualization sequence, two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above. Alternately, the second AUTO-REFRESH command and NOP or DESELECT sequence can be issued after step 10.

7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue NOP or DESELECT commands for at least ^{t}MRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least ^{t}MRD time.

The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

Register Definition

Mode Registers

The mode registers are used to define the specific mode of operation of the Mobile DDR SDRAM. There are two mode registers used to specify the operational characteristics of the device. The standard mode register, which exists for all SDRAM devices, and the extended mode register, which is exists on all Mobile SDRAM devices.

Standard Mode Register

The standard mode register definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 3 on page 10. The standard mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again.

Reprogramming the standard mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 specify the operating mode.

Note: Standard refers to meeting JEDEC-standard mode register definitions.

Burst Length

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 3 on page 10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap until a boundary is reached. The block is uniquely selected by A1–A*i* when BL = 2, by A2–A*i* when BL = 4, by A3–A*i* when BL = 8 (where A*i* is

the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address. See Table 5 on page 11 for more information.

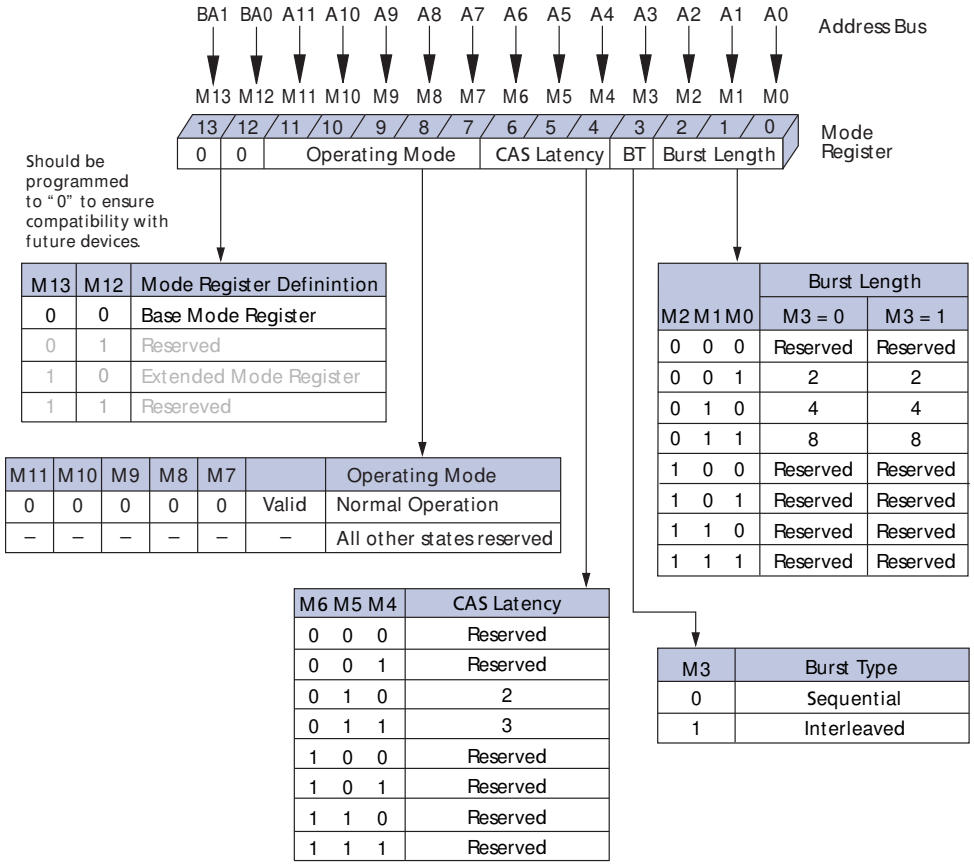
READ Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 3 clocks, as shown in Figure 3 on page 10.

For CL = 3, if the READ command is registered at clock edge *n*, then the data will nominally be available at (*n* + 2 clocks + ^{t}AC). For CL = 2, if the READ command is registered at clock edge *n*, then the data will be nominally be available at (*n* + 1 clock + ^{t}AC).

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 3: Standard Mode Register Definition



M13	M12	Mode Register Definintion
0	0	Base Mode Register
0	1	Reserved
1	0	Extended Mode Register
1	1	Resereved

M11	M10	M9	M8	M7		Operating Mode
0	0	0	0	0	Valid	Normal Operation
–	–	–	–	–	–	All other states reserved

M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

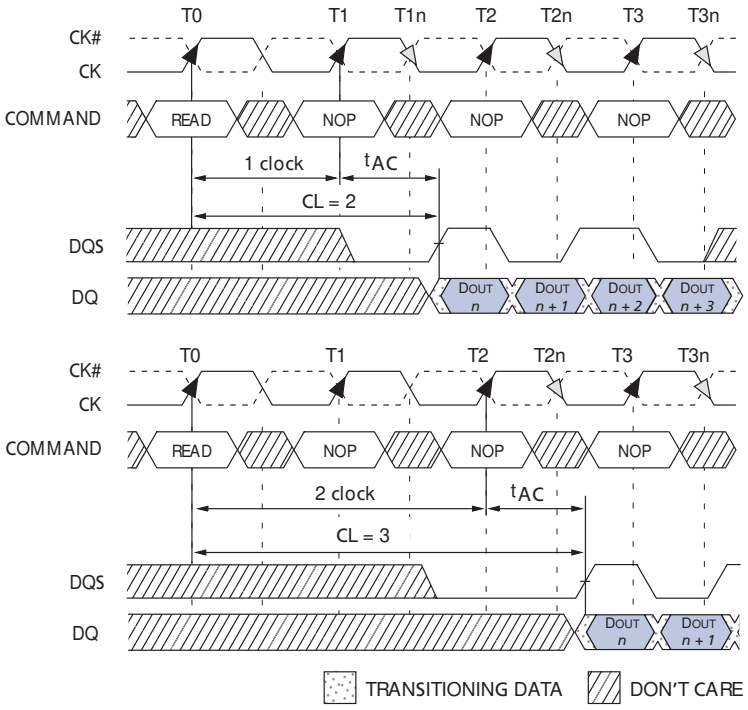
M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Table 5: Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Figure 4: CAS Latency



Notes: 1. BL = 4 in the cases shown.
2. Shown with nominal ^{t}AC and nominal ^{t}DSDQ.

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER SET command with bits A7–A11 each set to zero, and bits A0–A6 set to the desired values.

All other combinations of values for A7–A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions specific to low power operation. These additional functions include drive strength, temperature compensated self refresh, and partial array self refresh.

Temperature Compensated Self Refresh

On this version of the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Programming of the temperature compensated self refresh (TCSR) bits will have no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial Array Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The refresh options are as follows:

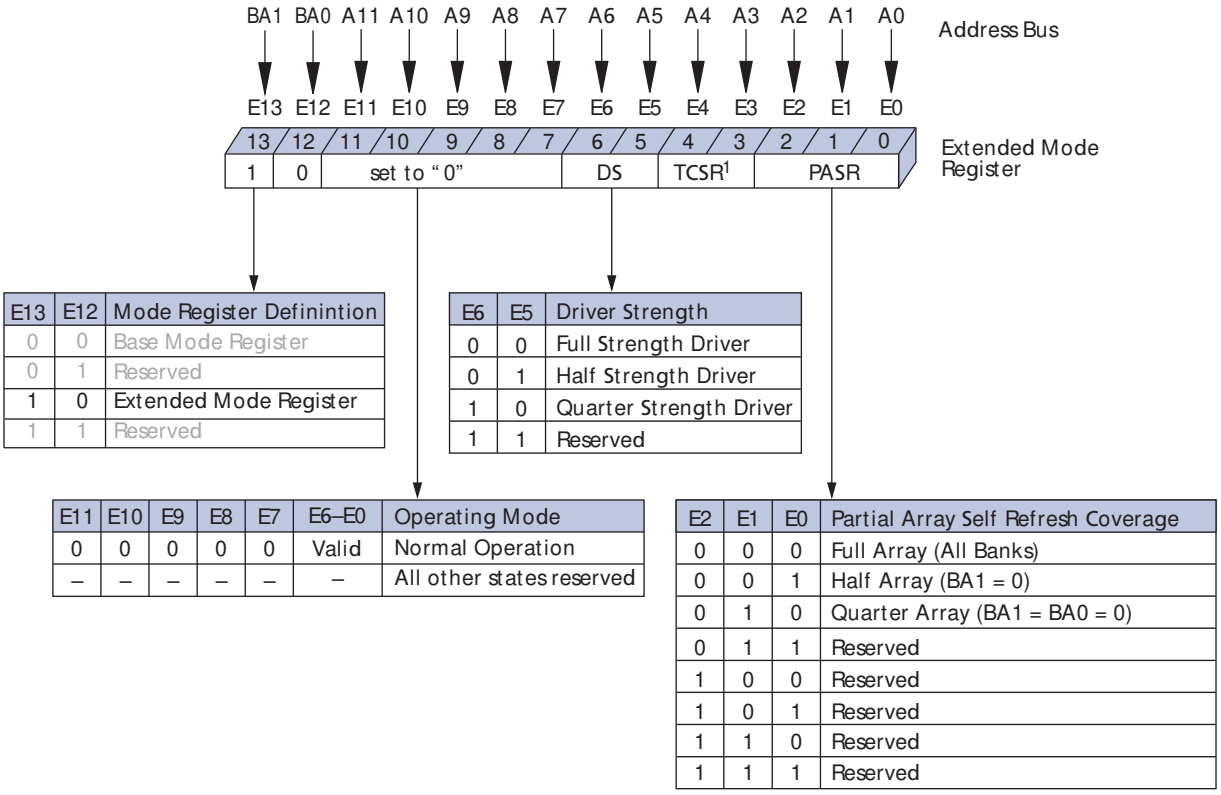
- Full array: banks 0, 1, 2, and 3
- Half array: banks 0 and 1
- Quarter array: bank 0

WRITE and READ commands can still occur during standard operation, but only the selected banks will be refreshed during SELF REFRESH. Data in banks that are disabled will be lost.

Output Driver Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 and A6 of the extended mode register can be used to select the driver strength of the DQ outputs. There are three allowable settings for the output drivers (25 ohm internal impedance, 55 ohm internal impedance, and 80 ohm internal impedance).

Figure 5: Extended Mode Register



E13	E12	Mode Register Definintion
0	0	Base Mode Register
0	1	Reserved
1	0	Extended Mode Register
1	1	Reserved

E6	E5	Driver Strength
0	0	Full Strength Driver
0	1	Half Strength Driver
1	0	Quarter Strength Driver
1	1	Reserved

E11	E10	E9	E8	E7	E6–E0	Operating Mode
0	0	0	0	0	Valid	Normal Operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial Array Self Refresh Coverage
0	0	0	Full Array (All Banks)
0	0	1	Half Array (BA1 = 0)
0	1	0	Quarter Array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes: 1. On-chip temperature sensor is used in place of TCSR. Setting these bits will have no effect.

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock which controls the SDRAM. There are two basic ways to control the clock:

1. Change the clock frequency.
2. Stop the clock.

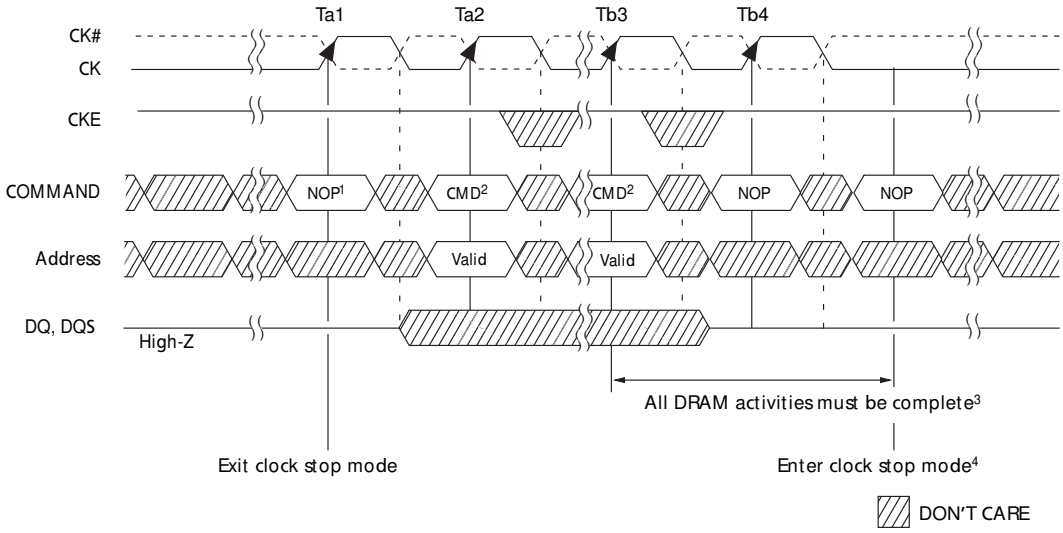
Both of these are specific to the application and its requirements and both allow power savings due to possible less transitions on the clock path.

The Mobile DDR SDRAM allows the clock to change frequency during operation, only if all the timing parameters are met with respect to that change and all refresh requirements are satisfied.

The clock can also be stopped if there are no data accesses in progress, either WRITEs or READs that would be affected by this change. If a WRITE or a READ is in progress the entire data burst must be complete prior to stopping the clock.

For READs, a burst completion is defined when the read postamble is satisfied; for WRITEs, a burst completion is defined when the write postamble and ^{t}WR or ^{t}WTR are satisfied. CKE must be held HIGH with CK = LOW and CK# = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP is required after the clock is restarted before a valid command can be issued. Figure 6 on page 14 illustrates the clock stop mode.

Figure 6: Clock Stop Mode



Notes:
1. Prior to Ta1, the device is in clock stop mode. To exit, at least one NOP is required before any valid command.
2. Any valid command is allowed, device is not in clock suspend mode.
3. Any DRAM operation already in process must be completed before entering clock stop mode. This includes ^{t}RCD, ^{t}RP, ^{t}RFC, ^{t}MRD, ^{t}WR, all data-out for READ bursts.
4. To enter and maintain a clock stop mode: CK = LOW, CK# = HIGH, CKE = HIGH.

Commands

Table 6 and Table 7 provide quick references of available commands. This is followed by a written description of each command. Three additional Truth Tables (Table 8 on page 42, Table 9 on page 43, and Table 10 on page 45) provide CKE commands and current/next state information.

Table 6: Truth Table – Commands

Note 1 applies to all commands; All states and sequences not shown are reserved and/or illegal.

Name (Function)	CS#	RAS#	CAS#	WE#	ADDR	Notes
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER (standard or extended mode registers)	L	L	L	L	Op-Code	2

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0–BA1 select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A11 provide the op-code to be written to the selected mode register.
3. BA0–BA1 provide bank address and A0–A11 provide row address.
4. BA0–BA1 provide bank address; A0–A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to READ bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.

Table 7: Truth Table – DM Operation

Name (Function)	DM	DQ
Write enable	L	Valid
Write inhibit	H	X

Note: Used to mask write data; provided coincident with corresponding data.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# = LOW, RAS# = CAS# = WE# = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A11. See mode register descriptions in "Register Definition" on page 9. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = 8 for x16) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the precharge command is issued. Except in the case of

concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating ^{t}RAS (MIN), as described for each burst type in "Operations" on page 19. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed.

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in "Operations" on page 19. The open page which the READ burst was terminated from remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the Mobile DDR SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 128Mb Mobile DDR SDRAM requires AUTO REFRESH cycles at an average interval of 15.625µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the auto refresh period. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the Mobile DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Mobile DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during SELF REFRESH.

During SELF REFRESH, the device is refreshed as identified in the external mode register (see PASR setting).

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the Mobile DDR SDRAM must have NOP commands issued for ^{t}XSR is required for the completion of any internal refresh in progress.

Operations

Bank/row Activation

Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 7.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 8 on page 20,which covers any case where $2 < {}^{t}\text{RCD (MIN)} / {}^{t}\text{CK} \leq 3$. (Figure 8 also shows the same case for ^{t}RCD; the same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 7: Activating a Specific Row in a Specific Bank

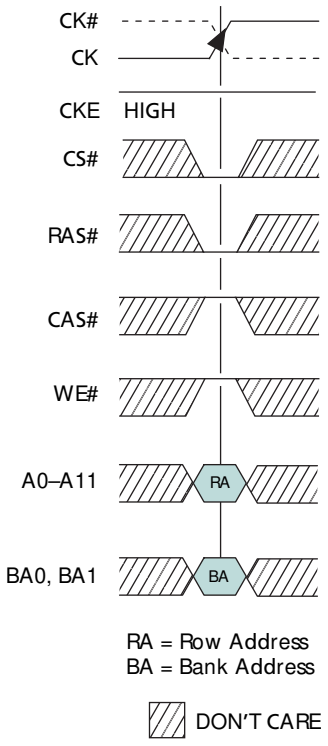
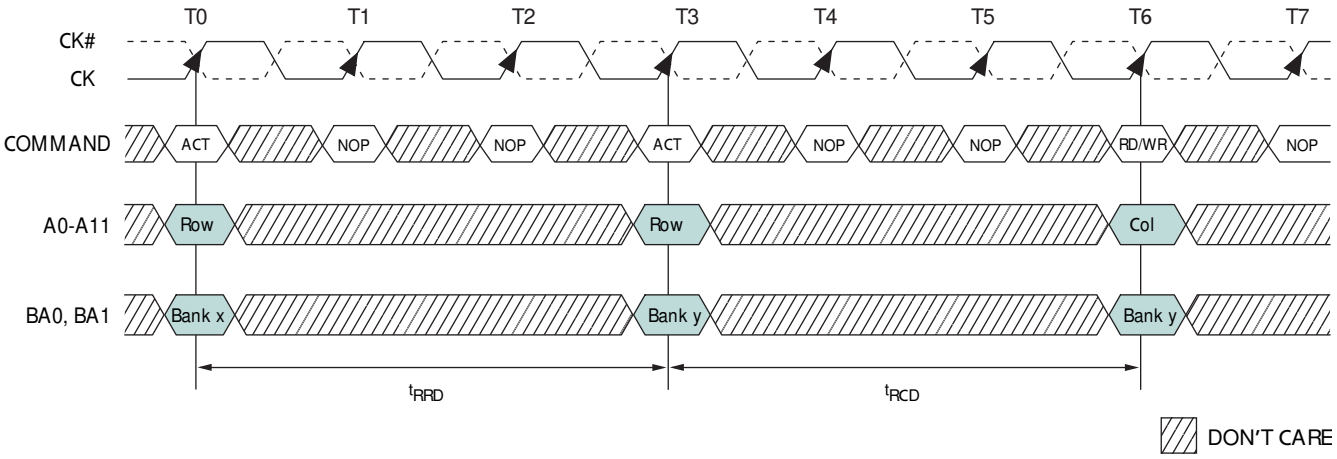


Figure 8: Example: Meeting ^{t}RCD (^{t}RRD) MIN When 2 < ^{t}RCD (^{t}RRD) MIN/^{t}CK ≤ 3



READs

READ bursts are initiated with a READ command, as shown in Figure 9 on page 21.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#). Figure 10 on page 22 shows general timing for each possible CAS latency setting. DQS is driven by the Mobile DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), the valid data window are depicted in Figure 31 on page 55. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is depicted in Figure 32 on page 56.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued ***x*** cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 11 on page 23.

A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown for illustration in Figure 12 on page 24. Full-speed random read accesses within a page (or pages) can be performed, as shown in Figure 13 on page 25.

Figure 9: READ Command

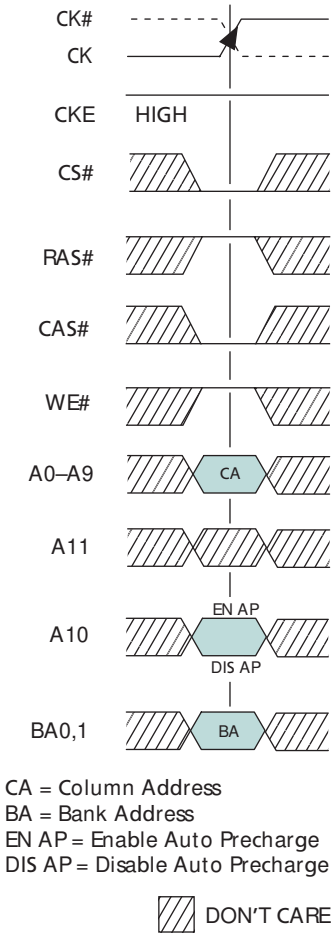
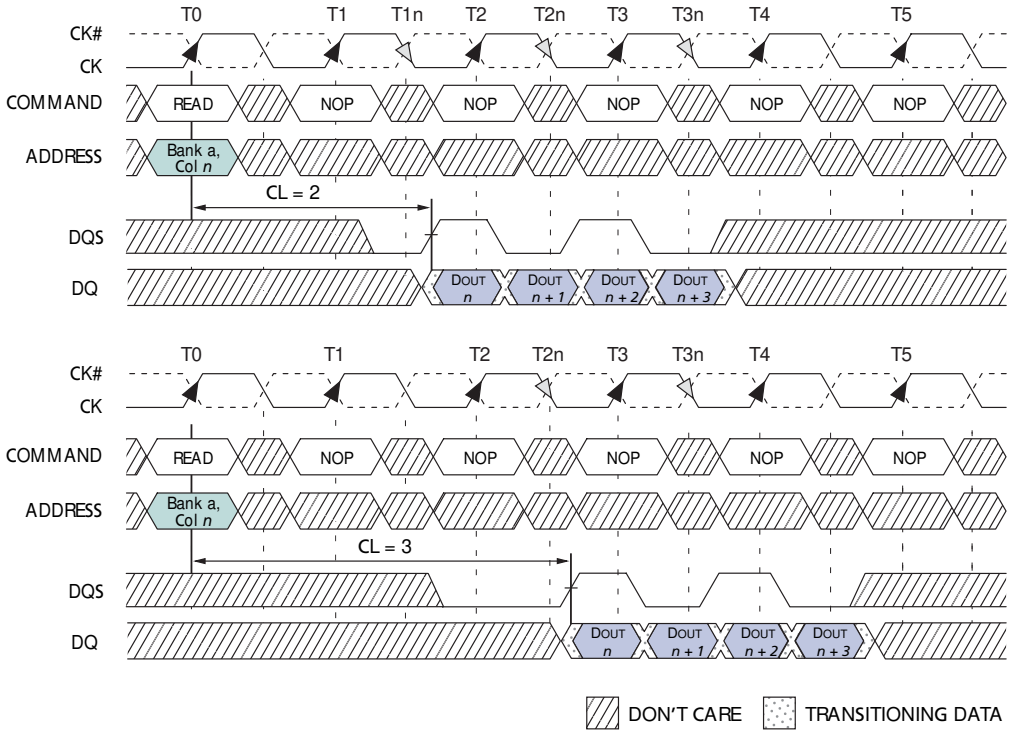
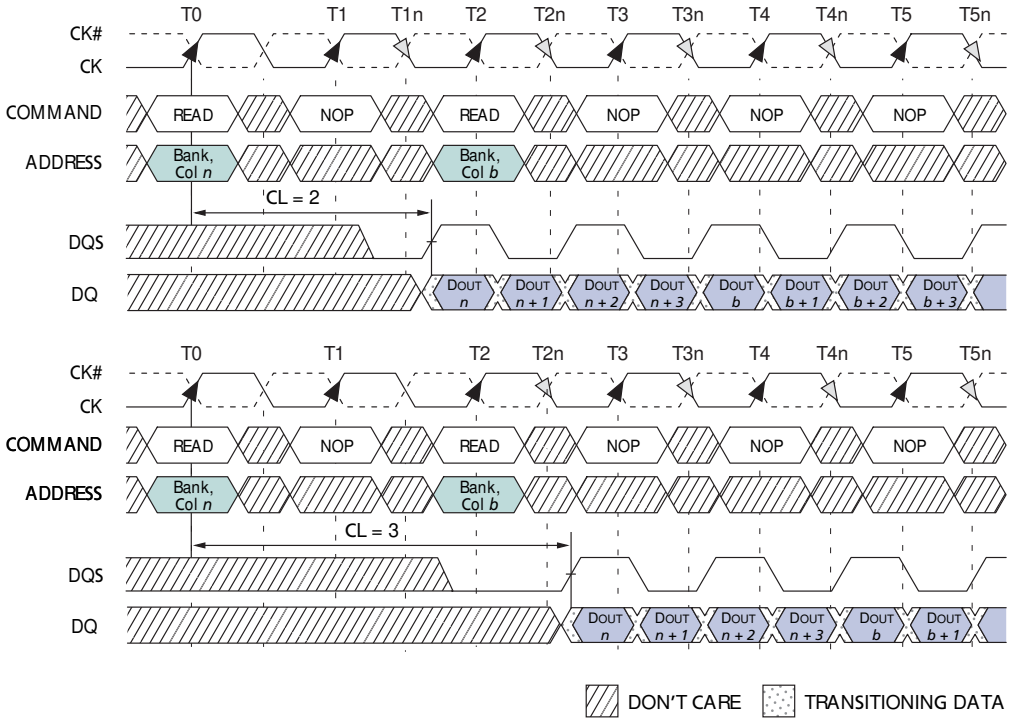


Figure 10: READ Burst



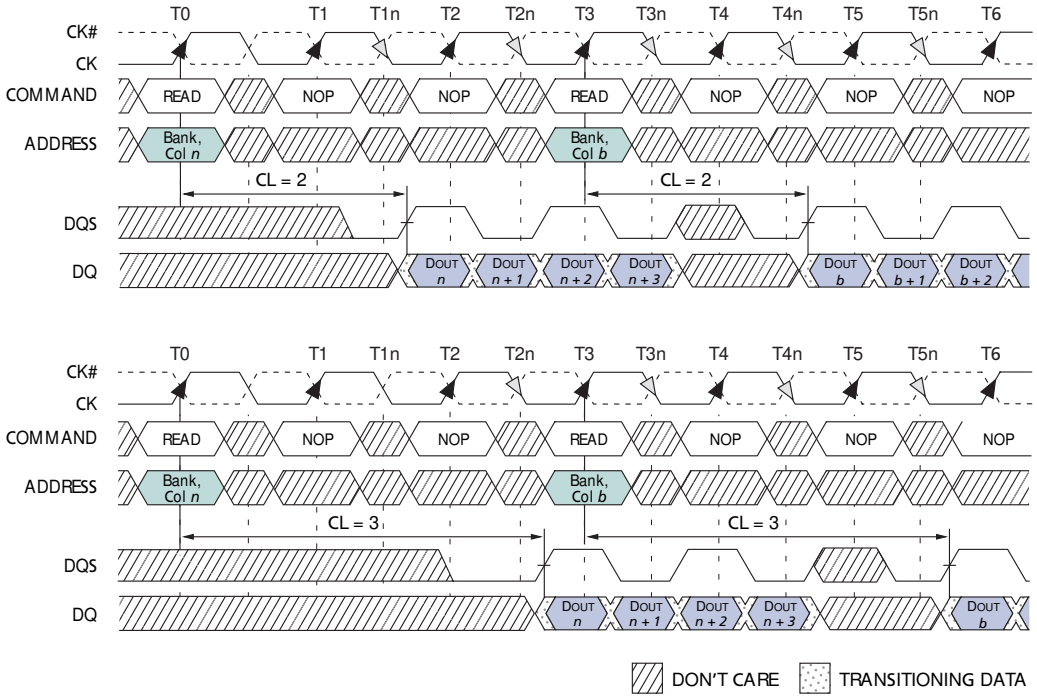
Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 11: Consecutive READ Bursts



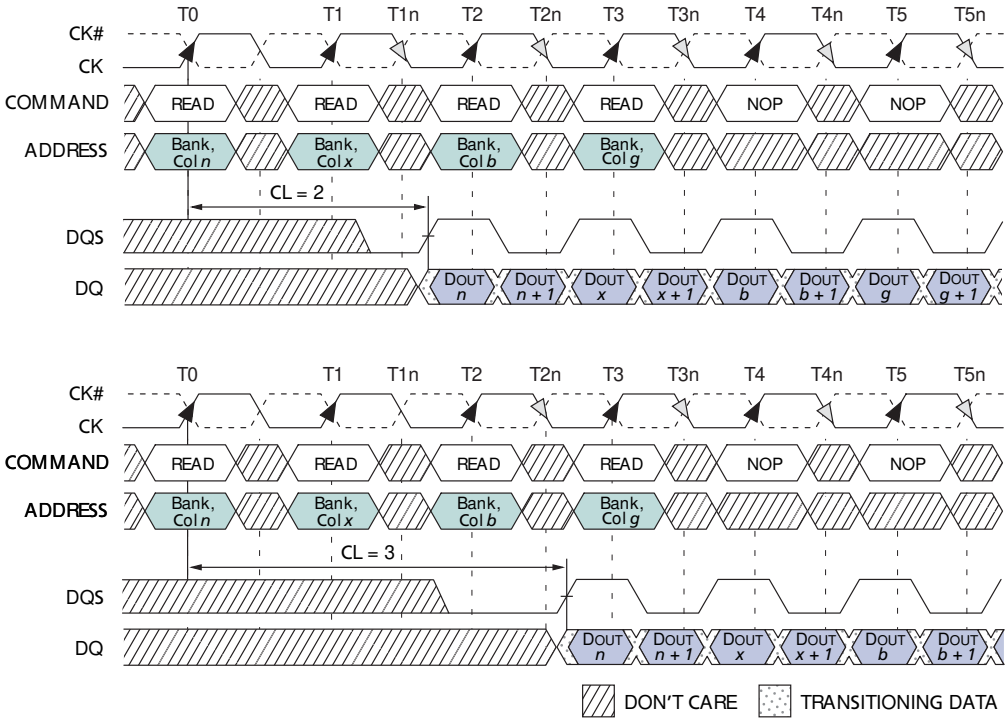
Notes:
1. DOUT *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. This example represents consecutive READ commands issued to the device.

Figure 12: Nonconsecutive READ Bursts



Notes:
1. DOUT *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. This example represents nonconsecutive READ commands issued to the device.

Figure 13: Random READ Accesses



Notes:
1. DOUT *n* (or *x*, b, *g*) = data-out from column *n* (or column *x*, column *b*, column *g*).
2. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
3. READs are to an active row in any bank.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Truncated READs

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 14 on page 26. The burst terminate latency is equal to the READ (CAS) latency, i.e., the BURST TERMINATE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 15 on page 27. The ^{t}DQSS (MIN) case is shown; the ^{t}DQSS (MAX) case has a longer bus idle time. (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the *n*-prefetch architecture). This is shown in Figure 16 on page 28. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

Note: Part of the row precharge time is hidden during the access of the last data elements.