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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Mobile DDR SDRAM

MT46H16M16LF – 4 Meg x 16 x 4 banks
MT46H8M32LF/LG – 2 Meg x 32 x 4 banks

For the latest data sheet, refer to Micron's Web site: www.micron.com

Features

- VDD/VDDQ = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths: 2, 4, or 8
- Concurrent auto precharge option supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS compatible inputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive (DS)
- Clock stop capability
- 64ms refresh period

Table 1: Configuration Addressing

DQ Bus Width	Architecture	JEDEC-Standard Option	Reduced Page-Size Option
	Number of banks	4	4
	Bank address balls	BA0, BA1	BA0, BA1
x16	Row address balls	A0–A12	–
	Column address balls	A0–A8	–
x32	Row address balls	A0–A11	A0–A12
	Column address balls	A0–A8	A0–A7

Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz)		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-6	83.3	166	6.5ns	5.0ns
-75	83.3	133	6.5ns	6.0ns

Options — Marking

Options	Marking
• VDD/VDDQ	
– 1.8V/1.8V	H
• Configuration	
– 16 Meg x 16 (4 Meg x 16 x 4 banks)	16M16
– 8 Meg x 32 (2 Meg x 32 x 4 banks)	8M32
• Row size option	
– JEDEC-standard option	LF
– Reduced page-size option[2]	LG
• Plastic "green" packages	
– 60-ball VFBGA 8mm x 9mm[1]	BF
– 90-ball VFBGA 8mm x 13mm[2]	B5
• Timing – cycle time	
– 6ns at CL = 3	-6
– 7.5ns at CL = 3	-75
• Power	
– Standard	None
– Low IDD2P/IDD6	L
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
• Design revision	:A

Notes: 1. Only available for x16 configuration.
2. Only available for x32 configuration.

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Figure 1: 256Mb Mobile DDR Part Numbering

Example Part Number: MT46H16M16LFXX-75IT :A

Micron DDR MT46	V_{DD}/ V_{DDQ}	Mobile Configuration	Package	–	Speed	Temp	Revision

V_{DD}/V_{DDQ}	
1.8V/1.8V	H

Configuration	
16 Meg x 16	16M16LF
8 Meg x 32	8M32LF

Package	
60-Ball VFBGA (lead-free)	BF
90-Ball VFBGA (lead-free)	B5

	Speed Grade
-6	^{t}CK = 6.0ns
-75	^{t}CK = 7.5ns
-10	^{t}CK = 9.6ns

	Operating Temp
	Commercial
IT	Industrial

	Revision
:A	First Generation

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA part marking decoder at www.micron.com/decoder.

General Description

The 256Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM. On the x16 device, each of the 67,108,864-bit banks is organized as 8,192 rows by 512 columns by 16 bits. On the x32 device, each of the 67,108,864-bit banks is organized as 4,096 rows by 512 columns by 32 bits.

The 256Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 256Mb Mobile DDR SDRAM effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Mobile DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes: one for the lower byte and one for the upper byte. The x32 offering has four data strobes, one per byte.

The 256Mb Mobile DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Mobile DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAM, the pipelined, multibank architecture of Mobile DDR SDRAM enables concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. Deep power-down mode is offered to achieve maximum power reduction by eliminating the power draw of the memory array. Data will not be retained when the device enters DPD mode.

Self refresh mode offers temperature compensation through an on-chip temperature sensor and partial-array self refresh, which enables users to achieve additional power savings. The temperature sensor is enabled by default, and the partial-array self refresh can be programmed through the extended mode register.

Notes:
1. Throughout the data sheet, various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
2. Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.

Functional Block Diagrams

Figure 2: Functional Block Diagram (16 Meg x 16)

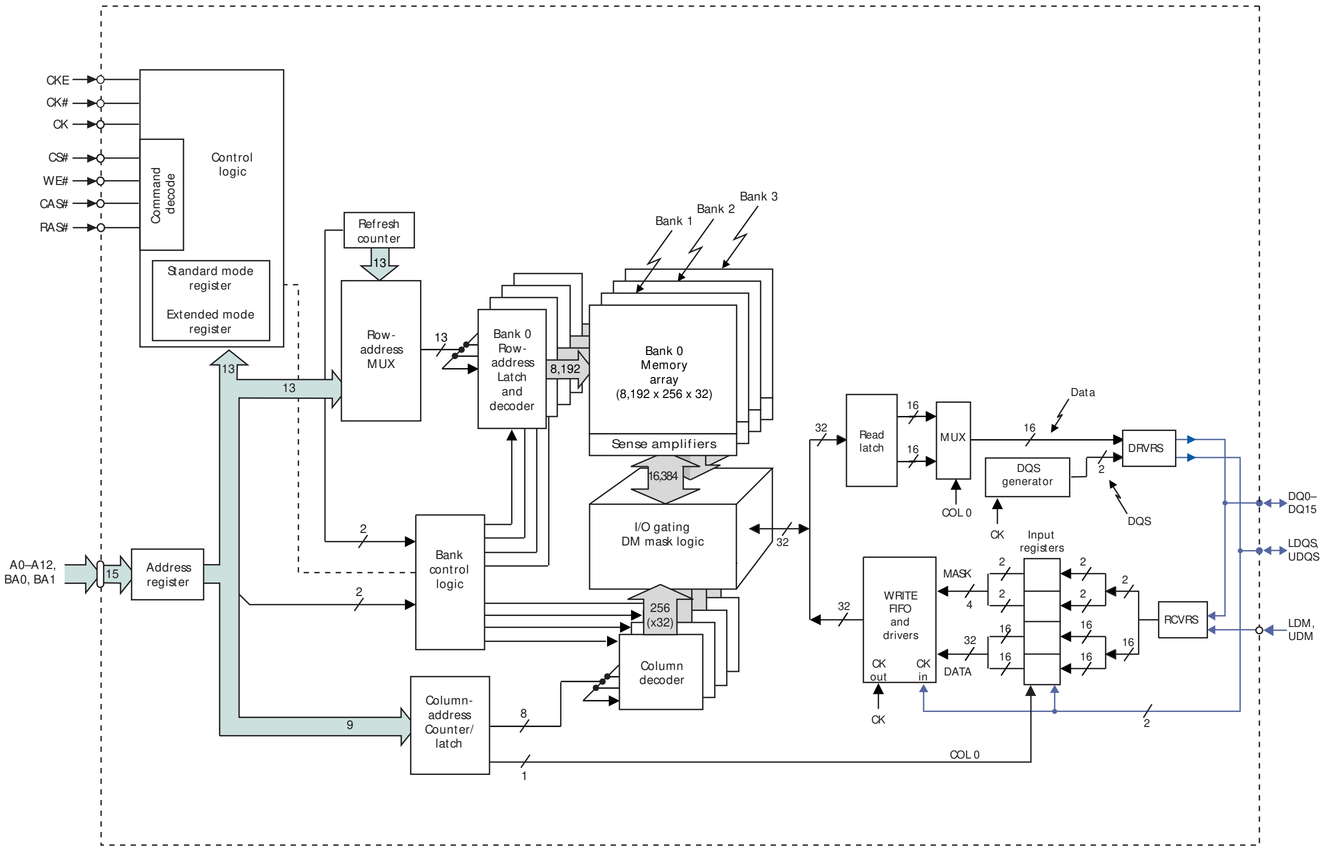
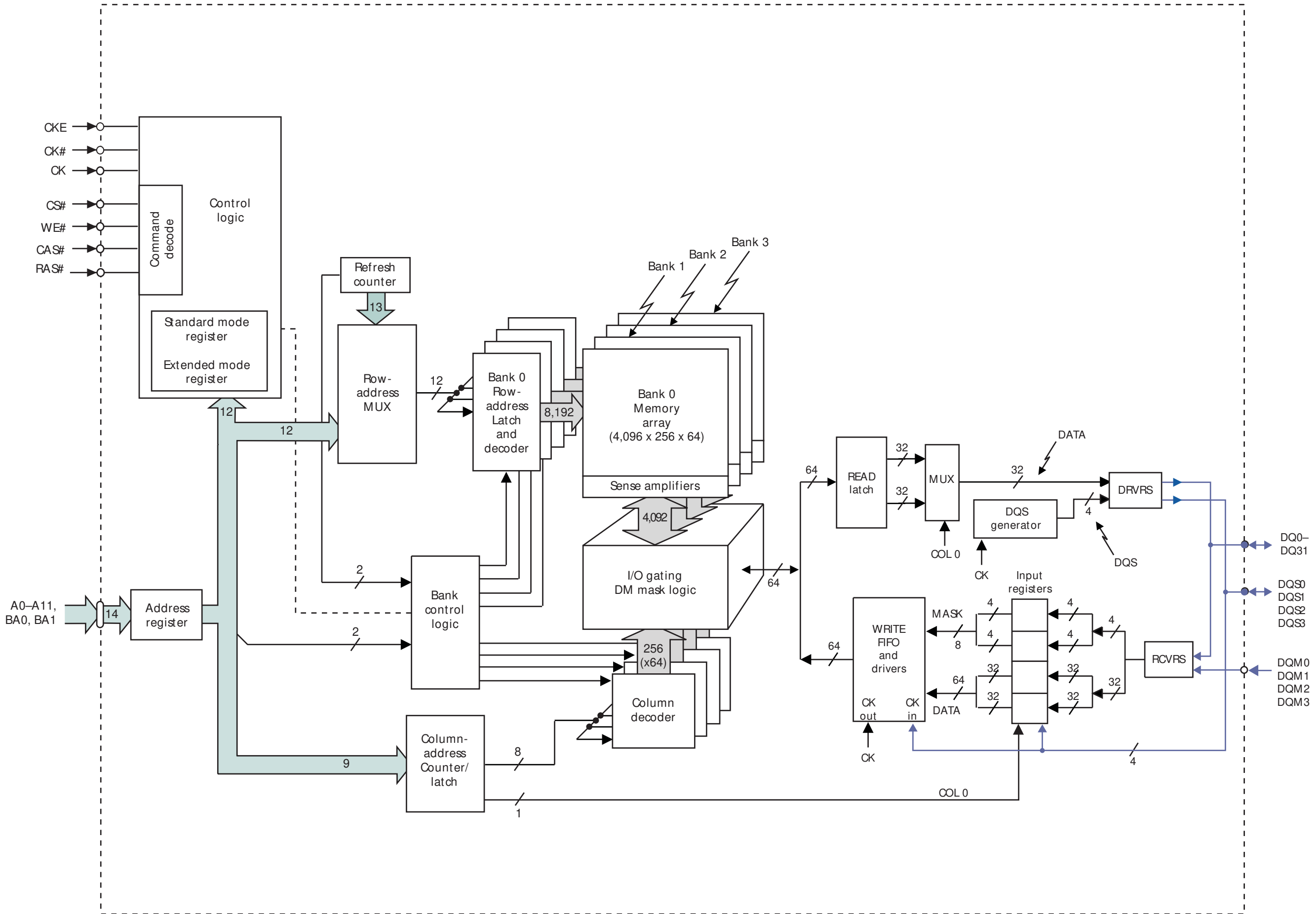


Figure 3: Functional Block Diagram (8 Meg x 32)



Notes: 1. JEDEC-standard x32 DQ configuration shown.

Ballouts and Ball Descriptions

Figure 4: 60-Ball VFBGA Ball Assignments – 8mm x 9mm (Top View)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	DQ15	$V_{SS}Q$				$V_{DD}Q$	DQ0	V_{DD}
B	$V_{DD}Q$	DQ13	DQ14				DQ1	DQ2	$V_{SS}Q$
C	$V_{SS}Q$	DQ11	DQ12				DQ3	DQ4	$V_{DD}Q$
D	$V_{DD}Q$	DQ9	DQ10				DQ5	DQ6	TEST[1]
E	$V_{SS}Q$	UDQS	DQ8				DQ7	LDQS	$V_{DD}Q$
F	V_{SS}	UDM	NC				NC	LDM	V_{DD}
G	CKE	CK	CK#				WE#	CAS#	RAS#
H	A9	A11	A12				CS#	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	V_{SS}	A4	A5				A2	A3	V_{DD}

Ball Down

Notes: 1. D9 is a test pin that must be connected to V_{SS} or $V_{SS}Q$ in normal operation.

Figure 5: 90-Ball VFBGA Ball Assignments – 8mm x 13mm (Top View)

	1	2	3	4	5	6	7	8	9
A	VSS	DQ31	VSSQ				VDDQ	DQ16	VDD
B	VDDQ	DQ29	DQ30				DQ17	DQ18	VSSQ
C	VSSQ	DQ27	DQ28				DQ19	DQ20	VDDQ
D	VDDQ	DQ25	DQ26				DQ21	DQ22	TEST[1]
E	VSSQ	DQS3	DQ24				DQ23	DQS2	VDDQ
F	VDD	DM3	NC				NC	DM2	VSS
G	CKE	CK	CK#				WE#	CAS#	RAS#
H	A9	A11	A12/DNU				CS#	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	A4	DM1	A5				A2	DM0	A3
L	VSSQ	DQS1	DQ8				DQ7	DQS0	VDDQ
M	VDDQ	DQ9	DQ10				DQ5	DQ6	VSSQ
N	VSSQ	DQ11	DQ12				DQ3	DQ4	VDDQ
P	VDDQ	DQ13	DQ14				DQ1	DQ2	VSSQ
R	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD

Ball Down

Notes: 1. D9 is a test pin that must be connected to VSS or VSSQ in normal operation.

Table 3: 60-Ball VFBGA Ball Descriptions

Ball Numbers	Symbol	Type	Description
G2, G3	CK, CK#	Input	**Clock**: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
G1	CKE	Input	**Clock enable**: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle) or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
H7	CS#	Input	**Chip select**: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
G9, G8, G7	RAS#, CAS#, WE#	Input	**Command inputs**: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F2, F8	UDM, LDM	Input	**Input data mask**: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x16, LDM is DM for DQ0–DQ7, and UDM is DM for DQ8–DQ15.
H8, H9	BA0, BA1	Input	**Bank address inputs**: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
J8, J9, K7, K8, K2, K3, J1, J2, J3, H1, J7, H2, H3	A0–A12	Input	**Address inputs**: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A8, B7, B8, C7, C8, D7, D8, E7, E3, D2, D3, C2, C3, B2, B3, A2	DQ0–DQ15	I/O	**Data input/output**: Data bus for x16.
E2, E8	UDQS, LDQS	I/O	**Data strobe**: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. Data strobe is used to capture data.
A7, B1, C9, D1, E9	$V_{DD}Q$	Supply	DQ power supply.
A3, B9, C1, E1	$V_{SS}Q$	Supply	DQ ground.
A9, F9, K9	V_{DD}	Supply	Power supply.
A1, F1, K1	V_{SS}	Supply	Ground.
F3, F7	NC	–	**No connect**: May be left unconnected.
D9	TEST	–	Test pin that must be connected to V_{SS} or $V_{SS}Q$ in normal operation.

Table 4: 90-Ball VFBGA Ball Description

Ball Numbers	Symbol	Type	Description
G2, G3	CK, CK#	Input	**Clock**: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
G1	CKE	Input	**Clock enable**: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle) or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
H7	CS#	Input	**Chip select**: CS# enables the command decoder (registered LOW) and disables the command decoder (registered HIGH). All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
G9, G8, G7	RAS#, CAS#, WE#	Input	**Command inputs**: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
K8, K2, F8, F2	DM0–DM3	Input	**Input data mask**: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x32, DM0 is DM for DQ0–DQ7; DM1 is DM for DQ8–DQ15; DM2 is DM for DQ16–DQ23; and DM3 is DM for DQ24–DQ31.
H8, H9	BA0, BA1	Input	**Bank address inputs**: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
J8, J9, K7, K9, K1, K3, J1, J2, J3, H1, J7, H2	A0–A11	Input	**Address inputs**: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
H3	A12/DNU	Input	A12 is an address input for the LG reduced page-size option (see "Options" on page 1). Leave as DNU for JEDEC-standard option.
R8, P7, P8, N7, N8, M7, M8, L7, L3, M2, M3, N2, N3, P2, P3, R2, A8, B7, B8, C7, C8, D7, D8, E7, E3, D2, D3, C2, C3, B2, B3, A2	DQ0–DQ31	I/O	**Data input/output**: Data bus for x32.
L8, L2, E8, E2	DQS0–DQS3	I/O	**Data strobe**: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. Data strobe is used to capture data.
A7, B1, C9, D1, E9, L9, M1, N9, P1, R7	V_{DDQ}	Supply	DQ power supply.

Table 4: 90-Ball VFBGA Ball Description (Continued)

Ball Numbers	Symbol	Type	Description
A3, B9, C1, E1, L1, M9, N1, P9, R3	VssQ	Supply	DQ ground.
A9, F1, R9	VDD	Supply	Power supply
A1, F9, R1	Vss	Supply	Ground.
F3, F7	NC	–	**No connect**: May be left unconnected.
D9	TEST	–	Test pin that must be connected to Vss or VssQ in normal operation.

Functional Description

The 256Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM. Each of the 67,108,864-bit banks on the x16 is organized as 8,192 rows by 512 columns by 16 bits. Each of the 67,108,864-bit banks on the x32 is organized as 4,096 rows by 512 columns by 32 bits for the standard addressing configuration.

The 256Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. Single read or write access for the 256Mb Mobile DDR SDRAM consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The DLL circuit that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Mobile DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine must be followed to ensure proper functionality of the Mobile DDR SDRAM. The clock stop feature is not available until the device has been properly initialized.

To properly initialize the Mobile DDR SDRAM, this sequence must be followed:

1. The core power (V_{DD}) and I/O power (V_{DDQ}) must be brought up simultaneously. It is recommended that V_{DD} and V_{DDQ} be from the same power source, or V_{DDQ} must never exceed V_{DD}. Assert and hold CKE HIGH.
2. After power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. After the clock is stable, a 200µs (MIN) delay is required by the Mobile DDR SDRAM prior to applying an executable command. During this time, a NOP or DESELECT command must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue a NOP or DESELECT command for at least ^tRP time.
6. Issue an AUTO REFRESH command followed by a NOP or DESELECT command for at least ^tRFC time. Issue a second AUTO REFRESH command followed by a NOP or DESELECT command for at least ^tRFC time. As part of the initialization sequence, two AUTO REFRESH commands must be issued.

7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue a NOP or DESELECT command for at least ^{t}MRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least ^{t}MRD time.

The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

Register Definition

Mode Registers

The mode registers are used to define the specific mode of operation of the Mobile DDR SDRAM. Two mode registers are used to specify the operational characteristics of the device.

Standard Mode Register

The standard mode register bit definition enables the selection of burst length, burst type, CAS latency, and operating mode, as shown in Figure 6 on page 16. Reserved states should not be used, as this may result in setting the device into an unknown state or cause incompatibility with future versions of Mobile DDR SDRAM. The standard mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again, the device goes into deep power-down mode, or the device loses power.

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait before initiating the subsequent operation. Violating any of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the Mobile DDR SDRAM are burst oriented; the burst length is programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both sequential and interleaved burst types.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap when a boundary is reached. The block is uniquely selected by A1–A*i* when BL = 2, by A2–A*i* when BL = 4, and by A3–A*i* when BL = 8, where A*i* is the most significant column address bit for a given configuration. The remaining (least significant) address bits are used to specify the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed either to be sequential or interleaved via the standard mode register.

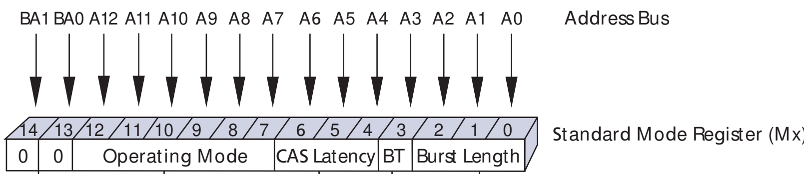
The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address (see Table 5 on page 17).

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first output data. The latency can be set to two or three clocks, as shown in Figure 7 on page 18.

For CAS latency three (CL = 3), if the READ command is registered at clock edge *n*, then the data will nominally be available at (n + 2 clocks + ^{t}AC). For CL = 2, if the READ command is registered at clock edge *n*, then the data will be nominally be available at (n + 1 clock + ^{t}AC).

Figure 6: Standard Mode Register Definition



M14	M13	Mode Register Definition
0	0	Standard mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

			Burst Length	
M2	M1	M0	M3 = 0	M3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

	Burst Type
0	Sequential
1	Interleaved

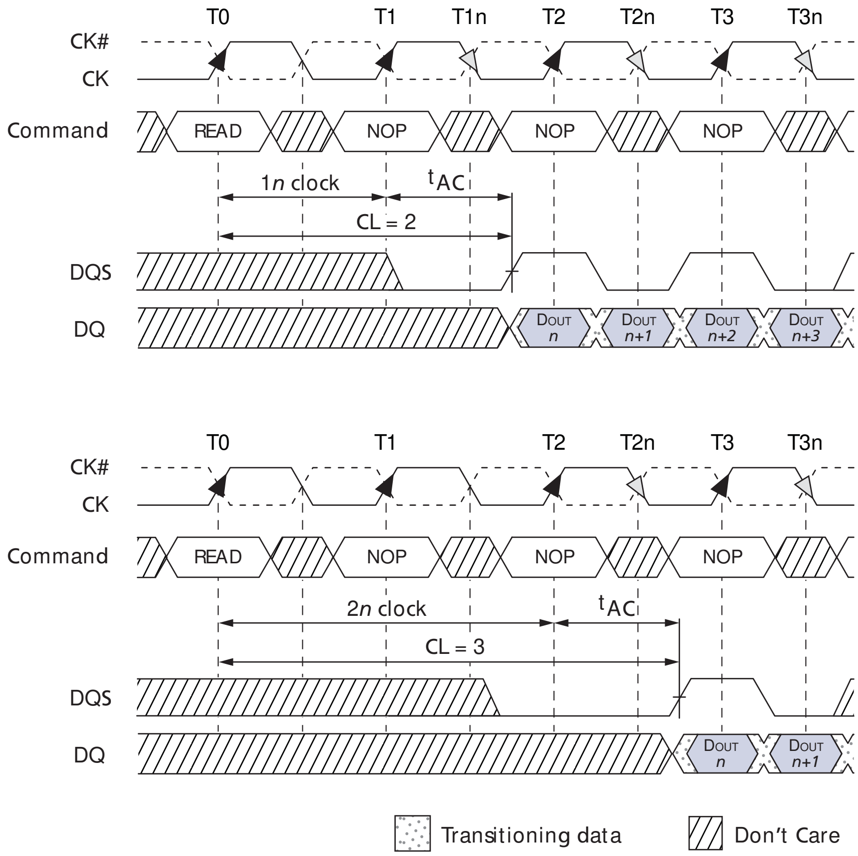
M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M12	M11	M10	M9	M8	M7	M6–M0	Operating Mode
0	0	0	0	0	0	Valid	Normal operation
–	–	–	–	–	–		All other states reserved

Table 5: Burst Definition Table

Burst Length	Starting Column Address				Order of Accesses Within a Burst	
					Type = Sequential	Type = Interleaved
2				**A0**		
				0	0-1	0-1
				1	1-0	1-0
4			**A1**	**A0**		
			0	0	0-1-2-3	0-1-2-3
			0	1	1-2-3-0	1-0-3-2
			1	0	2-3-0-1	2-3-0-1
			1	1	3-0-1-2	3-2-1-0
8		**A2**	**A1**	**A0**		
		0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
		0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
		0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
		0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
		1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
		1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
		1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
		1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Figure 7: CAS Latency



Notes:
1. BL = 4 in the cases shown.
2. Shown with nominal ^{t}AC and nominal ^{t}DQSQ.

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER command with bits A7–A11 (x32) or A7–A12 (x16) each set to zero and bits A0–A6 set to the desired values.

All other combinations of values for A7–A11/A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used, because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions specific to Mobile SDRAM operation. These additional functions include drive strength, temperature-compensated self refresh, and partial-array self refresh.

The extended mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 1) and will retain the stored information until it is programmed again, the device goes into deep power-down mode, or the device loses power.

Temperature-Compensated Self Refresh

On this version of the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the SELF REFRESH oscillator. Programming the TCSR bits will have no effect on the device. The SELF REFRESH oscillator will continue to refresh at the factory-programmed optimal rate for the device temperature.

Partial-Array Self Refresh

For further power savings during SELF REFRESH, the partial-array self refresh (PASR) feature enables the controller to select the amount of memory that will be refreshed during SELF REFRESH.

Table 6: Partial-Array Self Refresh Options

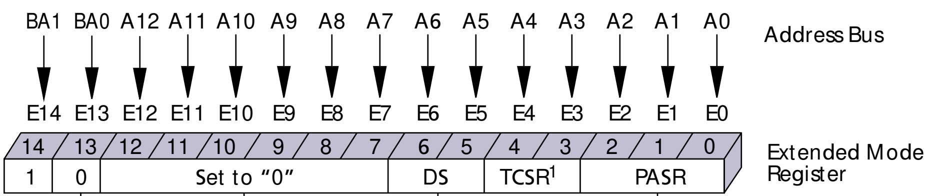
Memory	Bank
Full array	Banks 0, 1, 2, and 3
Half array	Banks 0 and 1
Quarter array	Bank 0
Eighth array	Bank 0 with row address MSB = 0
Sixteenth array	Bank 0 with row address MSB = 0 and MSB - 1 = 0

WRITE and READ commands can still occur during standard operation, but only the selected regions of the array will be refreshed during SELF REFRESH. Data in regions that are not selected will be lost.

Output Driver Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on expected loading of the memory bus. There are four allowable settings for the output drivers: 25Ω, 55Ω, 80Ω, and 100Ω internal impedance.

Figure 8: Extended Mode Register



E14	E13	Mode Register Definition
0	0	Standard mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

E6	E5	Driver Strength
0	0	Full-strength driver
0	1	Half-strength driver
1	0	Quarter-strength driver
1	1	One-eighth-strength driver

E12	E11	E10	E9	E8	E7	E6–E0	Operating Mode
0	0	0	0	0	0	Valid	Normal operation
–	–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array
0	0	1	Half array
0	1	0	Quarter array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array
1	1	0	One-sixteenth array
1	1	1	Reserved

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock that controls the DDR SDRAM. Control the clock in two ways:

- Change the clock frequency.
- Stop the clock.

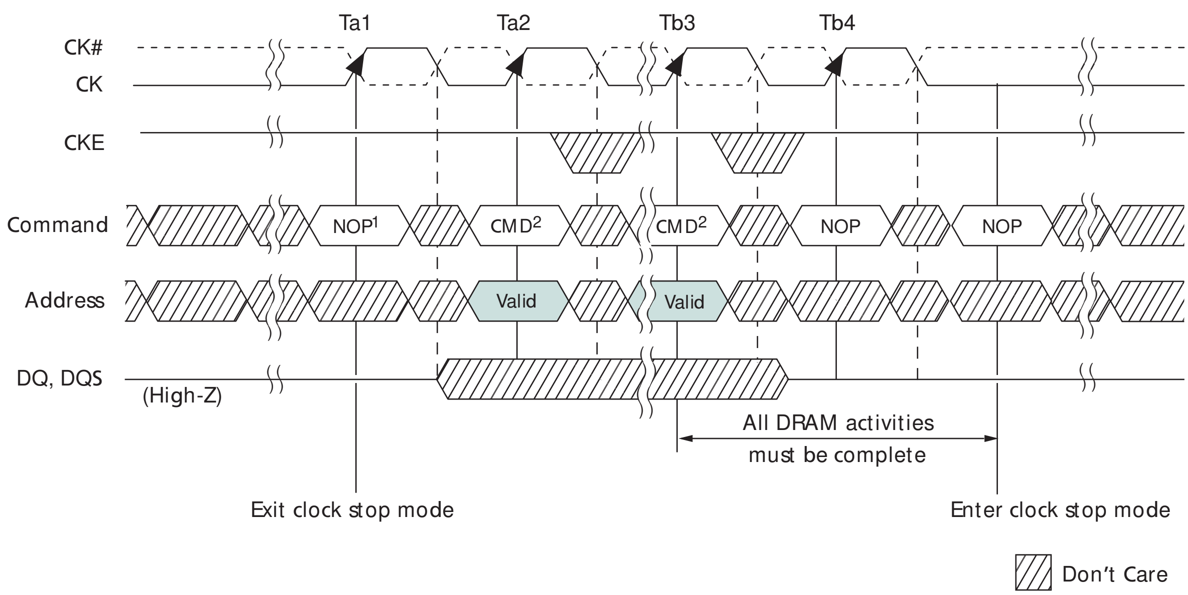
The Mobile DDR SDRAM enables the clock to change frequency during operation only if all the timing parameters are met and all refresh requirements are satisfied.

The clock can be stopped if no DRAM operations are in progress that would be affected by this change. Any DRAM operation already in process must be completed before entering clock stop mode; this includes the following timings: ^{t}RCD, ^{t}RP, ^{t}RFC, ^{t}MRD, ^{t}WR, and all data-out for READ bursts.

For example, if a WRITE or a READ is in progress, the entire data burst must be complete prior to stopping the clock. For READs, a burst completion is defined when the read postamble is satisfied. For WRITEs, a burst completion is defined when the write postamble and ^{t}WR or ^{t}WTR are satisfied.

CKE must be held HIGH with CK = LOW and CK# = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP or DESELECT is required after the clock is restarted before a valid command can be issued. Figure 9 on page 21 illustrates the clock stop mode.

Figure 9: Clock Stop Mode



Notes:
1. Prior to Ta1, the device is in clock stop mode. To exit, at least one NOP is required before any valid command is issued.
2. Any valid command is allowed; device is not in clock stop mode.

Commands

Tables 7 and 8 provide a quick reference of available commands. This is followed by a description of each command. Three additional truth tables provide CKE commands and current/next state information (see Table 9 on page 51, Table 10 on page 52, and Table 11 on page 54).

Table 7: Truth Table – Commands
Notes 1 and 2 apply to all commands

Name (Function)	CS#	RAS#	CAS#	WE#	Address	Notes
DESELECT (NOP)	H	X	X	X	X	3
NO OPERATION (NOP)	L	H	H	H	X	3
ACTIVE (select bank and activate row)	L	L	H	H	Bank/row	4
READ (select bank and column, and start READ burst)	L	H	L	H	Bank/column	5
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	Bank/column	5
BURST TERMINATE or deep power-down (enter deep power-down mode)	L	H	H	L	X	6, 7
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	8
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	9, 10
LOAD MODE REGISTER (standard or extended mode registers)	L	L	L	L	Op-code	11

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and deep power-down.
2. All states and sequences not shown are reserved and/or illegal.
3. DESELECT and NOP are functionally interchangeable.
4. BA0–BA1 provide bank address and A0–A12/A13 provide row address.
5. BA0–BA1 provide bank address; A0–A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent); A10 LOW disables the auto precharge feature.
6. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
7. This command is a BURST TERMINATE if CKE is HIGH and deep power-down if CKE is LOW.
8. A10 LOW: BA0–BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
9. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
10. Internal refresh counter controls row addressing; all self refresh inputs and I/Os are "Don't Care" except for CKE.
11. BA0–BA1 either select the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A12/A13 provide the op-code to be written to the selected mode register.

Table 8: Truth Table – DM Operation

Name (Function)	DM	DQ	Notes
Write enable	L	Valid	1, 2
Write inhibit	H	X	1, 2

Notes:
1. Used to mask write data; provided coincident with the corresponding data.
2. All states and sequences not shown are reserved and illegal.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected Mobile DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs BA0–BA1 and A0–A12. See mode register descriptions in “Register Definition” on page 15. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = the most significant column address bit for each configuration) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0–BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = the most significant column address bit for each configuration) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. The exception is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging.

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as described in "Operations" on page 26. The open page from which the READ burst was terminated remains open.

AUTO REFRESH

The AUTO REFRESH command is nonpersistent and must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 256Mb Mobile DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125µs (MAX).

To enable improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although not a JEDEC requirement, CKE must be active (HIGH) during the auto refresh period to provide for future functionality features. The auto refresh period begins when the AUTO REFRESH command is registered, and it ends ^{t}RFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the Mobile DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Mobile DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except that CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during SELF REFRESH. For details on entering and exiting self refresh mode, see Figure 44 on page 72. During SELF REFRESH, the device is refreshed as identified in the extended mode register (see PASR setting).

Auto Precharge

Auto precharge is a feature that performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst.

Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This earliest valid stage is determined as if an explicit PRECHARGE command were issued at the earliest possible time, without violating ^{t}RAS (MIN), as described for each burst type in "Operations" on page 26. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed.

Deep Power-Down

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power draw of the memory array. Data will not be retained when the device enters deep power-down mode.

Figure 10: Mobile DRAM State Diagram