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Double Data Rate (DDR) SDRAM

MT46V64M4 – 16 Meg x 4 x 4 banks
MT46V32M8 – 8 Meg x 8 x 4 banks
MT46V16M16 – 4 Meg x 16 x 4 banks

Features

- V_{DD} = 2.5V ±0.2V; V_{DDQ} = 2.5V ±0.2V
  V_{DD} = 2.6V ±0.1V; V_{DDQ} = 2.6V ±0.1V (DDR400)[1]
- Bidirectional data strobe (DQS) transmitted/ received with data, that is, source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths (BL): 2, 4, or 8
- Auto refresh
  – 64ms, 8192-cycle
- Longer-lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL_2-compatible)
- Concurrent auto precharge option supported
- ^{t}RAS lockout supported (^{t}RAP = ^{t}RCD)

Options / Marking

- Configuration
  – 64 Meg x 4 (16 Meg x 4 x 4 banks) — 64M4
  – 32 Meg x 8 (8 Meg x 8 x 4 banks) — 32M8
  – 16 Meg x 16 (4 Meg x 16 x 4 banks) — 16M16
- Plastic package – OCPL
  – 66-pin TSOP — TG
  – 66-pin TSOP (Pb-free) — P
- Plastic package
  – 60-ball FBGA (8mm x 12.5mm) — CV
  – 60-ball FBGA (8mm x 12.5mm) (Pb-free) — CY
- Timing – cycle time
  – 5ns @ CL = 3 (DDR400) — -5B[3]
  – 6ns @ CL = 2.5 (DDR333) FBGA only — -6[2]
  – 6ns @ CL = 2.5 (DDR333) TSOP only — -6T[2]
- Self refresh
  – Standard — None
  – Low-power self refresh — L
- Temperature rating
  – Commercial (0°C to +70°C) — None
  – Industrial (–40°C to +85°C) — IT
- Revision
  – x4, x8, x16 — :K[4]
  – x4, x8, x16 — :M

Notes: 1. DDR400 devices operating at ≤ DDR333 conditions can use V_{DD}/V_{DDQ} = 2.5V ±0.2V.
2. Available only on Revision K.
3. Available only on Revision M.
4. Not recommended for new designs.

Table 1: Key Timing Parameters
CL = CAS (READ) latency; MIN clock rate with 50% duty cycle at CL = 2 (-75E, -75Z), CL = 2.5 (-6, -6T, -75), and CL = 3 (-5B)

Speed Grade	Clock Rate (MHz)			Data-Out Window	Access Window	DQS–DQ Skew
	CL = 2	CL = 2.5	CL = 3			
-5B	133	167	200	1.6ns	±0.70ns	0.40ns
-6	133	167	n/a	2.1ns	±0.70ns	0.40ns
6T	133	167	n/a	2.0ns	±0.70ns	0.45ns
-75E/-75Z	133	133	n/a	2.5ns	±0.75ns	0.50ns
-75	100	133	n/a	2.5ns	±0.75ns	0.50ns

Table 2: Addressing

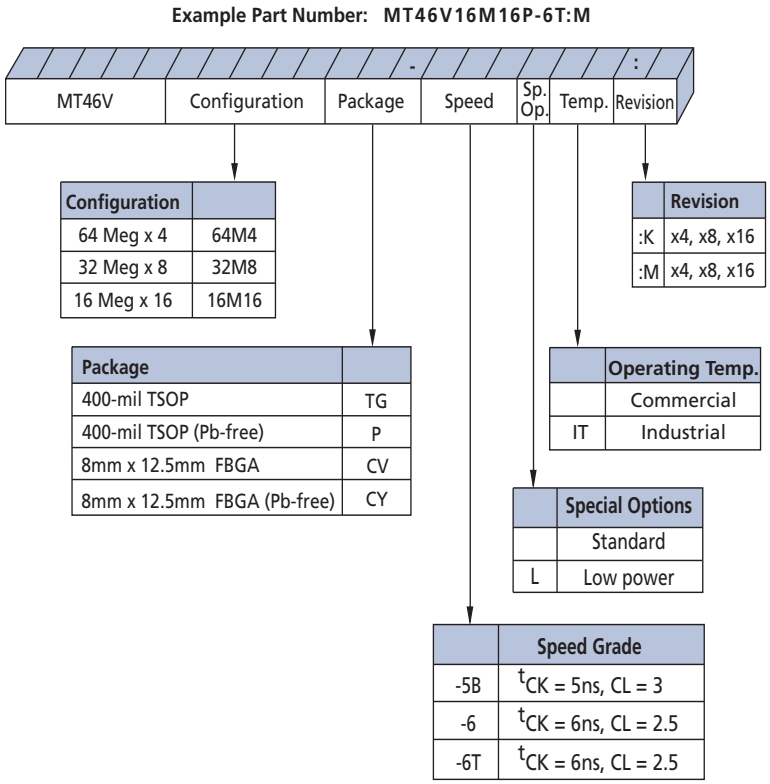
Parameter	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4 banks	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Bank address	4 (BA[1:0])	4 (BA[1:0])	4 (BA[1:0])
Column address	2K (A[9:0], A11)	1K (A[9:0])	512 (A[8:0])

Table 3: Speed Grade Compatibility

Marking	PC3200 (3-3-3)	PC2700 (2.5-3-3)	PC2100 (2-2-2)	PC2100 (2-3-3)	PC2100 (2.5-3-3)	PC1600(2-2-2)
-5B[1]	Yes	Yes	Yes	Yes	Yes	Yes
-6	–	Yes	Yes	Yes	Yes	Yes
-6T	–	Yes	Yes	Yes	Yes	Yes
-75E	–	–	Yes	Yes	Yes	Yes
-75Z	–	–	–	Yes	Yes	Yes
-75	–	–	–	–	Yes	Yes
	-5B	**-6/-6T**	**-75E**	**-75Z**	**-75**	**-75**

Notes: 1. The -5B device is backward compatible with all slower speed grades. The voltage range of -5B device operating at slower speed grades is $V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$.

Figure 1: 256Mb DDR SDRAM Part Numbers



FBGA Part Marking System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: www.micron.com.

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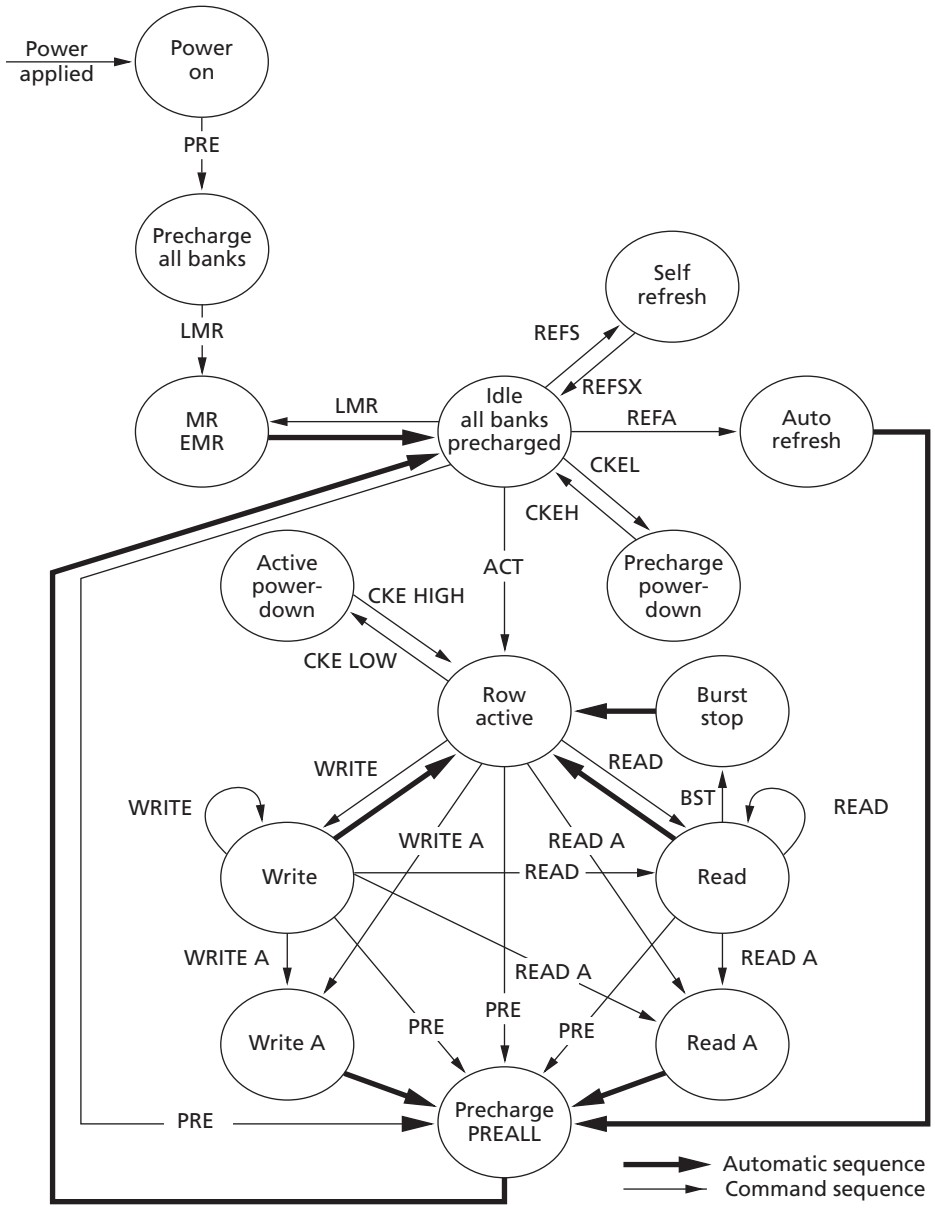
State Diagram

Figure 2: Simplified State Diagram



ACT = ACTIVE
BST = BURST TERMINATE
CKEH = Exit power-down
CKEL = Enter power-down
EMR = Extended mode register
LMR = LOAD MODE REGISTER
MR = Mode register
PRE = PRECHARGE
PREALL = PRECHARGE all banks
READ A = READ with auto precharge
REFA = AUTO REFRESH
REFS = Enter self refresh
REFSX = Exit self refresh
WRITE A = WRITE with auto precharge

Note: This diagram represents operations within a single bank only and does not capture concurrent operations in other banks.

Functional Description

The DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which may then be followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC standard for SSTL_2. All full-drive option outputs are SSTL_2, Class II compatible.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ[7:0]) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]) DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

Functional Block Diagrams

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a 4-bank DRAM.

Figure 3: 64 Meg x 4 Functional Block Diagram

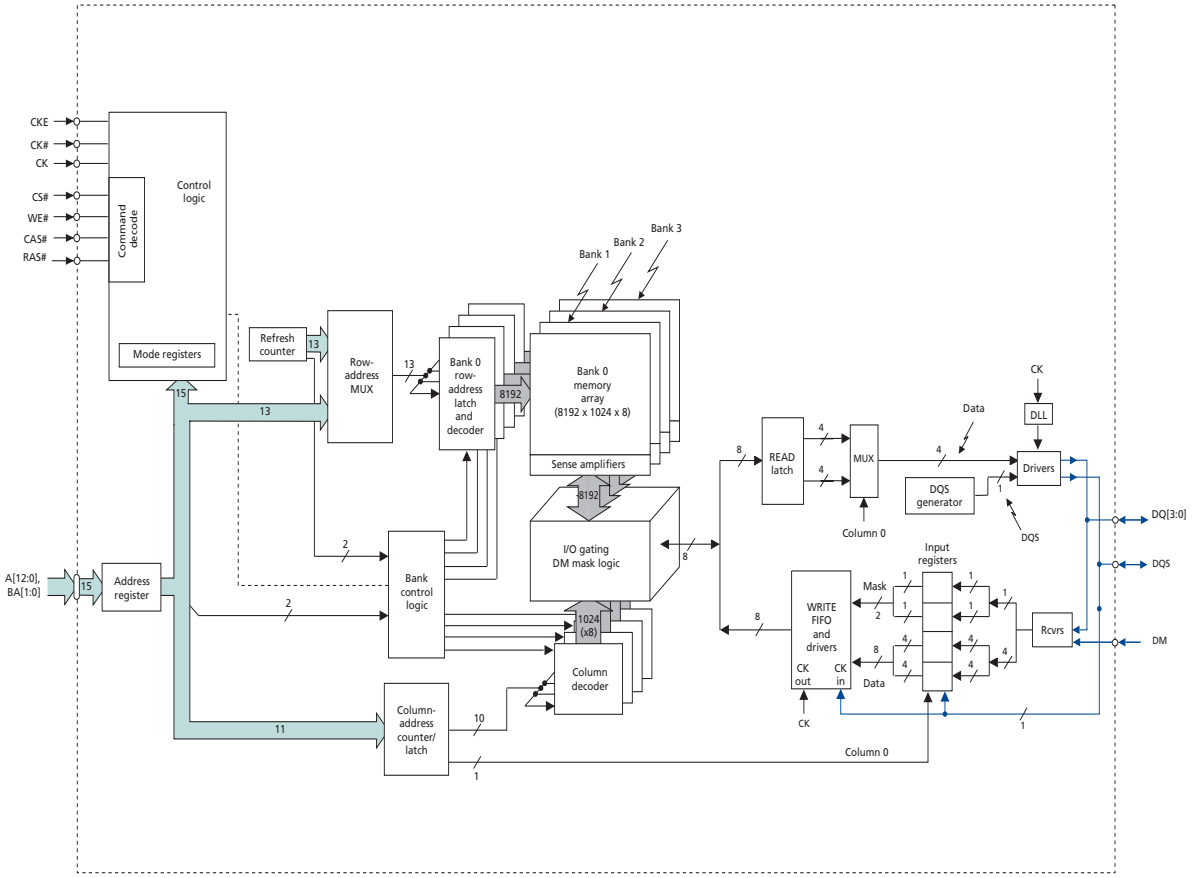


Figure 4: 32 Meg x 8 Functional Block Diagram

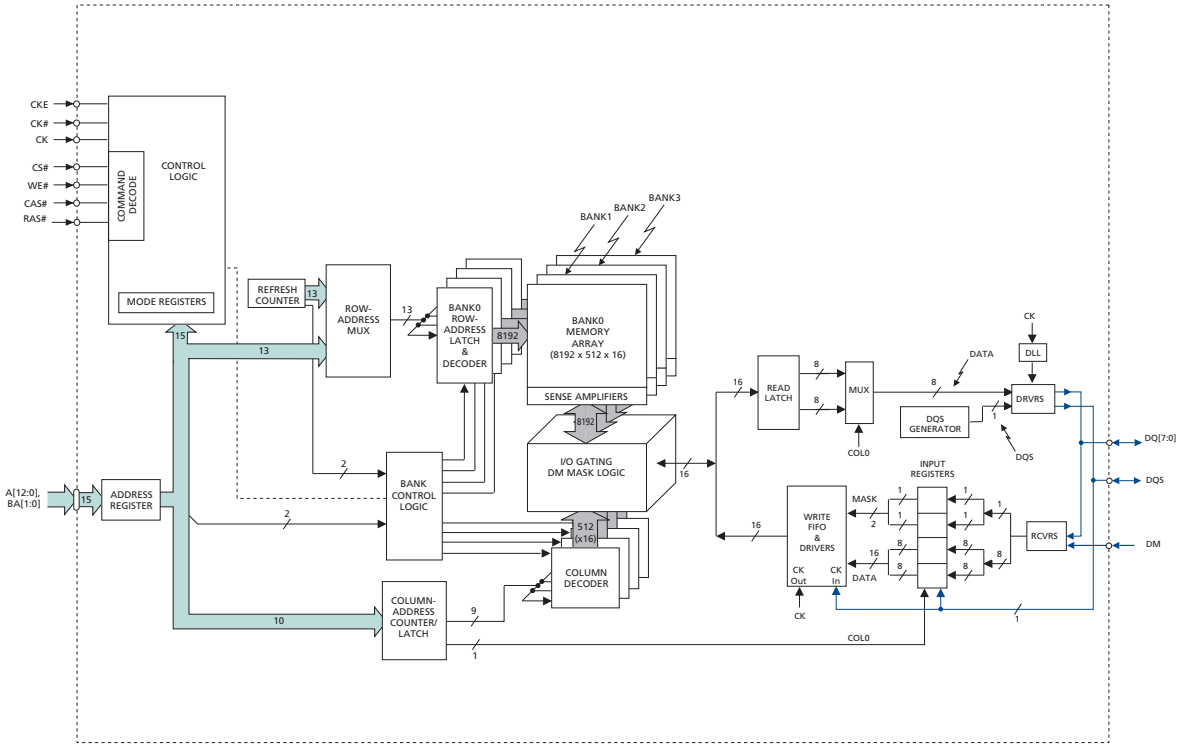
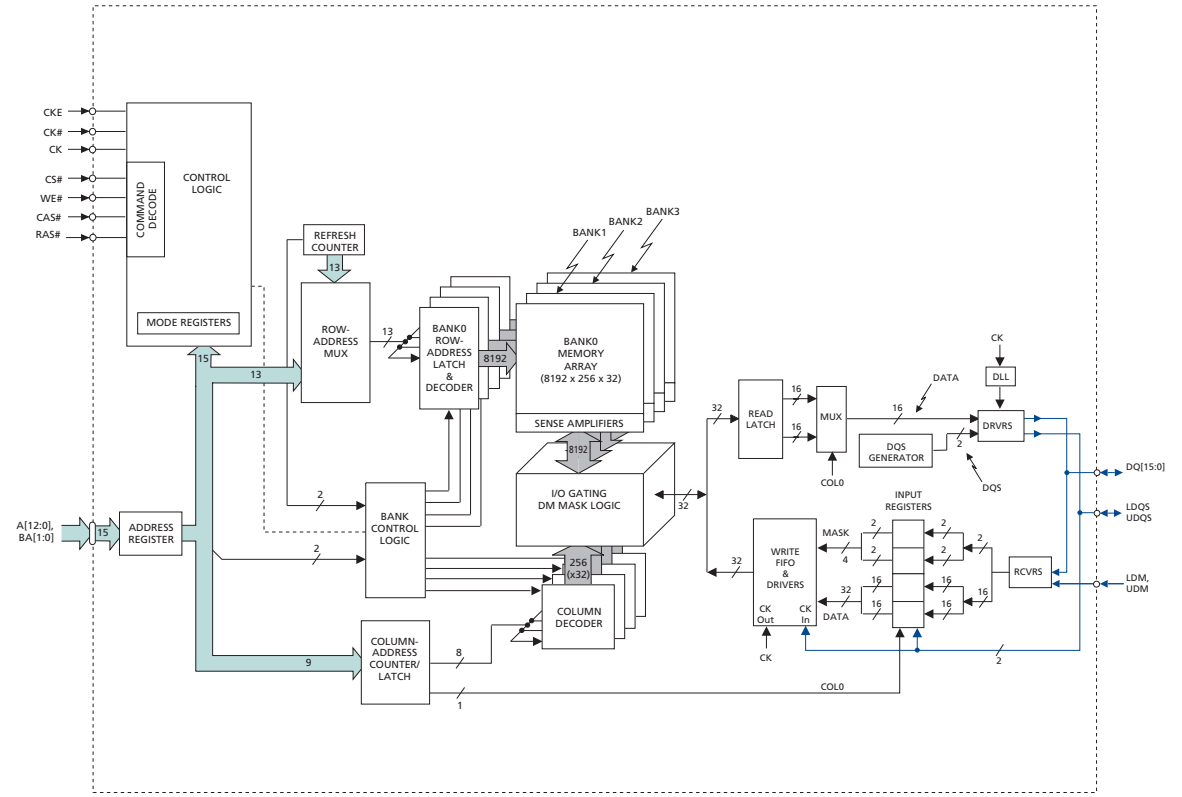


Figure 5: 16 Meg x 16 Functional Block Diagram



Pin and Ball Assignments and Descriptions

Figure 6: 66-Pin TSOP Pin Assignments (Top View)

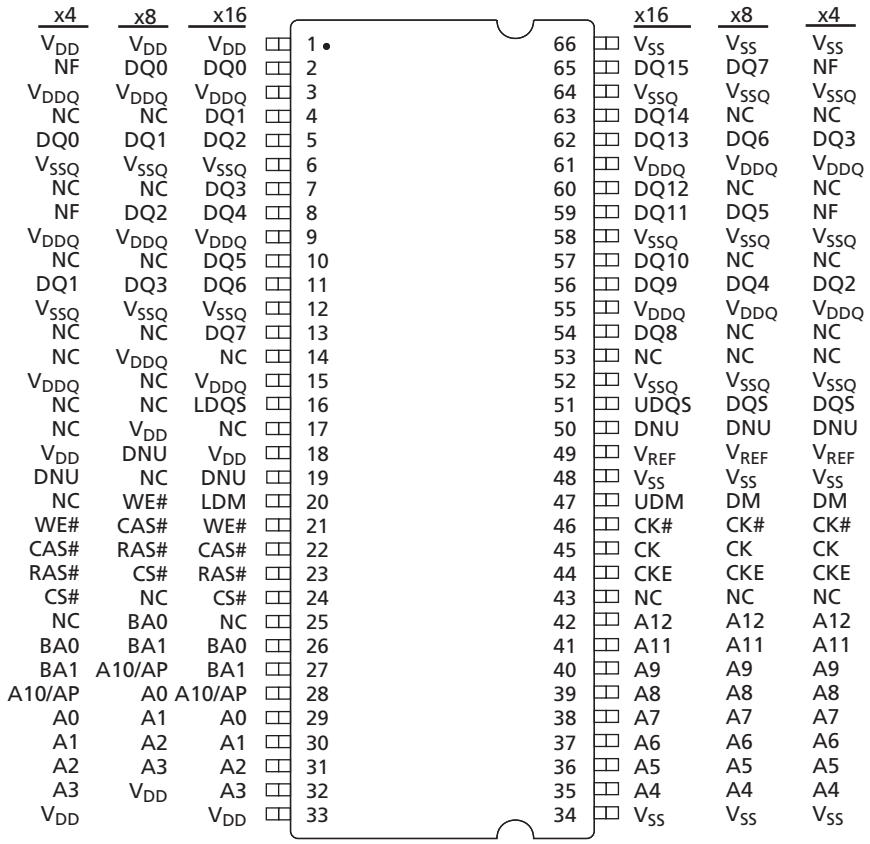


Figure 7: 60-Ball FBGA Ball Assignments (Top View)

x4 (Top View)

1	2	3	4 5 6	7	8	9
V_{SSQ}	NF	V_{SS}	A	V_{DD}	NF	V_{DDQ}
NC	V_{DDQ}	DQ3	B	DQ0	V_{SSQ}	NC
NC	V_{SSQ}	NF	C	NF	V_{DDQ}	NC
NC	V_{DDQ}	DQ2	D	DQ1	V_{SSQ}	NC
NC	V_{SSQ}	DQS	E	NC	V_{DDQ}	NC
V_{REF}	V_{SS}	DM	F	NC	V_{DD}	DNU
	CK	CK#	G	WE#	CAS#	
	A12	CKE	H	RAS#	CS#	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10	
	A6	A5	L	A2	A1	
	A4	V_{SS}	M	V_{DD}	A3	

x8 (Top View)

1	2	3	4 5 6	7	8	9
V_{SSQ}	DQ7	V_{SS}	A	V_{DD}	DQ0	V_{DDQ}
NC	V_{DDQ}	DQ6	B	DQ1	V_{SSQ}	NC
NC	V_{SSQ}	DQ5	C	DQ2	V_{DDQ}	NC
NC	V_{DDQ}	DQ4	D	DQ3	V_{SSQ}	NC
NC	V_{SSQ}	DQS	E	NC	V_{DDQ}	NC
V_{REF}	V_{SS}	DM	F	NC	V_{DD}	DNU
	CK	CK#	G	WE#	CAS#	
	A12	CKE	H	RAS#	CS#	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10	
	A6	A5	L	A2	A1	
	A4	V_{SS}	M	V_{DD}	A3	

x16 (Top View)

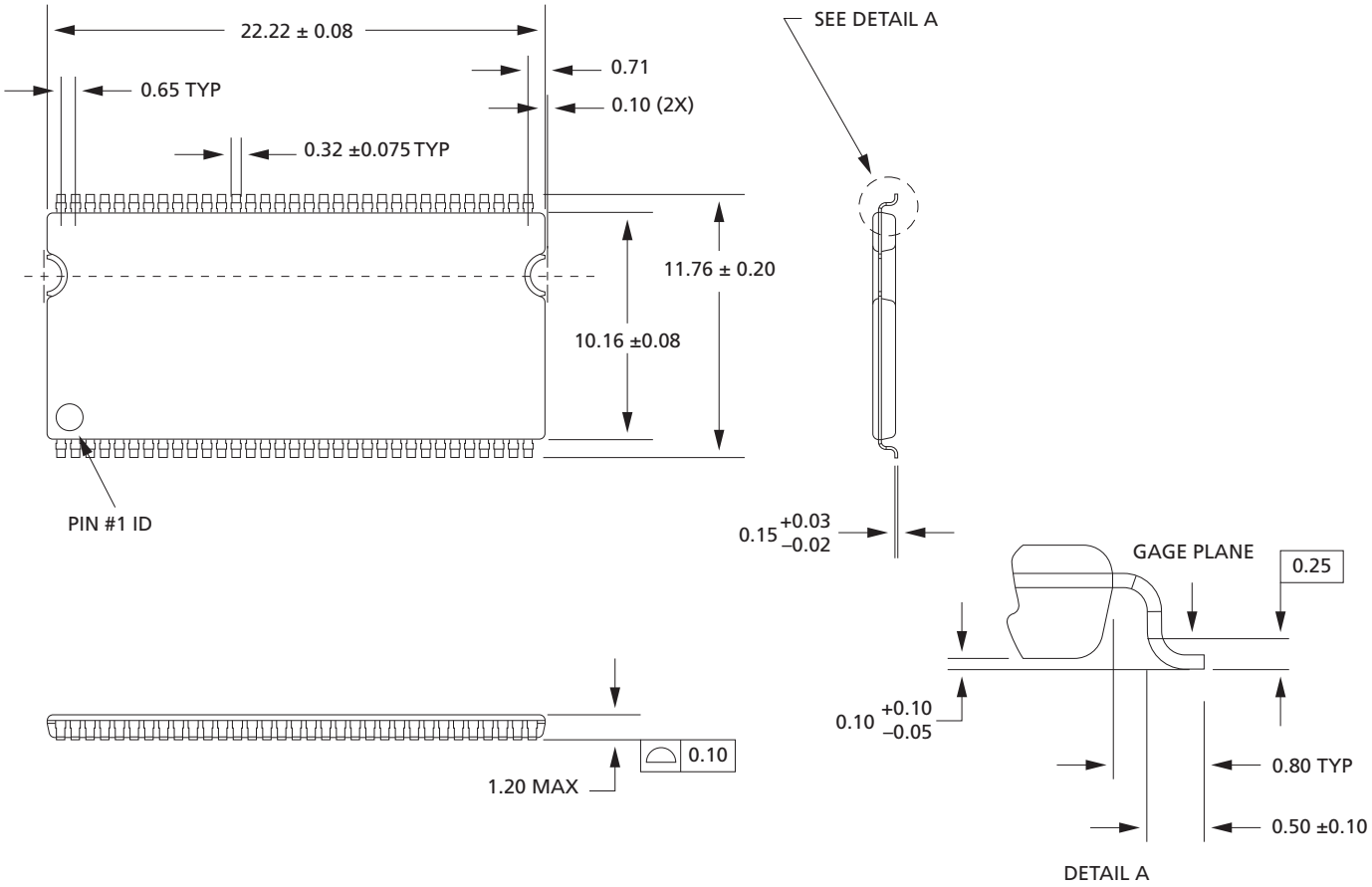
1	2	3	4 5 6	7	8	9
V_{SSQ}	DQ15	V_{SS}	A	V_{DD}	DQ0	V_{DDQ}
DQ14	V_{DDQ}	DQ13	B	DQ2	V_{SSQ}	DQ1
DQ12	V_{SSQ}	DQ11	C	DQ4	V_{DDQ}	DQ3
DQ10	V_{DDQ}	DQ9	D	DQ6	V_{SSQ}	DQ5
DQ8	V_{SSQ}	UDQS	E	LDQS	V_{DDQ}	DQ7
V_{REF}	V_{SS}	UDM	F	LDM	V_{DD}	DNU
	CK	CK#	G	WE#	CAS#	
	A12	CKE	H	RAS#	CS#	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10	
	A6	A5	L	A2	A1	
	A4	V_{SS}	M	V_{DD}	A3	

Table 4: Pin and Ball Descriptions

Symbol	Type	Description
A[12:0]	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[1:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
BA[1:0]	Input	**Bank address inputs:** BA[1:0] define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[1:0] also define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER (LMR) command.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle) or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
DM LDM, UDM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For x16 devices, LDM is DM for DQ[7:0], and UDM is DM for DQ[15:8]. Pin 20 is NC on x4 and x8 devices.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.
DQ[15:0]	I/O	**Data input/output:** Data bus for x16 devices.
DQ[7:0]	I/O	**Data input/output:** Data bus for x8 devices.
DQ[3:0]	I/O	**Data input/output:** Data bus for x4 devices.
DQS LDQS, UDQS	I/O	**Data strobe:** Output with read data; input with write data. DQS is edge-aligned with read data; centered in write data. It is used to capture data. For x16 devices, LDQS is DQS for DQ[7:0], and UDQS is DQS for DQ[15:8]. Pin 16 (E7) is NC for x4 and x8 devices.
V_{DD}	Supply	Power supply.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{REF}	Supply	SSTL_2 reference voltage.
NC	–	**No connect for x16, x8, x4:** These pins should be left unconnected.
DNU	–	**Do not use:** Must float to minimize noise on V_{REF}.

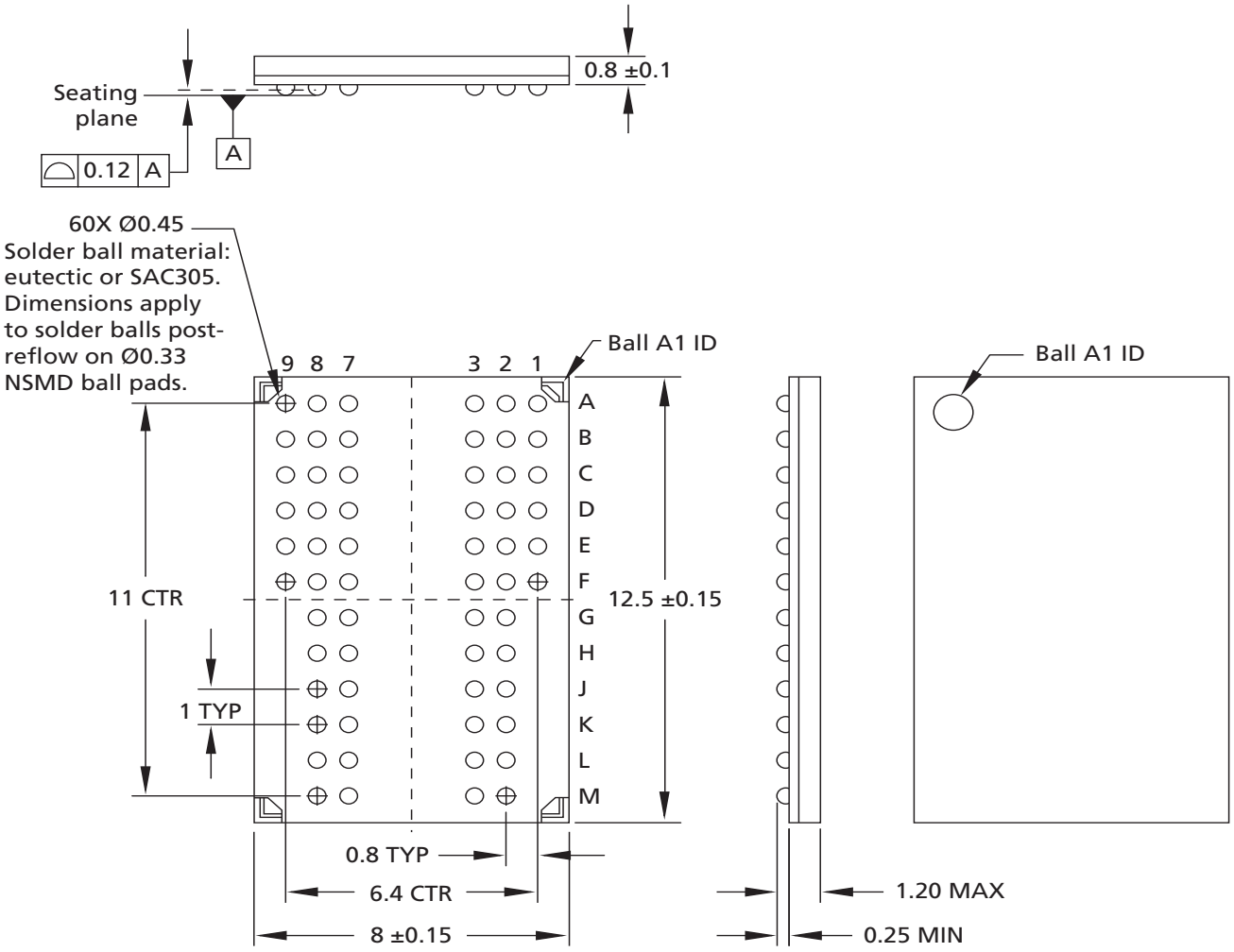
Package Dimensions

Figure 8: 66-Pin Plastic TSOP (400 mil)



Notes:
1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. Not all packages will have the half-moon shaped notches as shown.

Figure 9: 60-Ball FBGA (8mm x 12.5mm)



Notes:
1. All dimensions are in millimeters.
2. Topside part marking decoder can be found on Micron's Web site.

Electrical Specifications – I_{DD}

Table 5: I_{DD} Specifications and Conditions (x4, x8, x16: -5B, -6, -6T) – Die Revision K

V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V (-5B); V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V (-6, -6T); 0°C ≤ T_A ≤ 70°C; Notes: 6–5, 11, 13, 15, 47; Notes appear on pages 35–40; See also Table 7 on page 18

Parameter/Condition		Symbol	-5B	-6/6T	Units	Notes
Operating one-bank precharge current: ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	100	90	mA	23, 48
Operating one-bank active-read-precharge current: Burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	120	115	mA	23, 48
Precharge power-down standby current: All banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD2P}	4	4	mA	24, 33
Idle standby current: CS# = HIGH; All banks are idle; ^tCK = ^tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS, and DM		I_{DD2F}	50	50	mA	51
Active power-down standby current: One bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD3P}	35	30	mA	24, 33
Active standby current: CS# = HIGH; CKE = HIGH; One bank active; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	60	55	mA	23
Operating burst read current: Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); I_{OUT} = 0mA		I_{DD4R}	180	160	mA	23, 48
Operating burst write current: Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	180	160	mA	23
Auto refresh burst current:	^tREFC = ^tRFC (MIN)	I_{DD5}	160	160	mA	50
	^tREFC =7.8µs	I_{DD5A}	6	6	mA	28, 50
Self refresh current: CKE ≤ 0.2V	Standard	I_{DD6}	4	4	mA	12
	Low power (L)	I_{DD6A}	2	2	mA	12
Operating bank interleave read current: Four-bank interleaving READs (burst = 4) with auto precharge; ^tRC = minimum ^tRC allowed; ^tCK = ^tCK (MIN); Address and control inputs change only during ACTIVE, READ, or WRITE commands		I_{DD7}	290	270	mA	23, 49

Table 6: I_{DD} Specifications and Conditions (x4, x8, x16: -5B, -6, -6T) – Die Revision M

V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V (-5B); V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V (-6, -6T);
0°C ≤ T_A ≤ 70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 35–40; See also Table 7 on page 18

Parameter/Condition		Symbol	-5B	-6/6T	Units	Notes
Operating one-bank precharge current: $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	75	65	mA	23, 48
Operating one-bank active-read-precharge current: Burst = 4; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	85	75	mA	23, 48
Precharge power-down standby current: All banks idle; Power-down mode; $^tCK = ^tCK$ (MIN); CKE = LOW		I_{DD2P}	4	4	mA	24, 33
Idle standby current: CS# = HIGH; All banks are idle; $^tCK = ^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS, and DM		I_{DD2F}	23	23	mA	51
Active power-down standby current: One bank active; Power-down mode; $^tCK = ^tCK$ (MIN); CKE = LOW		I_{DD3P}	14	14	mA	24, 33
Active standby current: CS# = HIGH; CKE = HIGH; One bank active; $^tRC = ^tRAS$ (MAX); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	30	30	mA	23
Operating burst read current: Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); I_{OUT} = 0mA		I_{DD4R}	105	95	mA	23, 48
Operating burst write current: Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	105	95	mA	23
Auto refresh burst current:	$^tREFC = ^tRFC$ (MIN)	I_{DD5}	115	105	mA	50
	^tREFC = 7.8µs	I_{DD5A}	6	6	mA	28, 50
Self refresh current: CKE ≤ 0.2V	Standard	I_{DD6}	4	4	mA	12
	Low power (L)	I_{DD6A}	2	2	mA	12
Operating bank interleave read current: Four-bank interleaving READs (burst = 4) with auto precharge; ^tRC = minimum ^tRC allowed; $^tCK = ^tCK$ (MIN); Address and control inputs change only during ACTIVE, READ, or WRITE commands		I_{DD7}	175	175	mA	23, 49

Electrical Specifications – DC and AC

Stresses greater than those listed in Table 7 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Parameter	Min	Max	Units
V_{DD} supply voltage relative to V_{SS}	–1V	3.6V	V
V_{DDQ} supply voltage relative to V_{SS}	–1V	3.6V	V
V_{REF} and inputs voltage relative to V_{SS}	–1V	3.6V	V
I/O pins voltage relative to V_{SS}	–0.5V	V_{DDQ} + 0.5V	V
Storage temperature (plastic)	–55	150	°C
Short circuit output current	–	50	mA

Table 8: DC Electrical Characteristics and Operating Conditions (-5B)

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 35; V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		V_{DD}	2.5	2.7	V	37, 42
I/O supply voltage		V_{DDQ}	2.5	2.7	V	37, 42, 45
I/O reference voltage		V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	7, 45
I/O termination voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	8, 45
Input high (logic 1) voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V	29
Input low (logic 0) voltage		$V_{IL(DC)}$	–0.3	V_{REF} - 0.15	V	29
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)		I_I	–2	2	µA	
Output leakage current: (DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})		I_{OZ}	–5	5	µA	
Full-drive option output levels (x4, x8, x16):	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	–16.8	–	mA	38, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	16.8	–	mA	
Reduced-drive option output levels (Design Revision F and K only):	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OHR}	–9	–	mA	39, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OLR}	9	–	mA	
Ambient operating temperatures	Commercial	T_A	0	70	°C	
	Industrial	T_A	–40	85	°C	

Table 9: DC Electrical Characteristics and Operating Conditions (-6, -6T, -75E, -75Z, -75)

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 35; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

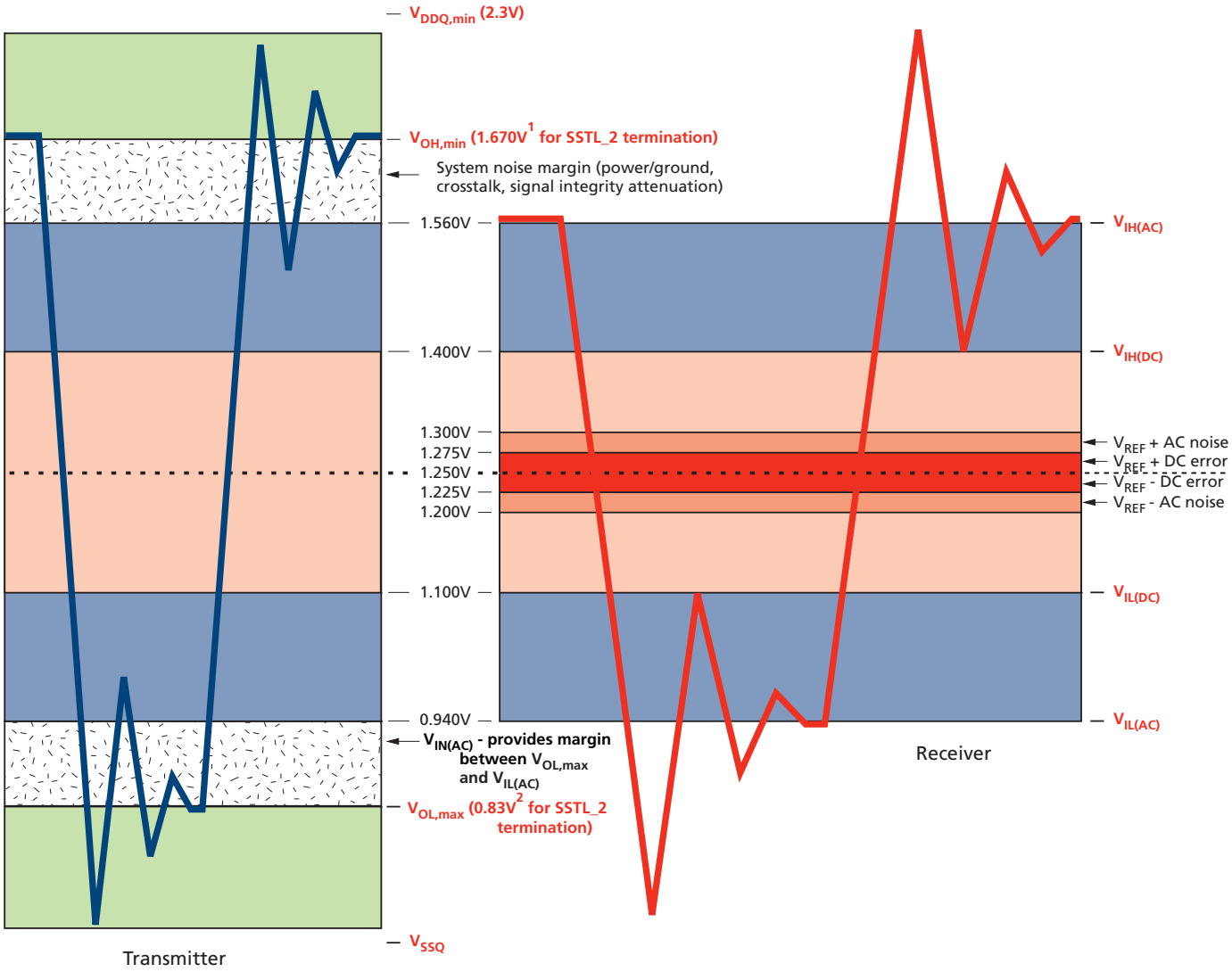
Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		V_{DD}	2.3	2.7	V	37, 42
I/O supply voltage		V_{DDQ}	2.3	2.7	V	37, 42, 45
I/O reference voltage		V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	7, 45
I/O termination voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	8, 45
Input high (logic 1) voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V	29
Input low (logic 0) voltage		$V_{IL(DC)}$	–0.3	V_{REF} - 0.15	V	29
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)		I_I	–2	2	µA	
Output leakage current: (DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})		I_{OZ}	–5	5	µA	
Full-drive option output levels (x4, x8, x16):	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	–16.8	–	mA	38, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	16.8	–	mA	
Reduced-drive option output levels (Design Revision F and K only):	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OHR}	–9	–	mA	39, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OLR}	9	–	mA	
Ambient operating temperatures	Commercial	T_A	0	70	°C	
	Industrial	T_A	–40	85	°C	

Table 10: AC Input Operating Conditions

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 35;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V (V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V for -5B)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage	$V_{IH(AC)}$	V_{REF} + 0.310	–	V	15, 29, 41
Input low (logic 0) voltage	$V_{IL(AC)}$	–	V_{REF} - 0.310	V	15, 29, 41
I/O reference voltage	$V_{REF(AC)}$	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	7

Figure 10: Input Voltage Waveform



Notes:
1. $V_{OH,min}$ with test load is 1.927V.
2. $V_{OL,max}$ with test load is 0.373V.
3. Numbers in diagram reflect nominal values utilizing circuit below for all devices other than -5B.

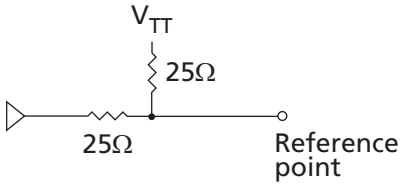
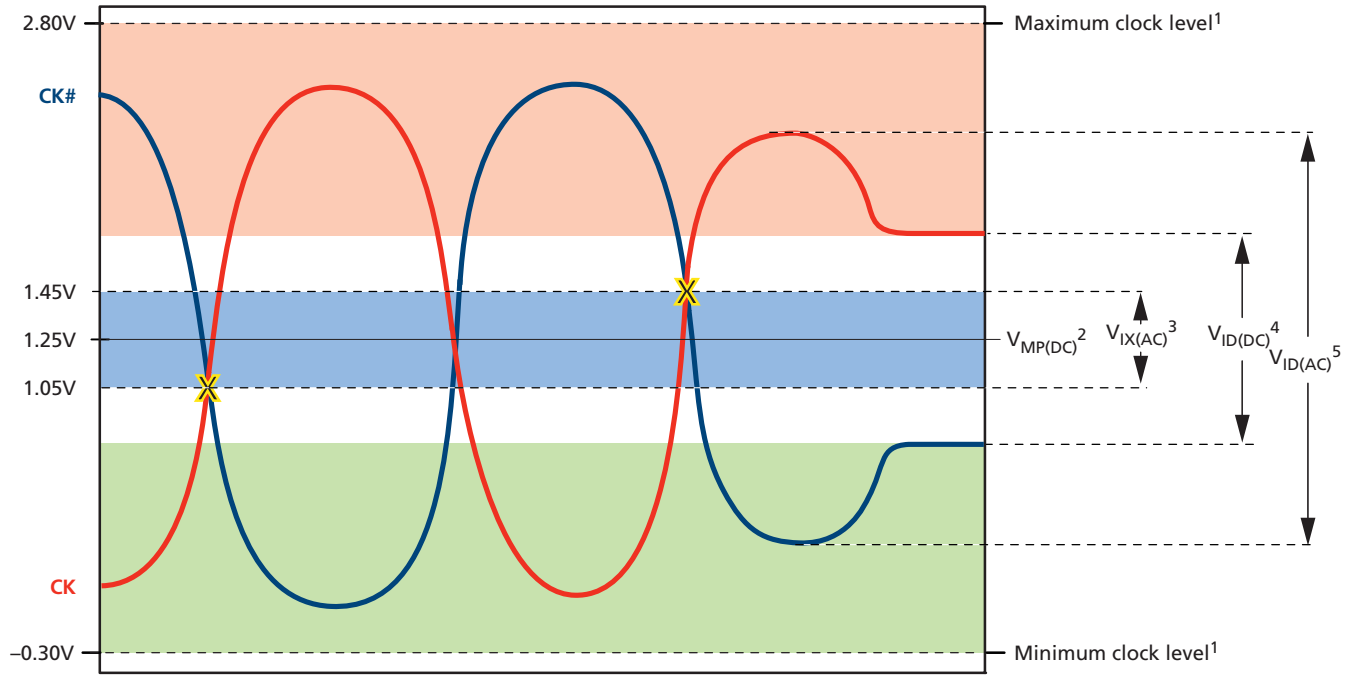


Table 11: Clock Input Operating Conditions

Notes: 1–5, 16, 17, and 31 apply to the entire table; Notes appear on page 35;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V (V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V for -5B)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input mid-point voltage: CK and CK#	$V_{MP(DC)}$	1.15	1.35	V	7, 10
Clock input voltage level: CK and CK#	$V_{IN(DC)}$	–0.3	V_{DDQ} + 0.3	V	7
Clock input differential voltage: CK and CK#	$V_{ID(DC)}$	0.36	V_{DDQ} + 0.6	V	7, 9
Clock input differential voltage: CK and CK#	$V_{ID(AC)}$	0.7	V_{DDQ} + 0.6	V	9
Clock input crossing point voltage: CK and CK#	$V_{IX(AC)}$	0.5 × V_{DDQ} - 0.2	0.5 × V_{DDQ} + 0.2	V	10

Figure 11: SSTL_2 Clock Input



Notes:
1. CK or CK# may not be more positive than V_{DDQ} + 0.3V or more negative than V_{SS} - 0.3V.
2. This provides a minimum of 1.15V to a maximum of 1.35V and is always half of V_{DDQ}.
3. CK and CK# must cross in this region.
4. CK and CK# must meet at least $V_{ID(DC),min}$ when static and is centered around $V_{MP(DC)}$.
5. CK and CK# must have a minimum 700mV peak-to-peak swing.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values for all devices other than -5B.

Table 12: Capacitance (x4, x8 TSOP)
Note: 14 applies to the entire table; Notes appear on page 35

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ[3:0] (x4), DQ[7:0] (x8)	DC_{IO}	–	0.50	pF	25
Delta input capacitance: Command and address	DC_{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC_{I2}	–	0.25	pF	30
Input/output capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF	
Input capacitance: Command and address	C_{I1}	2.0	3.0	pF	
Input capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input capacitance: CKE	C_{I3}	2.0	3.0	pF	

Table 13: Capacitance (x4, x8 FBGA)
Note: 14 applies to the entire table; Notes appear on page 35

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ, DQS, DM	DC_{IO}	–	0.50	pF	25
Delta input capacitance: Command and address	DC_{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC_{I2}	–	0.25	pF	30
Input/output capacitance: DQ, DQS, DM	C_{IO}	3.5	4.5	pF	
Input capacitance: Command and address	C_{I1}	1.5	2.5	pF	
Input capacitance: CK, CK#	C_{I2}	1.5	2.5	pF	
Input capacitance: CKE	C_{I3}	1.5	2.5	pF	

Table 14: Capacitance (x16 TSOP)
Note: 14 applies to the entire table; Notes appear on page 35

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ[7:0], LDQS, LDM	DC_{IOL}	–	0.50	pF	25
Delta input/output capacitance: DQ[15:8], UDQS, UDM	DC_{IOU}	–	0.50	pF	25
Delta input capacitance: Command and address	DC_{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC_{I2}	–	0.25	pF	30
Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM	C_{IO}	4.0	5.0	pF	
Input capacitance: Command and address	C_{I1}	2.0	3.0	pF	
Input capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input capacitance: CKE	C_{I3}	2.0	3.0	pF	

Table 15: Capacitance (x16 FBGA)
Note: 14 applies to the entire table; Notes appear on page 35

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ[7:0], LDQS, LDM	DC_{IOL}	–	0.50	pF	25
Delta input/output capacitance: DQ[15:8], UDQS, UDM	DC_{IOU}	–	0.50	pF	25
Delta input capacitance: Command and address	DC_{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC_{I2}	–	0.25	pF	30
Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM	C_{IO}	3.5	4.5	pF	
Input capacitance: Command and address	C_{I1}	1.5	2.5	pF	
Input capacitance: CK, CK#	C_{I2}	1.5	2.5	pF	
Input capacitance: CKE	C_{I3}	1.5	2.5	pF	

Table 16: Electrical Characteristics and Recommended AC Operating Conditions (-5B)

Notes 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 35;
$0°C \le T_A \le 70°C$; V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V

AC Characteristics			-5B			
Parameter		**Symbol**	**Min**	**Max**	**Units**	**Notes**
Access window of DQ from CK/CK#		^{t}AC	–0.70	0.70	ns	
CK high-level width		^{t}CH	0.45	0.55	^{t}CK	31
Clock cycle time	CL = 3	^{t}CK (3)	5	7.5	ns	52
	CL = 2.5	^{t}CK (2.5)	6	13	ns	46, 52
	CL = 2	^{t}CK (2)	7.5	13	ns	46, 52
CK low-level width		^{t}CL	0.45	0.55	^{t}CK	31
DQ and DM input hold time relative to DQS		^{t}DH	0.40	–	ns	27, 32
DQ and DM input pulse width (for each input)		^{t}DIPW	1.75	–	ns	32
Access window of DQS from CK/CK#		^{t}DQSCK	–0.60	0.60	ns	
DQS input high pulse width		^{t}DQSH	0.35	–	^{t}CK	
DQS input low pulse width		^{t}DQSL	0.35	–	^{t}CK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^{t}DQSQ	–	0.40	ns	26, 27
WRITE command to first DQS latching transition		^{t}DQSS	0.72	1.28	^{t}CK	
DQ and DM input setup time relative to DQS		^{t}DS	0.40	–	ns	27, 32
DQS falling edge from CK rising – hold time		^{t}DSH	0.2	–	^{t}CK	
DQS falling edge to CK rising – setup time		^{t}DSS	0.2	–	^{t}CK	
Half-clock period		^{t}HP	^{t}CH,^{t}CL	–	ns	35
Data-out High-Z window from CK/CK#		^{t}HZ	–	0.70	ns	19, 43
Address and control input hold time (slew rate ≥0.5 V/ns)		$^{t}IH_F$	0.60	–	ns	15
Address and control input pulse width (for each input)		^{t}IPW	2.2	–	ns	
Address and control input setup time (fast slew rate)		$^{t}IS_F$	0.60	–	ns	15
Address and control input setup time (slow slew rate)		$^{t}IS_S$	0.70	–	ns	
Data-out Low-Z window from CK/CK#		^{t}LZ	–0.70	–	ns	19, 43
LOAD MODE REGISTER command cycle time		^{t}MRD	10	–	ns	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		^{t}QH	^{t}HP -^{t}QHS	–	ns	26, 27
Data hold skew factor		^{t}QHS	–	0.50	ns	
ACTIVE-to-READ with auto precharge command		^{t}RAP	15	–	ns	
ACTIVE-to-PRECHARGE command		^{t}RAS	40	70,000	ns	36
ACTIVE-to-ACTIVE/AUTO REFRESH command period		^{t}RC	55	–	ns	55
ACTIVE-to-READ or WRITE delay		^{t}RCD	15	–	ns	
REFRESH-to-REFRESH command interval		^{t}REFC	–	70.3	µs	24
Average periodic refresh interval		^{t}REFI	–	7.8	µs	24
AUTO REFRESH command period		^{t}RFC	70	–	ns	50
PRECHARGE command period		^{t}RP	15	–	ns	
DQS read preamble		^{t}RPRE	0.9	1.1	^{t}CK	44
DQS read postamble		^{t}RPST	0.4	0.6	^{t}CK	44
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	10	–	ns	
Terminating voltage delay to V_{DD}		^{t}VTD	0	–	ns	
DQS write preamble		^{t}WPRE	0.25	–	^{t}CK	
DQS write preamble setup time		^{t}WPRES	0	–	ns	21, 22
DQS write postamble		^{t}WPST	0.4	0.6	^{t}CK	20
Write recovery time		^{t}WR	15	–	ns	

Table 16: Electrical Characteristics and Recommended AC Operating Conditions (-5B) (continued)
Notes 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 35;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V

AC Characteristics		-5B			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Internal WRITE-to-READ command delay	^{t}WTR	2	–	^{t}CK	
Exit SELF REFRESH-to-non-READ command	^{t}XSNR	70	–	ns	
Exit SELF REFRESH-to-READ command	^{t}XSRD	200	–	^{t}CK	
Data valid output window	n/a	^{t}QH - ^{t}DQSQ		ns	26

Table 17: Electrical Characteristics and Recommended AC Operating Conditions (-6)

Notes: 1–6, 16–18, 34 apply to the entire table; Notes appear on page 35;
$0°C \le T_A \le 70°C$; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

AC Characteristics			-6 (FBGA)			
Parameter		**Symbol**	**Min**	**Max**	**Units**	**Notes**
Access window of DQ from CK/CK#		^tAC	–0.70	0.70	ns	
CK high-level width		^tCH	0.45	0.55	^tCK	31
Clock cycle time	CL = 2.5	^tCK (2.5)	6	13	ns	46, 52
	CL = 2	^tCK (2)	7.5	13	ns	46, 52
CK low-level width		^tCL	0.45	0.55	^tCK	31
DQ and DM input hold time relative to DQS		^tDH	0.45	–	ns	27, 32
DQ and DM input pulse width (for each input)		^tDIPW	1.75	–	ns	32
Access window of DQS from CK/CK#		^tDQSCK	–0.6	0.6	ns	
DQS input high pulse width		^tDQSH	0.35	–	^tCK	
DQS input low pulse width		^tDQSL	0.35	–	^tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	–	0.4	ns	26, 27
WRITE command to first DQS latching transition		^tDQSS	0.75	1.25	^tCK	
DQ and DM input setup time relative to DQS		^tDS	0.45	–	ns	27, 32
DQS falling edge from CK rising - hold time		^tDSH	0.2	–	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2	–	^tCK	
Half-clock period		^tHP	^tCH, ^tCL	–	ns	35
Data-out High-Z window from CK/CK#		^tHZ	–	0.7	ns	19, 43
Address and control input hold time (fast slew rate)		^tIH_F	0.75	–	ns	
Address and control input hold time (slow slew rate)		^tIH_S	0.8	–	ns	15
Address and control input pulse width (for each input)		^tIPW	2.2	–	ns	
Address and control input setup time (fast slew rate)		^tIS_F	0.75	–	ns	
Address and control input setup time (slow slew rate)		^tIS_S	0.8	–	ns	15
Data-out Low-Z window from CK/CK#		^tLZ	–0.7	–	ns	19, 43
LOAD MODE REGISTER command cycle time		^tMRD	12	–	ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS	–	ns	26, 27
Data hold skew factor		^tQHS	–	0.50	ns	
ACTIVE-to-READ with auto precharge command		^tRAP	15	–	ns	
ACTIVE-to-PRECHARGE command		^tRAS	42	70,000	ns	36, 54
ACTIVE-to-ACTIVE/AUTO REFRESH command period		^tRC	60	–	ns	55
ACTIVE-to-READ or WRITE delay		^tRCD	15	–	ns	
REFRESH-to-REFRESH command interval		^tREFC	–	70.3	µs	24
Average periodic refresh interval		^tREFI	–	7.8	µs	24
AUTO REFRESH command period		^tRFC	72	–	ns	50
PRECHARGE command period		^tRP	15	–	ns	
DQS read preamble		^tRPRE	0.9	1.1	^tCK	44
DQS read postamble		^tRPST	0.4	0.6	^tCK	44
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	12	–	ns	
Terminating voltage delay to V_{SS}		^tVTD	0	–	ns	
DQS write preamble		^tWPRE	0.25	–	^tCK	
DQS write preamble setup time		^tWPRES	0	–	ns	21, 22
DQS write postamble		^tWPST	0.4	0.6	^tCK	20
Write recovery time		^tWR	15	–	ns	