



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Double Data Rate (DDR) SDRAM

**MT46V128M4 – 32 Meg x 4 x 4 banks**
**MT46V64M8 – 16 Meg x 8 x 4 banks**
**MT46V32M16 – 8 Meg x 16 x 4 banks**

## Features

- $V_{DD} = 2.5V \pm 0.2V$ ,  $V_{DDQ} = 2.5V \pm 0.2V$   
 $V_{DD} = 2.6V \pm 0.1V$ ,  $V_{DDQ} = 2.6V \pm 0.1V$  (DDR400)<sup>1</sup>
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto refresh
  - 64ms, 8192-cycle
- Longer-lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL\_2 compatible)
- Concurrent auto precharge option is supported
- <sup>t</sup>RAS lockout supported (<sup>t</sup>RAP = <sup>t</sup>RCD)

## Options

- Configuration
  - 128 Meg x 4 (32 Meg x 4 x 4 banks) 128M4
  - 64 Meg x 8 (16 Meg x 8 x 4 banks) 64M8
  - 32 Meg x 16 (8 Meg x 16 x 4 banks) 32M16
- Plastic package
  - 66-pin TSOP TG
  - 66-pin TSOP (Pb-free) P
  - 60-ball FBGA (10mm x 12.5mm) FN<sup>2</sup>
  - 60-ball FBGA (10mm x 12.5mm) (Pb-free) BN<sup>2</sup>
  - 60-ball FBGA (8mm x 12.5mm) CV<sup>3</sup>
  - 60-ball FBGA (8mm x 12.5mm) (Pb-free) CY<sup>3</sup>
- Timing – cycle time
  - 5ns @ CL = 3 (DDR400) -5B
  - 6ns @ CL = 2.5 (DDR333) (FBGA only) -6<sup>2</sup>
  - 6ns @ CL = 2.5 (DDR333) (TSOP only) -6T<sup>2</sup>
- Self refresh
  - Standard None
  - Low-power self refresh L
- Temperature rating
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT
- Revision
  - x4, x8, x16 :F
  - x4, x8, x16 :J

Notes: 1. DDR400 devices operating at  $\leq$  DDR333 conditions can use  $V_{DD}/V_{DDQ} = 2.5V \pm 0.2V$ .

2. Available only on Revision F.

3. Available only on Revision J.

**Table 1: Key Timing Parameters**

CL = CAS (READ) latency; data-out window is MIN clock rate with 50% duty cycle at CL = 2, CL = 2.5, or CL = 3

Speed Grade	Clock Rate (MHz)			Data-Out Window	Access Window	DQS-DQ Skew
	CL = 2	CL = 2.5	CL = 3			
-5B	133	167	200	1.6ns	$\pm 0.70$ ns	0.40ns
-6	133	167	n/a	2.1ns	$\pm 0.70$ ns	0.40ns
6T	133	167	n/a	2.0ns	$\pm 0.70$ ns	0.45ns
-75E/-75Z	133	133	n/a	2.5ns	$\pm 0.75$ ns	0.50ns
-75	100	133	n/a	2.5ns	$\pm 0.75$ ns	0.50ns

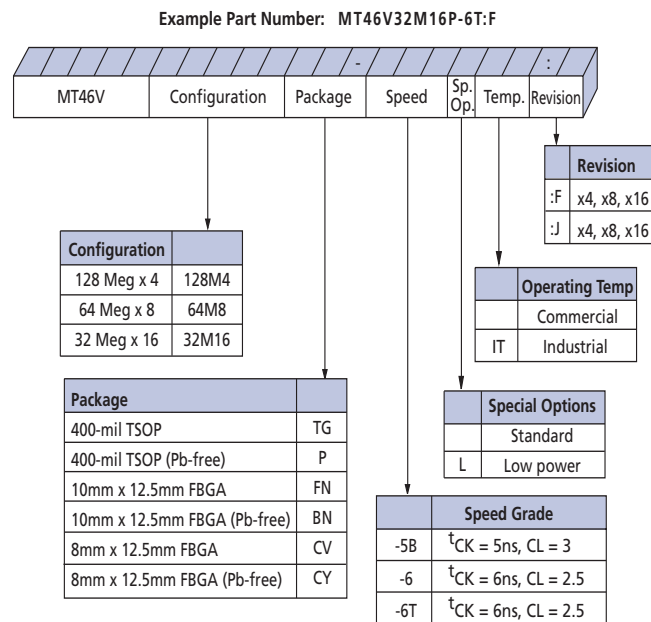
**Table 2: Addressing**

Parameter	128 Meg x 4	64 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank address	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column address	4K (A0–A9, A11, A12)	2K (A0–A9, A11)	1K (A0–A9)

**Table 3: Speed Grade Compatibility**

Marking	PC3200 (3-3-3)	PC2700 (2.5-3-3)	PC2100 (2-2-2)	PC2100 (2-3-3)	PC2100 (2.5-3-3)	PC1600 (2-2-2)
<b>-5B<sup>1</sup></b>	Yes	Yes	Yes	Yes	Yes	Yes
<b>-6</b>	–	Yes	Yes	Yes	Yes	Yes
<b>-6T</b>	–	Yes	Yes	Yes	Yes	Yes
<b>-75E</b>	–	–	Yes	Yes	Yes	Yes
<b>-75Z</b>	–	–	–	Yes	Yes	Yes
<b>-75</b>	–	–	–	–	Yes	Yes
	<b>-5B</b>	<b>-6/-6T</b>	<b>-75E</b>	<b>-75Z</b>	<b>-75</b>	<b>-75</b>

Notes: 1. The -5B device is backward compatible with all slower speed grades. The voltage range of -5B device operating at slower speed grades is  $V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$ .

**Figure 1: 512Mb DDR SDRAM Part Numbers**


### FBGA Part Number System

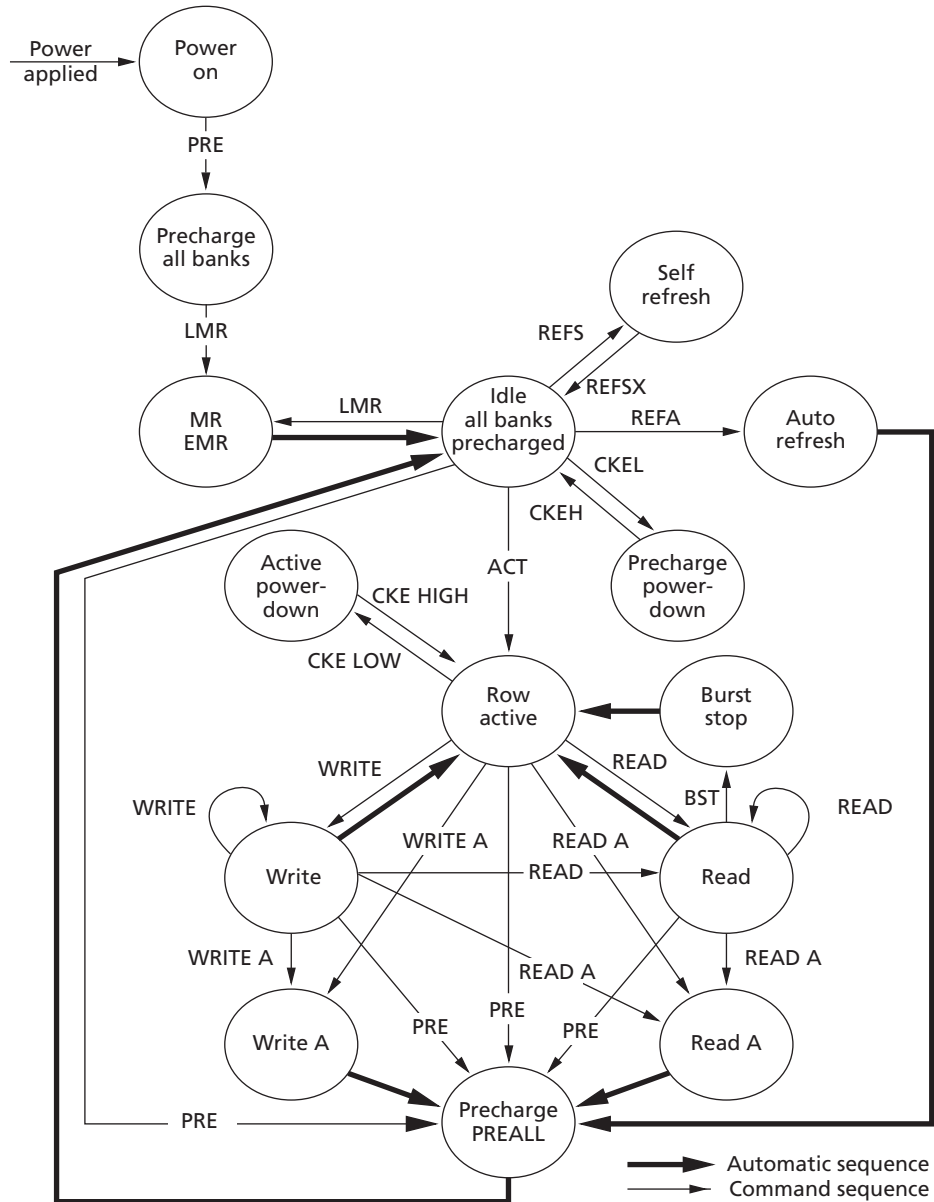
Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: [www.micron.com](http://www.micron.com).

**Table of Contents**

State Diagram	4
Functional Description	5
General Notes	5
Functional Block Diagrams	6
Pin and Ball Assignments and Descriptions	8
Package Dimensions	12
Electrical Specifications – I <sub>DD</sub>	15
Electrical Specifications – DC and AC	20
Notes	37
Commands	45
DESELECT	49
NO OPERATION (NOP)	49
LOAD MODE REGISTER (LMR)	49
ACTIVE (ACT)	50
READ	51
WRITE	52
PRECHARGE (PRE)	53
BURST TERMINATE (BST)	53
AUTO REFRESH (AR)	53
SELF REFRESH	53
Operations	54
INITIALIZATION	54
REGISTER DEFINITION	57
ACTIVE	61
READ	62
WRITE	74
PRECHARGE	87
AUTO REFRESH	89
SELF REFRESH	90
Power-down (CKE Not Active)	92

## State Diagram

Figure 2: Simplified State Diagram



ACT = ACTIVE  
 BST = BURST TERMINATE  
 CKEH = Exit power-down  
 CKEL = Enter power-down  
 EMR = Extended mode register  
 LMR = LOAD MODE REGISTER  
 MR = Mode register

PRE = PRECHARGE  
 PREALL = PRECHARGE all banks  
 READ A = READ with auto precharge  
 REFA = AUTO REFRESH  
 REFS = Enter self refresh  
 REFSX = Exit self refresh  
 WRITE A = WRITE with auto precharge

Note: This diagram represents operations within a single bank only and does not capture concurrent operations in other banks.

## Functional Description

The DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single  $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which may then be followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC standard for SSTL\_2. All full-drive option outputs are SSTL\_2, Class II compatible.

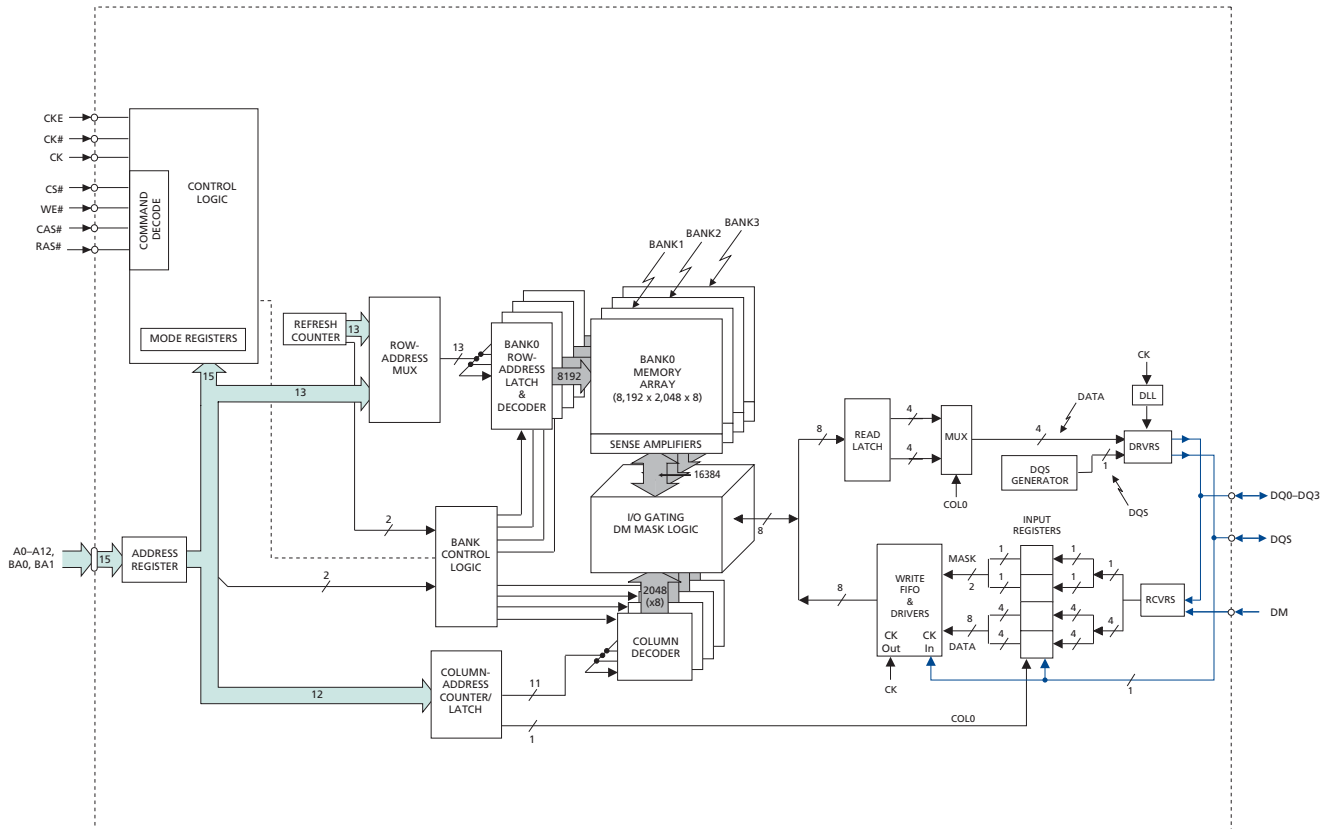
## General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ[7:0]) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]) DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

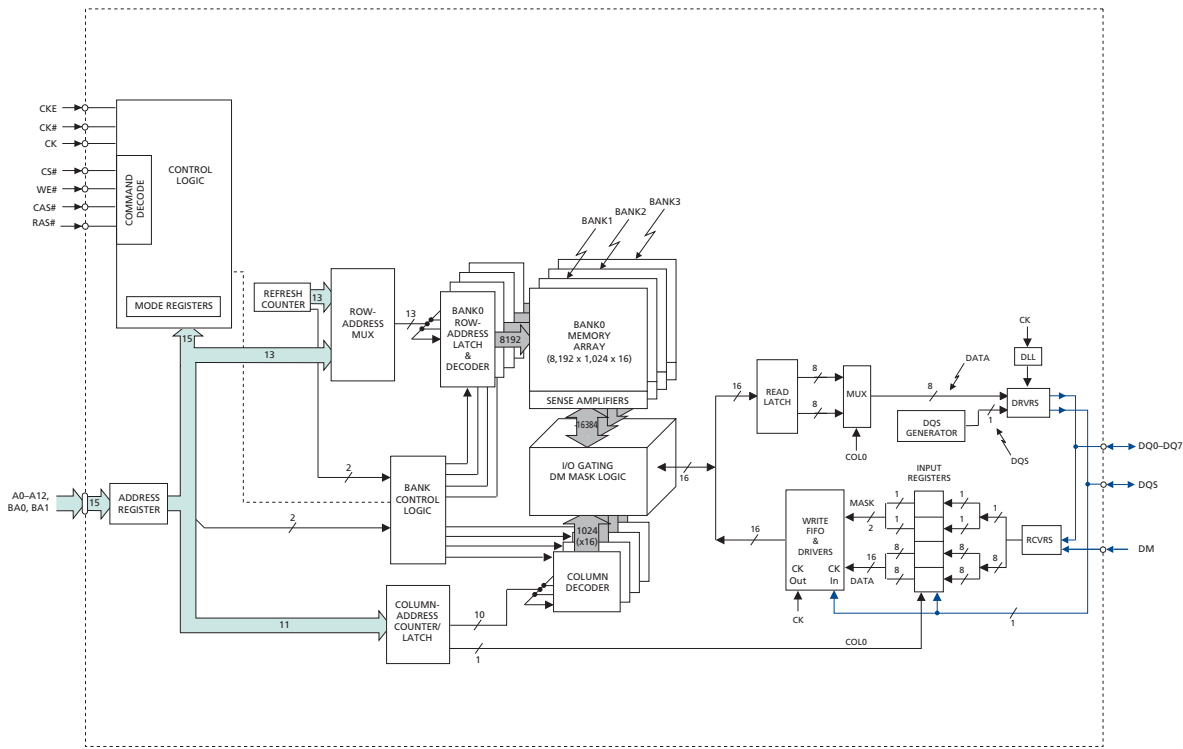
Functional Block Diagrams

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a 4-bank DRAM.

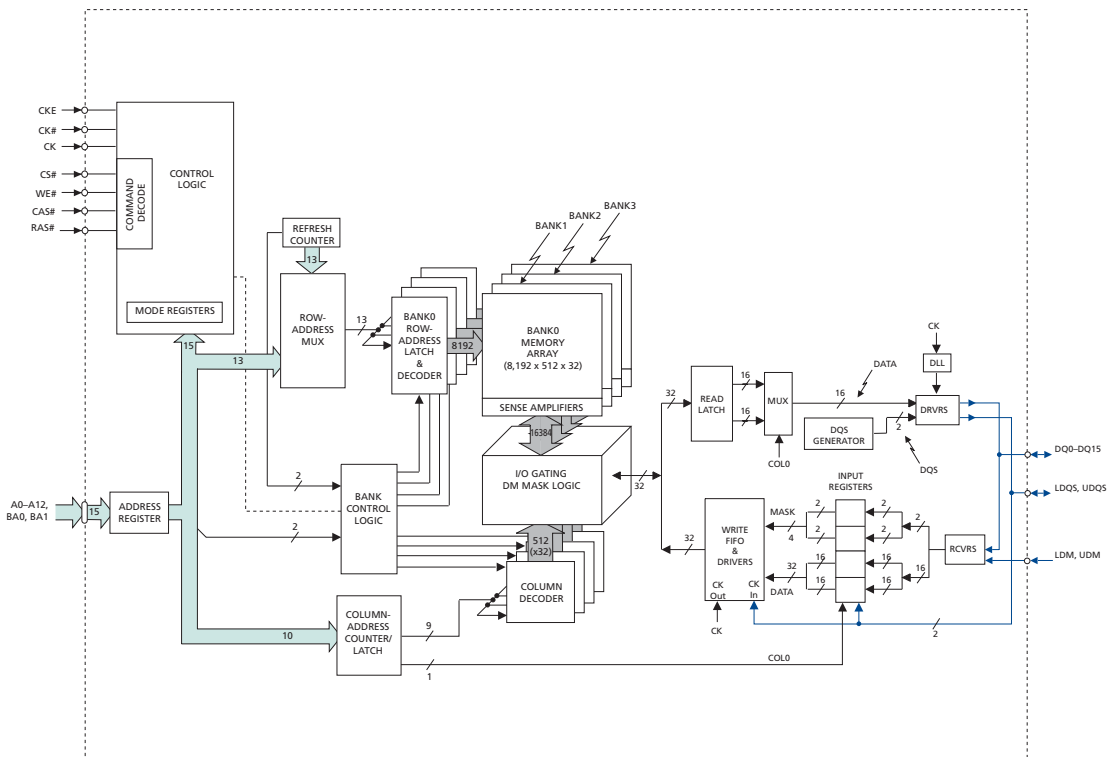
Figure 3: 128 Meg x 4 Functional Block Diagram



**Figure 4: 64 Meg x 8 Functional Block Diagram**



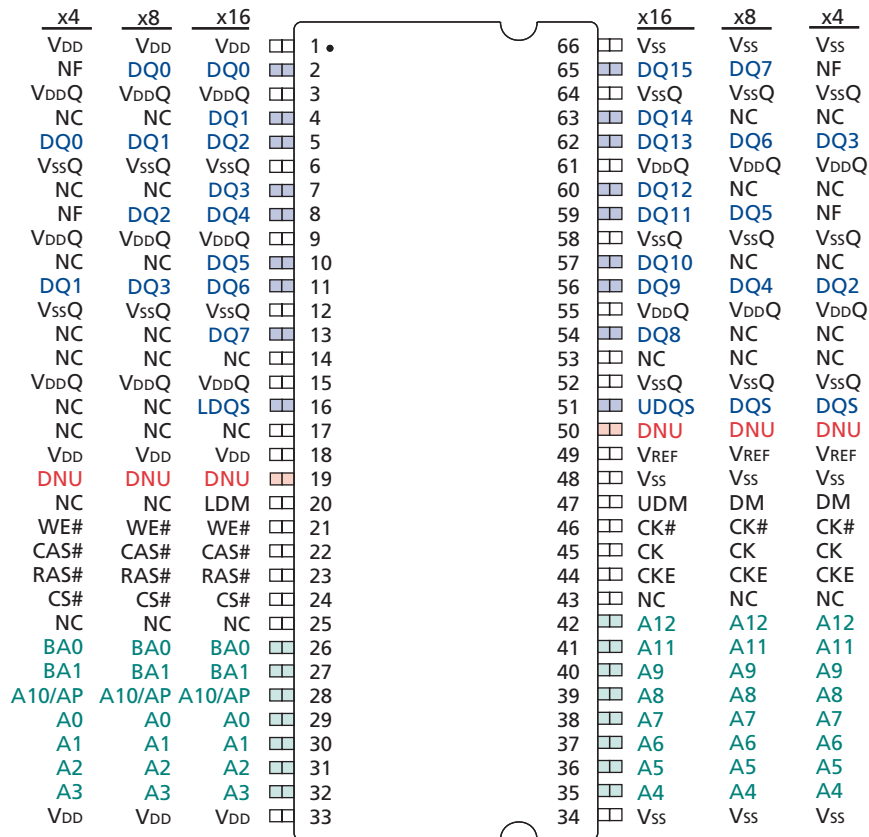
**Figure 5: 32 Meg x 16 Functional Block Diagram**





## Pin and Ball Assignments and Descriptions

**Figure 6: 66-Pin TSOP Pin Assignment (Top View)**



**Figure 7: 60-Ball FBGA Ball Assignment (Top View)**

x4 (Top View)

1	2	3	4	5	6	7	8	9
V <sub>SSQ</sub>	NF	V <sub>SS</sub>	●	A	●	V <sub>DD</sub>	NF	V <sub>DDQ</sub>
NC	V <sub>DDQ</sub>	DQ3	●	B	●	DQ0	V <sub>SSQ</sub>	NC
NC	V <sub>SSQ</sub>	NF	●	C	●	NF	V <sub>DDQ</sub>	NC
NC	V <sub>DDQ</sub>	DQ2	●	D	●	DQ1	V <sub>SSQ</sub>	NC
NC	V <sub>SSQ</sub>	DQ5	●	E	●	NC	V <sub>DDQ</sub>	NC
V <sub>REF</sub>	V <sub>SS</sub>	DM	●	F	●	NC	V <sub>DD</sub>	DNU
	CK	CK#	●	G	●	WE#	CAS#	
	A12	CKE	●	H	●	RAS#	CS#	
	A11	A9	●	J	●	BA1	BA0	
	A8	A7	●	K	●	A0	A10	
	A6	A5	●	L	●	A2	A1	
	A4	V <sub>SS</sub>	●	M	●	V <sub>DD</sub>	A3	

x8 (Top View)

1	2	3	4	5	6	7	8	9
V <sub>SSQ</sub>	DQ7	V <sub>SS</sub>	●	A	●	V <sub>DD</sub>	DQ0	V <sub>DDQ</sub>
NC	V <sub>DDQ</sub>	DQ6	●	B	●	DQ1	V <sub>SSQ</sub>	NC
NC	V <sub>SSQ</sub>	DQ5	●	C	●	DQ2	V <sub>DDQ</sub>	NC
NC	V <sub>DDQ</sub>	DQ4	●	D	●	DQ3	V <sub>SSQ</sub>	NC
NC	V <sub>SSQ</sub>	DQ5	●	E	●	NC	V <sub>DDQ</sub>	NC
V <sub>REF</sub>	V <sub>SS</sub>	DM	●	F	●	NC	V <sub>DD</sub>	DNU
	CK	CK#	●	G	●	WE#	CAS#	
	A12	CKE	●	H	●	RAS#	CS#	
	A11	A9	●	J	●	BA1	BA0	
	A8	A7	●	K	●	A0	A10	
	A6	A5	●	L	●	A2	A1	
	A4	V <sub>SS</sub>	●	M	●	V <sub>DD</sub>	A3	

x16 (Top View)

1	2	3	4	5	6	7	8	9
V <sub>SSQ</sub>	DQ15	V <sub>SS</sub>	●	A	●	V <sub>DD</sub>	DQ0	V <sub>DDQ</sub>
DQ14	V <sub>DDQ</sub>	DQ13	●	B	●	DQ2	V <sub>SSQ</sub>	DQ1
DQ12	V <sub>SSQ</sub>	DQ11	●	C	●	DQ4	V <sub>DDQ</sub>	DQ3
DQ10	V <sub>DDQ</sub>	DQ9	●	D	●	DQ6	V <sub>SSQ</sub>	DQ5
DQ8	V <sub>SSQ</sub>	UDQS	●	E	●	LDQS	V <sub>DDQ</sub>	DQ7
V <sub>REF</sub>	V <sub>SS</sub>	UDM	●	F	●	LDM	V <sub>DD</sub>	DNU
	CK	CK#	●	G	●	WE#	CAS#	
	A12	CKE	●	H	●	RAS#	CS#	
	A11	A9	●	J	●	BA1	BA0	
	A8	A7	●	K	●	A0	A10	
	A6	A5	●	L	●	A2	A1	
	A4	V <sub>SS</sub>	●	M	●	V <sub>DD</sub>	A3	

**Table 4: Pin and Ball Descriptions**

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
K7, L8, L7, M8, M2, L3, L2, K3, K2, J3, K8, J2, H2	29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 28, 41, 42	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
J8, J7	26, 27	BA0, BA1	Input	<b>Bank address inputs:</b> BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER (LMR) command.
G2, G3	45, 46	CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
H3	44	CKE	Input	<b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V <sub>DD</sub> is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only.
H8	24	CS#	Input	<b>Chip select:</b> CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F3, F7, F3	47, 20, 47	DM, LDM, UDM	Input	<b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16, LDM is DM for DQ[7:0] and UDM is DM for DQ[15:8]. Pin 20 is a NC on x4 and x8.
H7, G8, G7	23, 22, 21	RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with CS#) define the command being entered.
A8, B9, B7, C9, C7, D9, D7, E9, E1, D3, D1, C3, C1, B3, B1, A2	2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ[2:0], DQ[5:3], DQ[8:6], DQ[11:9], DQ[14:12], DQ15	I/O	<b>Data input/output:</b> Data bus for x16.
A8, B7, C7, D7, D3, C3, B3, A2	2, 5, 8, 11, 56, 59, 62, 65	DQ[2:0], DQ[5:3], DQ6, DQ7	I/O	<b>Data input/output:</b> Data bus for x8.
B7, D7, D3, B3	5, 11, 56, 62	DQ[2:0], DQ3	I/O	<b>Data input/output:</b> Data bus for x4.

**Table 4: Pin and Ball Descriptions (continued)**

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
E3 E7 E3	51 16 51	DQS LDQS UDQS	I/O	<b>Data strobe:</b> Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For the x16, LDQS is DQS for DQ[7:0] and UDQS is DQS for DQ[15:8]. Pin 16 (E7) is NC on x4 and x8.
F8, M7, A7	1, 18, 33	V <sub>DD</sub>	Supply	<b>Power supply:</b> 2.5V ±0.2V. (2.6V ±0.1V for DDR400).
B2, D2, C8, E8, A9	3, 9, 15, 55, 61	V <sub>DDQ</sub>	Supply	<b>DQ power supply:</b> 2.5V ±0.2V (2.6V ±0.1V for DDR400). Isolated on the die for improved noise immunity.
F1	49	V <sub>REF</sub>	Supply	SSTL_2 reference voltage.
A3, F2, M3	34, 48, 66	V <sub>SS</sub>	Supply	Ground.
A1, C2, E2, B8, D8	6, 12, 52, 58, 64	V <sub>SSQ</sub>	Supply	<b>DQ ground:</b> Isolated on the die for improved noise immunity.
–	14, 17, 25, 43, 53	NC	–	<b>No connect for x16:</b> These pins should be left unconnected.
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7	4, 7, 10, 13, 14, 16, 17, 20, 25, 43, 53, 54, 57, 60, 63	NC	–	<b>No connect for x8:</b> These pins should be left unconnected.
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7	4, 7, 10, 13, 14, 16, 17, 20, 25, 43, 53, 54, 57, 60, 63	NC	–	<b>No connect for x4:</b> These pins should be left unconnected.
A2, A8, C3, C7	2, 8, 59, 65	NF	–	<b>No function for x4:</b> These pins should be left unconnected.
F9	19, 50	DNU	–	<b>Do not use:</b> Must float to minimize noise on V <sub>REF</sub>

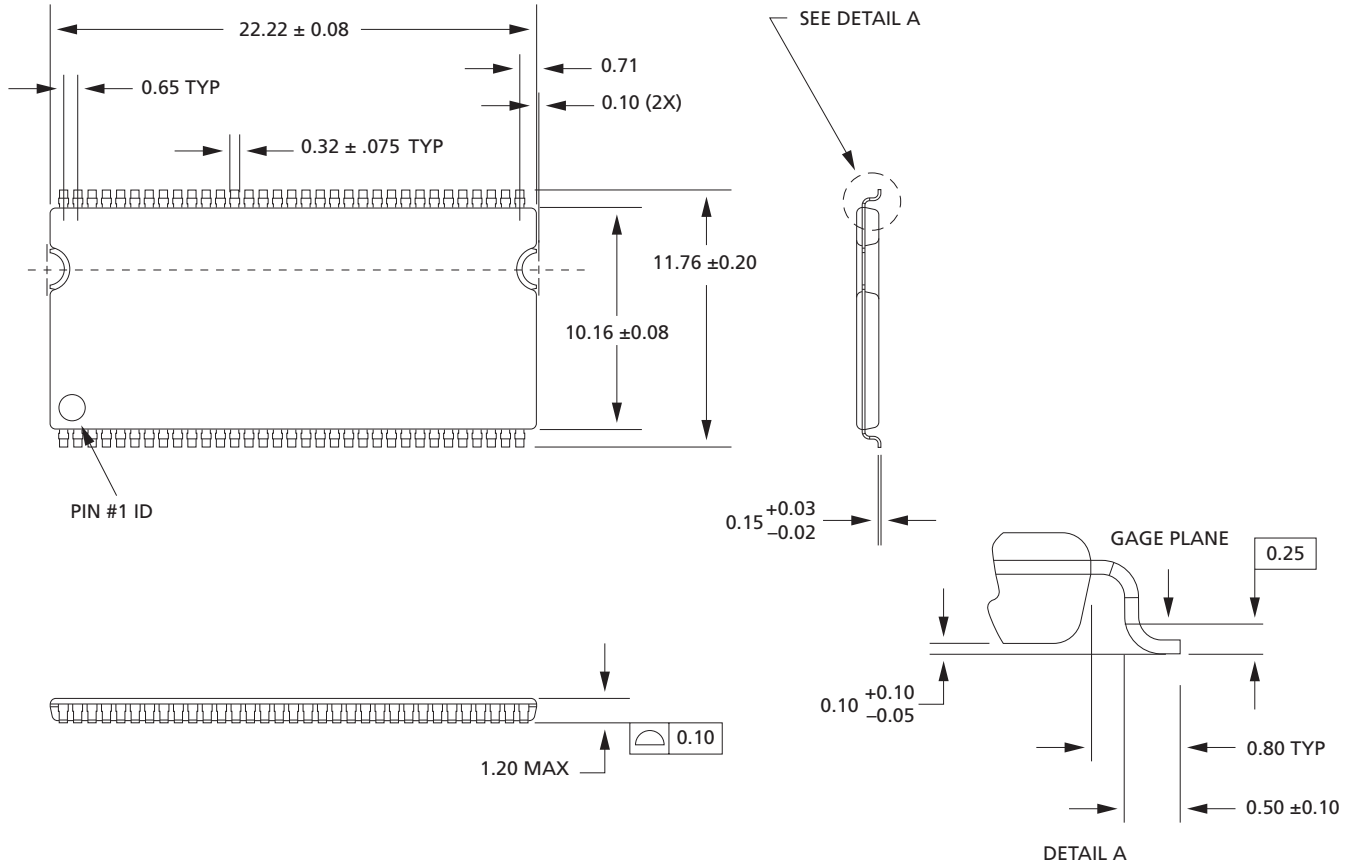
**Table 5: Reserved NC Pin and Ball Descriptions**

NC pins not listed may also be reserved for other uses; this table defines NC pins of importance

TSOP Numbers	Symbol	Type	Description
17	A13	Input	Address input A13 for 1Gb devices.

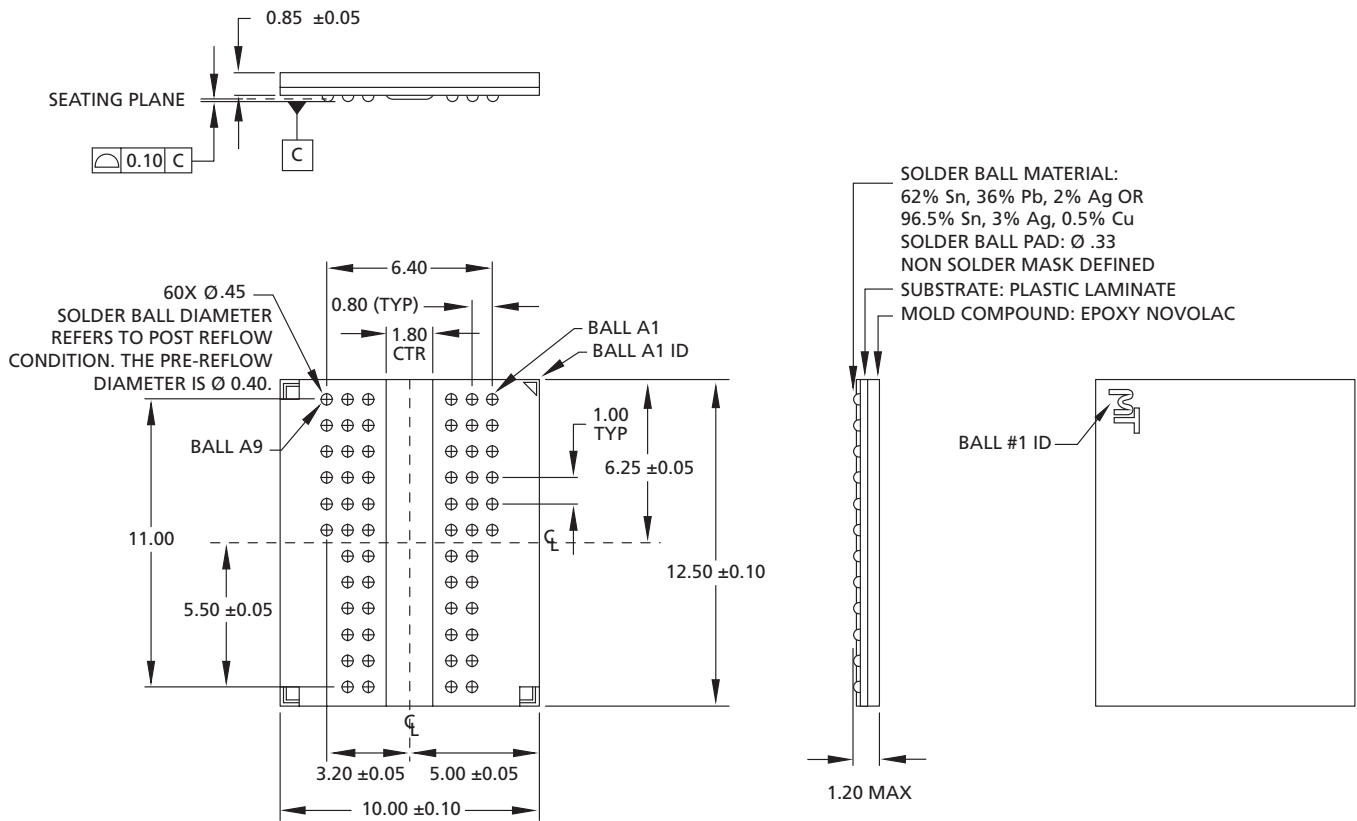
## Package Dimensions

Figure 8: 66-Pin Plastic TSOP (400 mil)



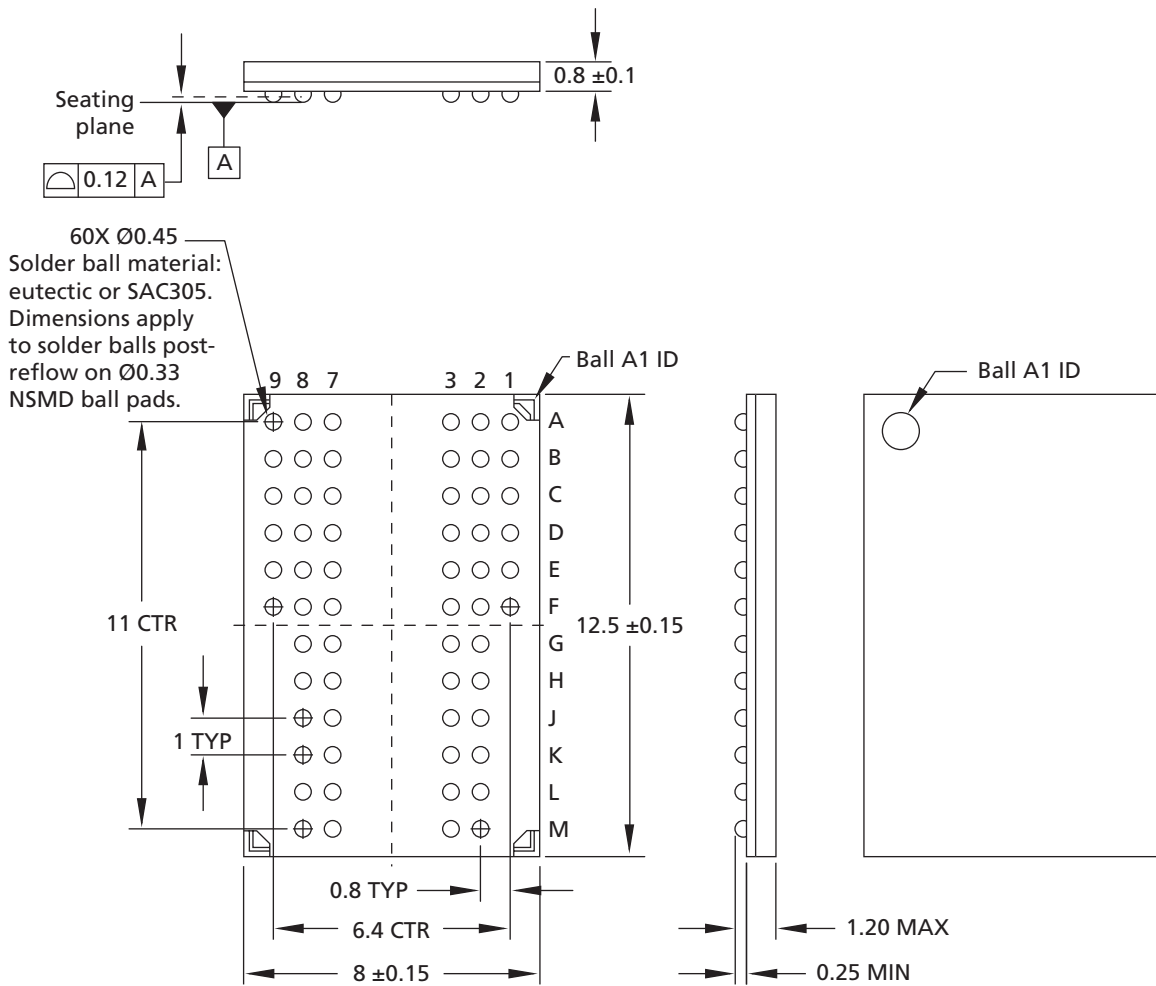
- Notes:
1. All dimensions are in millimeters.
  2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
  3. Not all packages will have the half moon shaped notches as shown.

**Figure 9: 60-Ball FBGA (10mm x 12.5mm)**



- Notes:
1. All dimensions are in millimeters.
  2. Topside part marking decoder can be found on Micron's Web site.

Figure 10: 60-Ball FBGA (8mm x 12.5mm)



- Notes: 1. All dimensions are in millimeters.  
2. Topside part marking decoder can be found on Micron's Web site.

## Electrical Specifications – I<sub>DD</sub>

**Table 6: I<sub>DD</sub> Specifications and Conditions (x4, x8) Die Revision F Only**

V<sub>DDQ</sub> = 2.6V ±0.1V, V<sub>DD</sub> = 2.6V ±0.1V (-5B); V<sub>DDQ</sub> = 2.5V ±0.2V, V<sub>DD</sub> = 2.5V ±0.2V (-6, -6T, -75E, -75Z, -75);  
 0°C ≤ T<sub>A</sub> ≤ 70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

Parameter/Condition	Symbol	-5B	-6/6T	-75E	-75Z/-75	Units	Notes	
<b>Operating one-bank active-precharge current:</b> t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	155	130	130	115	mA	23, 48	
<b>Operating one-bank active-read-precharge current:</b> Burst = 4; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle	I <sub>DD1</sub>	185	160	160	145	mA	23, 48	
<b>Precharge power-down standby current:</b> All banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = (LOW)	I <sub>DD2P</sub>	5	5	5	5	mA	24, 33	
<b>Idle standby current:</b> CS# = HIGH; All banks are idle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS, and DM	I <sub>DD2F</sub>	55	45	45	40	mA	51	
<b>Active power-down standby current:</b> One bank active; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = LOW	I <sub>DD3P</sub>	45	35	35	30	mA	24, 33	
<b>Active standby current:</b> CS# = HIGH; CKE = HIGH; One bank active; t <sub>RC</sub> = t <sub>RAS</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I <sub>DD3N</sub>	60	50	50	45	mA	23	
<b>Operating burst read current:</b> Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA	I <sub>DD4R</sub>	190	165	165	145	mA	23, 48	
<b>Operating burst write current:</b> Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I <sub>DD4W</sub>	195	175	155	135	mA	23	
<b>Auto refresh burst current:</b>	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub>	345	290	290	280	mA	50
	t <sub>RFC</sub> = 7.8μs	I <sub>DD5A</sub>	11	10	10	10	mA	28, 50
	t <sub>RFC</sub> = 1.95μs	I <sub>DD5A</sub>	16	15	15	15	mA	28, 50
<b>Self refresh current:</b> CKE ≤ 0.2V	Standard	I <sub>DD6</sub>	5	5	5	5	mA	12
	Low power (L)	I <sub>DD6A</sub>	3	3	3	3	mA	12
<b>Operating bank interleave read current:</b> Four bank interleaving READs (burst = 4) with auto precharge, t <sub>RC</sub> = minimum t <sub>RC</sub> allowed; t <sub>CK</sub> = t <sub>CK</sub> (MIN); Address and control inputs change only during active READ or WRITE commands	I <sub>DD7</sub>	450	405	400	350	mA	23, 49	



**Table 7: I<sub>DD</sub> Specifications and Conditions (x16) Die Revision F Only**

V<sub>DDQ</sub> = 2.6V ±0.1V, V<sub>DD</sub> = 2.6V ±0.1V (-5B); V<sub>DDQ</sub> = 2.5V ±0.2V, V<sub>DD</sub> = 2.5V ±0.2V (-6, -6T, -75E, -75Z, -75);  
 0°C ≤ T<sub>A</sub> ≤ 70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

Parameter/Condition	Symbol	-5B	-6/6T	-75E	-75Z/-75	Units	Notes	
<b>Operating one-bank active-precharge current:</b> t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	155	130	130	115	mA	23, 48	
<b>Operating one-bank active-read-precharge current:</b> Burst = 4; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle	I <sub>DD1</sub>	195	160	160	145	mA	23, 48	
<b>Precharge power-down standby current:</b> All banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = (LOW)	I <sub>DD2P</sub>	5	5	5	5	mA	24, 33	
<b>Idle standby current:</b> CS# = HIGH; All banks are idle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS, and DM	I <sub>DD2F</sub>	55	45	45	40	mA	51	
<b>Active power-down standby current:</b> One bank active; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = LOW	I <sub>DD3P</sub>	45	35	35	30	mA	24, 33	
<b>Active standby current:</b> CS# = HIGH; CKE = HIGH; One bank active; t <sub>RC</sub> = t <sub>RAS</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I <sub>DD3N</sub>	60	50	50	45	mA	23	
<b>Operating burst read current:</b> Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA	I <sub>DD4R</sub>	210	165	165	145	mA	23, 48	
<b>Operating burst write current:</b> Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I <sub>DD4W</sub>	215	195	160	135	mA	23	
<b>Auto refresh burst current:</b>	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub>	345	290	290	280	mA	50
	t <sub>RFC</sub> = 7.8μs	I <sub>DD5A</sub>	11	10	10	10	mA	28, 50
	t <sub>RFC</sub> = 1.95μs	I <sub>DD5A</sub>	16	15	15	15	mA	28, 50
<b>Self refresh current:</b> CKE ≤ 0.2V	Standard	I <sub>DD6</sub>	6	5	5	5	mA	12
	Low power (L)	I <sub>DD6A</sub>	4	3	3	3	mA	12
<b>Operating bank interleave read current:</b> Four bank interleaving READs (burst = 4) with auto precharge, t <sub>RC</sub> = minimum t <sub>RC</sub> allowed; t <sub>CK</sub> = t <sub>CK</sub> (MIN); Address and control inputs change only during active READ or WRITE commands	I <sub>DD7</sub>	480	405	400	350	mA	23, 49	

**Table 8: I<sub>DD</sub> Specifications and Conditions (x4, x8) Die Revision J Only**

V<sub>DDQ</sub> = 2.6V ±0.1V, V<sub>DD</sub> = 2.6V ±0.1V (-5B); V<sub>DDQ</sub> = 2.5V ±0.2V, V<sub>DD</sub> = 2.5V ±0.2V (-6, -6T);  
 0°C ≤ T<sub>A</sub> ≤ 70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

Parameter/Condition	Symbol	-5B	-6/6T	Units	Notes	
<b>Operating one-bank active-precharge current:</b> t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	75	65	mA	23, 48	
<b>Operating one-bank active-read-precharge current:</b> Burst = 4; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle	I <sub>DD1</sub>	85	75	mA	23, 48	
<b>Precharge power-down standby current:</b> All banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = (LOW)	I <sub>DD2P</sub>	5	5	mA	24, 33	
<b>Idle standby current:</b> CS# = HIGH; All banks are idle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS, and DM	I <sub>DD2F</sub>	23	23	mA	51	
<b>Active power-down standby current:</b> One bank active; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = LOW	I <sub>DD3P</sub>	18	14	mA	24, 33	
<b>Active standby current:</b> CS# = HIGH; CKE = HIGH; One bank active; t <sub>RC</sub> = t <sub>RAS</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I <sub>DD3N</sub>	40	38	mA	23	
<b>Operating burst read current:</b> Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA	I <sub>DD4R</sub>	120	85	mA	23, 48	
<b>Operating burst write current:</b> Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I <sub>DD4W</sub>	120	95	mA	23	
<b>Auto refresh burst current:</b>	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub>	120	105	mA	50
	t <sub>RFC</sub> = 7.8μs	I <sub>DD5A</sub>	8	8	mA	28, 50
<b>Self refresh current:</b> CKE ≤ 0.2V	Standard	I <sub>DD6</sub>	5	5	mA	12
	Low power (L)	I <sub>DD6A</sub>	3	3	mA	12
<b>Operating bank interleave read current:</b> Four bank interleaving READs (burst = 4) with auto precharge, t <sub>RC</sub> = minimum t <sub>RC</sub> allowed; t <sub>CK</sub> = t <sub>CK</sub> (MIN); Address and control inputs change only during active READ or WRITE commands	I <sub>DD7</sub>	230	210	mA	23, 49	

**Table 9: I<sub>DD</sub> Specifications and Conditions (x16) Die Revision J Only**
 $V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$  (-5B);  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$  (-6, -6T);

 $0^{\circ}C \leq T_A \leq 70^{\circ}C$ ; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

Parameter/Condition	Symbol	-5B	-6/6T	Units	Notes	
<b>Operating one-bank active-precharge current:</b> $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	$I_{DD0}$	75	65	mA	23, 48	
<b>Operating one-bank active-read-precharge current:</b> Burst = 4; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$ ; Address and control inputs changing once per clock cycle	$I_{DD1}$	85	75	mA	23, 48	
<b>Precharge power-down standby current:</b> All banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = (LOW)	$I_{DD2P}$	5	5	mA	24, 33	
<b>Idle standby current:</b> CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS, and DM	$I_{DD2F}$	23	23	mA	51	
<b>Active power-down standby current:</b> One bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = LOW	$I_{DD3P}$	18	14	mA	24, 33	
<b>Active standby current:</b> CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	$I_{DD3N}$	40	38	mA	23	
<b>Operating burst read current:</b> Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$	$I_{DD4R}$	125	95	mA	23, 48	
<b>Operating burst write current:</b> Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle	$I_{DD4W}$	120	95	mA	23	
<b>Auto refresh burst current:</b>	$t_{RFC} = t_{RFC}(\text{MIN})$	$I_{DD5}$	125	110	mA	50
	$t_{RFC} = 7.8\mu\text{s}$	$I_{DD5A}$	8	8	mA	28, 50
<b>Self refresh current:</b> CKE $\leq 0.2V$	Standard	$I_{DD6}$	5	5	mA	12
	Low power (L)	$I_{DD6A}$	3	3	mA	12
<b>Operating bank interleave read current:</b> Four bank interleaving READs (burst = 4) with auto precharge, $t_{RC} = \text{minimum } t_{RC} \text{ allowed}$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs change only during active READ or WRITE commands	$I_{DD7}$	230	210	mA	23, 49	

**Table 10: I<sub>DD</sub> Test Cycle Times**

Values reflect number of clock cycles for each test

I <sub>DD</sub> Test	Speed Grade	Clock Cycle Time	t <sub>RRD</sub>	t <sub>RCD</sub>	t <sub>RAS</sub>	t <sub>RP</sub>	t <sub>RC</sub>	t <sub>RFC</sub>	t <sub>REFI</sub>	CL
I <sub>DD0</sub>	-75/75Z	7.5ns	n/a	n/a	6	3	9	n/a	n/a	n/a
	-75E	7.5ns	n/a	n/a	6	2	8	n/a	n/a	n/a
	-6/-6T	6ns	n/a	n/a	7	3	10	n/a	n/a	n/a
	-5B	5ns	n/a	n/a	8	3	11	n/a	n/a	n/a
I <sub>DD1</sub>	-75	7.5ns	n/a	n/a	6	3	9	n/a	n/a	2.5
	-75Z	7.5ns	n/a	n/a	6	3	9	n/a	n/a	2
	-75E	7.5ns	n/a	n/a	6	2	8	n/a	n/a	2
	-6/-6T	6ns	n/a	n/a	7	3	10	n/a	n/a	2.5
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	3
I <sub>DD4R</sub>	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2.5
	-75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2.5
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	3
I <sub>DD4W</sub>	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
I <sub>DD5</sub>	-75/75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	10	10	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	9	9	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	12	12	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	14	14	n/a
I <sub>DD5A</sub>	-75/75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	10	1,029	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	10	1,029	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	12	1,288	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	14	1,546	n/a
I <sub>DD7</sub>	-75	7.5ns	2	3	n/a	3	10	n/a	n/a	2.5
	-75Z	7.5ns	2	3	n/a	3	10	n/a	n/a	2
	-75E	7.5ns	2	3	n/a	2	8	n/a	n/a	2
	-6/-6T	6ns	2	3	n/a	3	10	n/a	n/a	2.5
	-5B	5ns	2	3	n/a	3	11	n/a	n/a	3

## Electrical Specifications – DC and AC

Stresses greater than those listed in Table 11 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 11: Absolute Maximum Ratings**

Parameter	Min	Max	Units
$V_{DD}$ supply voltage relative to $V_{SS}$	-1V	3.6V	V
$V_{DDQ}$ supply voltage relative to $V_{SS}$	-1V	3.6V	V
$V_{REF}$ and inputs voltage relative to $V_{SS}$	-1V	3.6V	V
I/O pins voltage relative to $V_{SS}$	-0.5V	$V_{DDQ} + 0.5V$	V
Storage temperature (plastic)	-55	150	°C
Short circuit output current	-	50	mA

**Table 12: DC Electrical Characteristics and Operating Conditions (-5B)**

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 37;  $V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$

Parameter/Condition	Symbol	Min	Max	Units	Notes	
Supply voltage	$V_{DD}$	2.5	2.7	V	37, 42	
I/O supply voltage	$V_{DDQ}$	2.5	2.7	V	37, 42, 45	
I/O reference voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	7, 45	
I/O termination voltage (system)	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	8, 45	
Input high (logic 1) voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$	$V_{DD} + 0.3$	V	29	
Input low (logic 0) voltage	$V_{IL(DC)}$	-0.3	$V_{REF} - 0.15$	V	29	
Input leakage current: Any input $0V \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ pin $0V \leq V_{IN} \leq 1.35V$ (All other pins not under test = 0V)	$I_I$	-2	2	$\mu A$		
Output leakage current: (DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )	$I_{OZ}$	-5	5	$\mu A$		
Full-drive option output levels (x4, x8, x16):	High current ( $V_{OUT} = V_{DDQ} - 0.373V$ , minimum $V_{REF}$ minimum $V_{TT}$ )	$I_{OH}$	-16.8	-	mA	38, 40
	Low current ( $V_{OUT} = 0.373V$ , maximum $V_{REF}$ maximum $V_{TT}$ )	$I_{OL}$	16.8	-	mA	
Reduced-drive option output levels:	High current ( $V_{OUT} = V_{DDQ} - 0.373V$ , minimum $V_{REF}$ minimum $V_{TT}$ )	$I_{OHR}$	-9	-	mA	39, 40
	Low current ( $V_{OUT} = 0.373V$ , maximum $V_{REF}$ maximum $V_{TT}$ )	$I_{OLR}$	9	-	mA	
Ambient operating temperatures	Commercial	$T_A$	0	70	°C	
	Industrial	$T_A$	-40	85	°C	

**Table 13: DC Electrical Characteristics and Operating Conditions (-6, -6T, -75E, -75Z, -75)**

 Notes: 1–5 and 17 apply to the entire table; Notes appear on page 37;  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$ 

Parameter/Condition	Symbol	Min	Max	Units	Notes	
Supply voltage	$V_{DD}$	2.3	2.7	V	37, 42	
I/O supply voltage	$V_{DDQ}$	2.3	2.7	V	37, 42, 45	
I/O reference voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	7, 45	
I/O termination voltage (system)	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	8, 45	
Input high (logic 1) voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$	$V_{DD} + 0.3$	V	29	
Input low (logic 0) voltage	$V_{IL(DC)}$	-0.3	$V_{REF} - 0.15$	V	29	
Input leakage current: Any input $0V \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ pin $0V \leq V_{IN} \leq 1.35V$ (All other pins not under test = 0V)	$I_I$	-2	2	$\mu A$		
Output leakage current: (DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )	$I_{OZ}$	-5	5	$\mu A$		
Full-drive option output levels (x4, x8, x16):	High current ( $V_{OUT} = V_{DDQ} - 0.373V$ , minimum $V_{REF}$ minimum $V_{TT}$ )	$I_{OH}$	-16.8	-	mA	38, 40
	Low current ( $V_{OUT} = 0.373V$ , maximum $V_{REF}$ maximum $V_{TT}$ )	$I_{OL}$	16.8	-	mA	
Reduced-drive option output levels:	High current ( $V_{OUT} = V_{DDQ} - 0.373V$ , minimum $V_{REF}$ minimum $V_{TT}$ )	$I_{OHR}$	-9	-	mA	39, 40
	Low current ( $V_{OUT} = 0.373V$ , maximum $V_{REF}$ maximum $V_{TT}$ )	$I_{OLR}$	9	-	mA	
Ambient operating temperatures	Commercial	$T_A$	0	70	$^{\circ}C$	
	Industrial	$T_A$	-40	85	$^{\circ}C$	

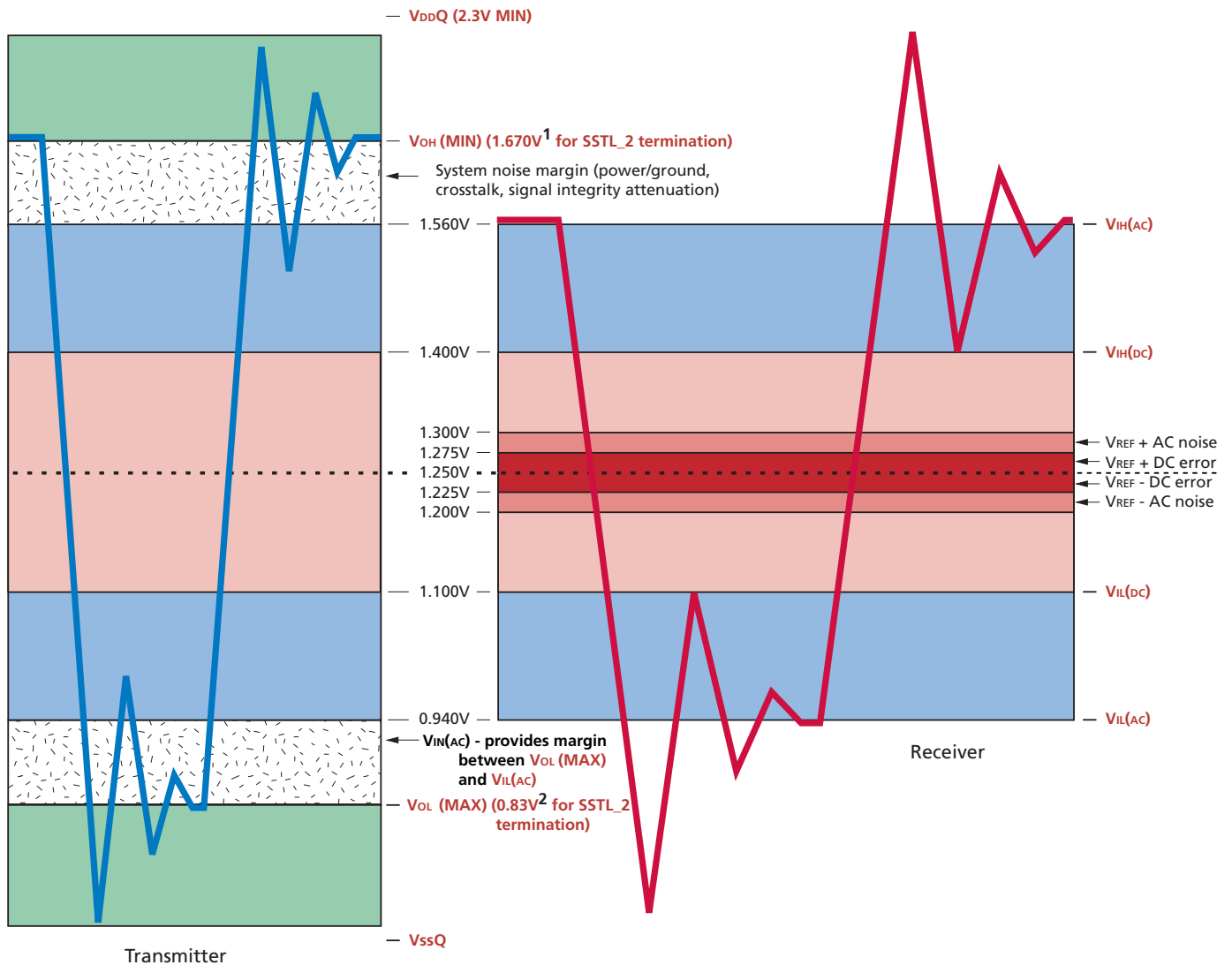
**Table 14: AC Input Operating Conditions**

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 37;

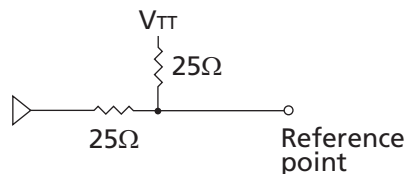
 $0^{\circ}C \leq T_A \leq 70^{\circ}C$ ;  $V_{DDQ} = 2.5V \pm 0.2V$ ,  $V_{DD} = 2.5V \pm 0.2V$  ( $V_{DDQ} = 2.6V \pm 0.1V$ ,  $V_{DD} = 2.6V \pm 0.1V$  for -5B)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage	$V_{IH(AC)}$	$V_{REF} + 0.310$	-	V	15, 29, 41
Input low (logic 0) voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.310$	V	15, 29, 41
I/O reference voltage	$V_{REF(AC)}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	7

Figure 11: Input Voltage Waveform



- Notes:
1.  $V_{OH,min}$  with test load is 1.927V.
  2.  $V_{OL,max}$  with test load is 0.373V.
  3. Numbers in diagram reflect nominal values utilizing circuit below for all devices other than -5B.

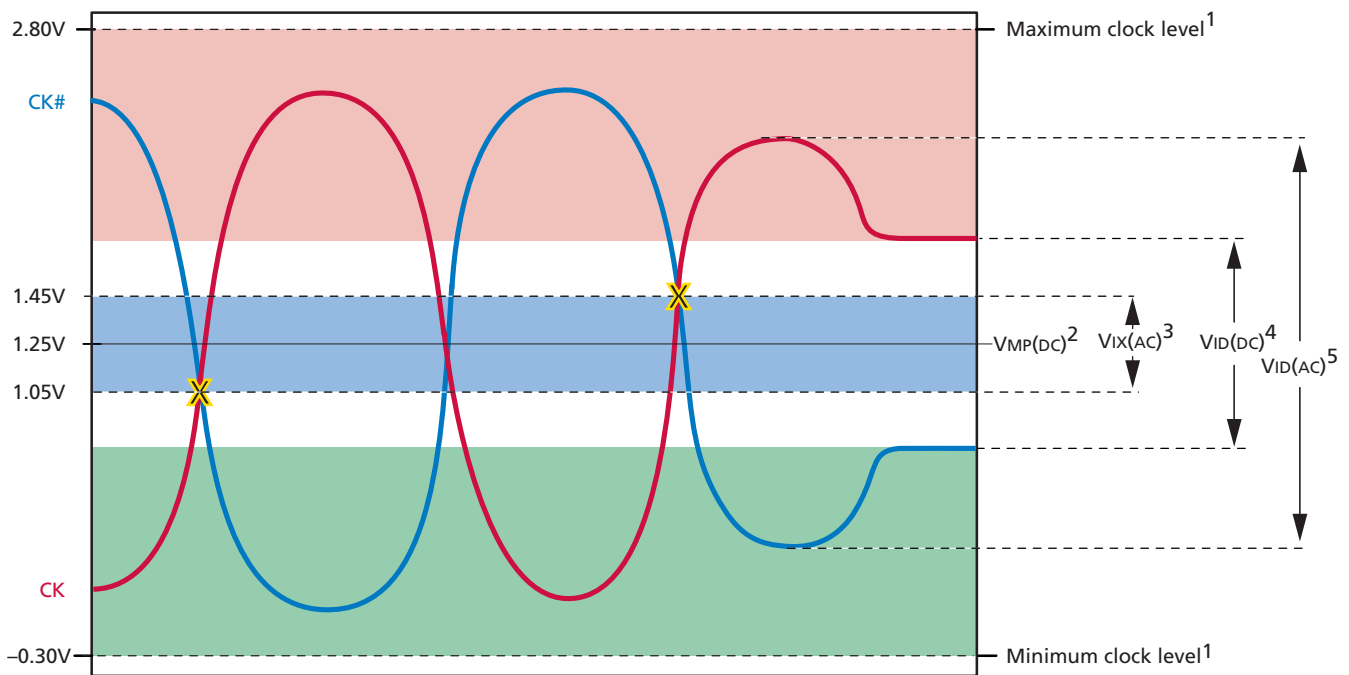


**Table 15: Clock Input Operating Conditions**

Notes: 1–5, 16, 17, and 31 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$  ( $V_{DDQ} = 2.6\text{V} \pm 0.1\text{V}$ ,  $V_{DD} = 2.6\text{V} \pm 0.1\text{V}$  for -5B)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input mid-point voltage: CK and CK#	$V_{MP(DC)}$	1.15	1.35	V	7, 10
Clock input voltage level: CK and CK#	$V_{IN(DC)}$	-0.3	$V_{DDQ} + 0.3$	V	7
Clock input differential voltage: CK and CK#	$V_{ID(DC)}$	0.36	$V_{DDQ} + 0.6$	V	7, 9
Clock input differential voltage: CK and CK#	$V_{ID(AC)}$	0.7	$V_{DDQ} + 0.6$	V	9
Clock input crossing point voltage: CK and CK#	$V_{IX(AC)}$	$0.5 \times V_{DDQ} - 0.2$	$0.5 \times V_{DDQ} + 0.2$	V	10

**Figure 12: SSTL\_2 Clock Input**



- Notes:
1. CK or CK# may not be more positive than  $V_{DDQ} + 0.3\text{V}$  or more negative than  $V_{SS} - 0.3\text{V}$ .
  2. This provides a minimum of 1.15V to a maximum of 1.35V and is always half of  $V_{DDQ}$ .
  3. CK and CK# must cross in this region.
  4. CK and CK# must meet at least  $V_{ID(DC),min}$  when static and is centered around  $V_{MP(DC)}$ .
  5. CK and CK# must have a minimum 700mV peak-to-peak swing.
  6. For AC operation, all DC clock requirements must also be satisfied.
  7. Numbers in diagram reflect nominal values for all devices other than -5B.



**Table 16: Capacitance (x4, x8 TSOP)**

Note: 14 applies to the entire table; Notes appear on page 37

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ[3:0] (x4), DQ[7:0] (x8)	DC <sub>IO</sub>	–	0.50	pF	25
Delta input capacitance: Command and address	DC <sub>I1</sub>	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC <sub>I2</sub>	–	0.25	pF	30
Input/output capacitance: DQ, DQS, DM	C <sub>IO</sub>	4.0	5.0	pF	
Input capacitance: Command and address	C <sub>I1</sub>	2.0	3.0	pF	
Input capacitance: CK, CK#	C <sub>I2</sub>	2.0	3.0	pF	
Input capacitance: CKE	C <sub>I3</sub>	2.0	3.0	pF	

**Table 17: Capacitance (x4, x8 FBGA)**

Note: 14 applies to the entire table; Notes appear on page 37

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ, DQS, DM	DC <sub>IO</sub>	–	0.50	pF	25
Delta input capacitance: Command and address	DC <sub>I1</sub>	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC <sub>I2</sub>	–	0.25	pF	30
Input/output capacitance: DQ, DQS, DM	C <sub>IO</sub>	3.5	4.5	pF	
Input capacitance: Command and address	C <sub>I1</sub>	1.5	2.5	pF	
Input capacitance: CK, CK#	C <sub>I2</sub>	1.5	2.5	pF	
Input capacitance: CKE	C <sub>I3</sub>	1.5	2.5	pF	

**Table 18: Capacitance (x16 TSOP)**

Note: 14 applies to the entire table; Notes appear on page 37

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ[7:0], LDQS, LDM	DC <sub>IO<sub>L</sub></sub>	–	0.50	pF	25
Delta input/output capacitance: DQ[15:8], UDQS, UDM	DC <sub>IO<sub>U</sub></sub>	–	0.50	pF	25
Delta input capacitance: Command and address	DC <sub>I1</sub>	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC <sub>I2</sub>	–	0.25	pF	30
Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM	C <sub>IO</sub>	4.0	5.0	pF	
Input capacitance: Command and address	C <sub>I1</sub>	2.0	3.0	pF	
Input capacitance: CK, CK#	C <sub>I2</sub>	2.0	3.0	pF	
Input capacitance: CKE	C <sub>I3</sub>	2.0	3.0	pF	

**Table 19: Capacitance (x16 FBGA)**

Note: 14 applies to the entire table; Notes appear on page 37

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ[7:0], LDQS, LDM	DC <sub>IO<sub>L</sub></sub>	–	0.50	pF	25
Delta input/output capacitance: DQ[15:8], UDQS, UDM	DC <sub>IO<sub>U</sub></sub>	–	0.50	pF	25
Delta input capacitance: Command and address	DC <sub>I1</sub>	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC <sub>I2</sub>	–	0.25	pF	30
Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM	C <sub>IO</sub>	3.5	4.5	pF	
Input capacitance: Command and address	C <sub>I1</sub>	1.5	2.5	pF	
Input capacitance: CK, CK#	C <sub>I2</sub>	1.5	2.5	pF	
Input capacitance: CKE	C <sub>I3</sub>	1.5	2.5	pF	

**Table 20: Electrical Characteristics and Recommended AC Operating Conditions (-5B)**

Notes 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 37;  
 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{\text{DDQ}} = 2.6\text{V} \pm 0.1\text{V}$ ,  $V_{\text{DD}} = 2.6\text{V} \pm 0.1\text{V}$

AC Characteristics		-5B		Units	Notes	
Parameter	Symbol	Min	Max			
Access window of DQ from CK/CK#	$t^{\text{AC}}$	-0.70	0.70	ns		
CK high-level width	$t^{\text{CH}}$	0.45	0.55	$t^{\text{CK}}$	31	
Clock cycle time	CL = 3	$t^{\text{CK}}(3)$	5	7.5	ns	52
	CL = 2.5	$t^{\text{CK}}(2.5)$	6	13	ns	46, 52
	CL = 2	$t^{\text{CK}}(2)$	7.5	13	ns	46, 52
CK low-level width	$t^{\text{CL}}$	0.45	0.55	$t^{\text{CK}}$	31	
DQ and DM input hold time relative to DQS	$t^{\text{DH}}$	0.40	–	ns	27, 32	
DQ and DM input pulse width (for each input)	$t^{\text{DIPW}}$	1.75	–	ns	32	
Access window of DQS from CK/CK#	$t^{\text{DQSCK}}$	-0.60	0.60	ns		
DQS input high pulse width	$t^{\text{DQSH}}$	0.35	–	$t^{\text{CK}}$		
DQS input low pulse width	$t^{\text{DQSL}}$	0.35	–	$t^{\text{CK}}$		
DQS–DQ skew, DQS to last DQ valid, per group, per access	$t^{\text{DQSQ}}$	–	0.40	ns	26, 27	
WRITE command to first DQS latching transition	$t^{\text{DQSS}}$	0.72	1.28	$t^{\text{CK}}$		
DQ and DM input setup time relative to DQS	$t^{\text{DS}}$	0.40	–	ns	27, 32	
DQS falling edge from CK rising – hold time	$t^{\text{DSH}}$	0.2	–	$t^{\text{CK}}$		
DQS falling edge to CK rising – setup time	$t^{\text{DSS}}$	0.2	–	$t^{\text{CK}}$		
Half-clock period	$t^{\text{HP}}$	$t^{\text{CH}}, t^{\text{CL}}$	–	ns	35	
Data-out High-Z window from CK/CK#	$t^{\text{HZ}}$	–	0.70	ns	19, 43	
Address and control input hold time (slew rate $\geq 0.5$ V/ns)	$t^{\text{IH}}_{\text{F}}$	0.60	–	ns	15	
Address and control input pulse width (for each input)	$t^{\text{IPW}}$	2.2	–	ns		
Address and control input setup time (slew rate $\geq 0.5$ V/ns)	$t^{\text{IS}}_{\text{F}}$	0.60	–	ns	15	
Data-out Low-Z window from CK/CK#	$t^{\text{LZ}}$	-0.70	–	ns	19, 43	
LOAD MODE REGISTER command cycle time	$t^{\text{MRD}}$	10	–	ns		
DQ–DQS hold, DQS to first DQ to go non-valid, per access	$t^{\text{QH}}$	$t^{\text{HP}} - t^{\text{QHS}}$	–	ns	26, 27	
Data hold skew factor	$t^{\text{QHS}}$	–	0.50	ns		
ACTIVE-to-READ with auto precharge command	$t^{\text{RAP}}$	15	–	ns		
ACTIVE-to-PRECHARGE command	$t^{\text{RAS}}$	40	70,000	ns	36	
ACTIVE-to-ACTIVE/AUTO REFRESH command period	$t^{\text{RC}}$	55	–	ns	55	
ACTIVE-to-READ or WRITE delay	$t^{\text{RCD}}$	15	–	ns		
REFRESH-to-REFRESH command interval	$t^{\text{REFC}}$	–	70.3	$\mu\text{s}$	24	
Average periodic refresh interval	$t^{\text{REFI}}$	–	7.8	$\mu\text{s}$	24	
AUTO REFRESH command period	$t^{\text{RFC}}$	70	–	ns	50	
PRECHARGE command period	$t^{\text{RP}}$	15	–	ns		
DQS read preamble	$t^{\text{RPRE}}$	0.9	1.1	$t^{\text{CK}}$	44	
DQS read postamble	$t^{\text{RPST}}$	0.4	0.6	$t^{\text{CK}}$	44	
ACTIVE bank a to ACTIVE bank b command	$t^{\text{RRD}}$	10	–	ns		
Terminating voltage delay to $V_{\text{DD}}$	$t^{\text{VTD}}$	0	–	ns		
DQS write preamble	$t^{\text{WPRE}}$	0.25	–	$t^{\text{CK}}$		
DQS write preamble setup time	$t^{\text{WPRES}}$	0	–	ns	21, 22	
DQS write postamble	$t^{\text{WPST}}$	0.4	0.6	$t^{\text{CK}}$	20	
Write recovery time	$t^{\text{WR}}$	15	–	ns		
Internal WRITE-to-READ command delay	$t^{\text{WTR}}$	2	–	$t^{\text{CK}}$		