



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Double Data Rate (DDR) SDRAM

MT46V128M4 – 32 Meg x 4 x 4 banks

MT46V64M8 – 16 Meg x 8 x 4 banks

MT46V32M16 – 8 Meg x 16 x 4 banks

Features

- VDD = +2.5V ±0.2V, VDDQ = +2.5V ±0.2V
VDD = +2.6V ±0.1V, VDDQ = +2.6V ±0.1V (DDR400)¹
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto refresh
– 64ms, 8192-cycle
- Longer-lead TSOP for improved reliability (OCPL)
- 2.5VI/O (SSTL_2 compatible)
- Concurrent auto precharge option is supported
- ^tRAS lockout supported (^tRAP = ^tRCD)

Options

- Configuration
 - 128 Meg x 4 (32 Meg x 4 x 4 banks)
 - 64 Meg x 8 (16 Meg x 8 x 4 banks)
 - 32 Meg x 16 (8 Meg x 16 x 4 banks)
- Plastic package
 - 66-pin TSOP
 - 66-pin TSOP (Pb-free)
 - 60-ball FBGA (10mm x 12.5mm)
 - 60-ball FBGA (10mm x 12.5mm) (Pb-free)
 - 60-ball FBGA (8mm x 12.5mm)
 - 60-ball FBGA (8mm x 12.5mm) (Pb-free)
- Timing – cycle time
 - 5ns @ CL = 3 (DDR400)
 - 6ns @ CL = 2.5 (DDR333) (FBGA only)
 - 6ns @ CL = 2.5 (DDR333) (TSOP only)
- Self refresh
 - Standard
 - Low-power self refresh
- Temperature rating
 - Commercial (0°C to +70°C)
 - Industrial (–40°C to +85°C)
- Revision
 - x4, x8, x16
 - x4, x8, x16

Marking

128M4
64M8
32M16

TG
P
FN²
BN²
CV³
CY³

-5B
-6²
-6T²

None
L

None
IT

:F
:J

- Notes: 1. DDR400 devices operating at ≤ DDR333 conditions can use VDD/VDDQ = +2.5V ±0.2V.
2. Available only on Revision F.
3. Available only on Revision J.

Table 1: Key Timing Parameters

CL = CAS (READ) latency; data-out window is MIN clock rate with 50% duty cycle at CL = 2, CL = 2.5, or CL = 3

Speed Grade	Clock Rate (MHz)			Data-Out Window	Access Window	DQS–DQ Skew
	CL = 2	CL = 2.5	CL = 3			
-5B	133	167	200	1.6ns	±0.70ns	+0.40ns
-6	133	167	n/a	2.1ns	±0.70ns	+0.40ns
6T	133	167	n/a	2.0ns	±0.70ns	+0.45ns
-75E/-75Z	133	133	n/a	2.5ns	±0.75ns	+0.50ns
-75	100	133	n/a	2.5ns	±0.75ns	+0.50ns

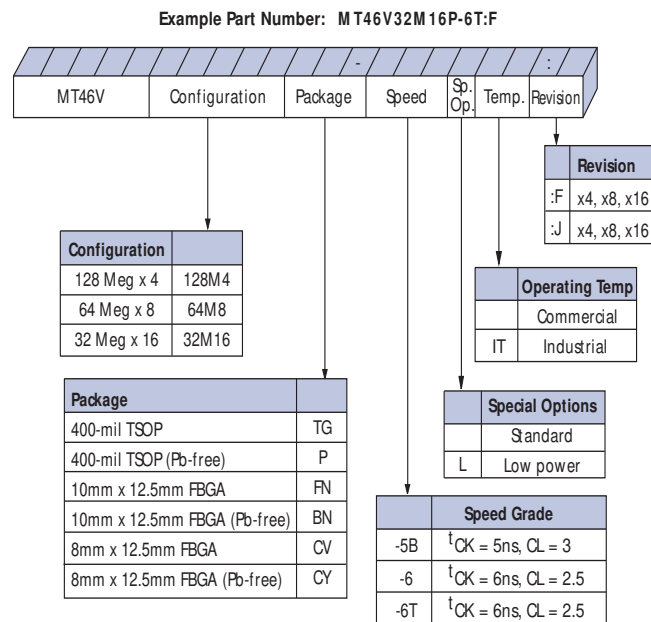
Table 2: Addressing

Parameter	128 Meg x 4	64 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank address	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column address	4K (A0–A9, A11, A12)	2K (A0–A9, A11)	1K (A0–A9)

Table 3: Speed Grade Compatibility

Marking	PC3200 (3-3-3)	PC2700 (2.5-3-3)	PC2100 (2-2-2)	PC2100 (2-3-3)	PC2100 (2.5-3-3)	PC1600 (2-2-2)
-5B ¹	Yes	Yes	Yes	Yes	Yes	Yes
-6	–	Yes	Yes	Yes	Yes	Yes
-6T	–	Yes	Yes	Yes	Yes	Yes
-75E	–	–	Yes	Yes	Yes	Yes
-75Z	–	–	–	Yes	Yes	Yes
-75	–	–	–	–	Yes	Yes
	-5B	-6/-6T	-75E	-75Z	-75	-75

Notes: 1. The -5B device is backward compatible with all slower speed grades. The voltage range of -5B device operating at slower speed grades is $V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$.

Figure 1: 512Mb DDR SDRAM Part Numbers


FBGA Part Number System

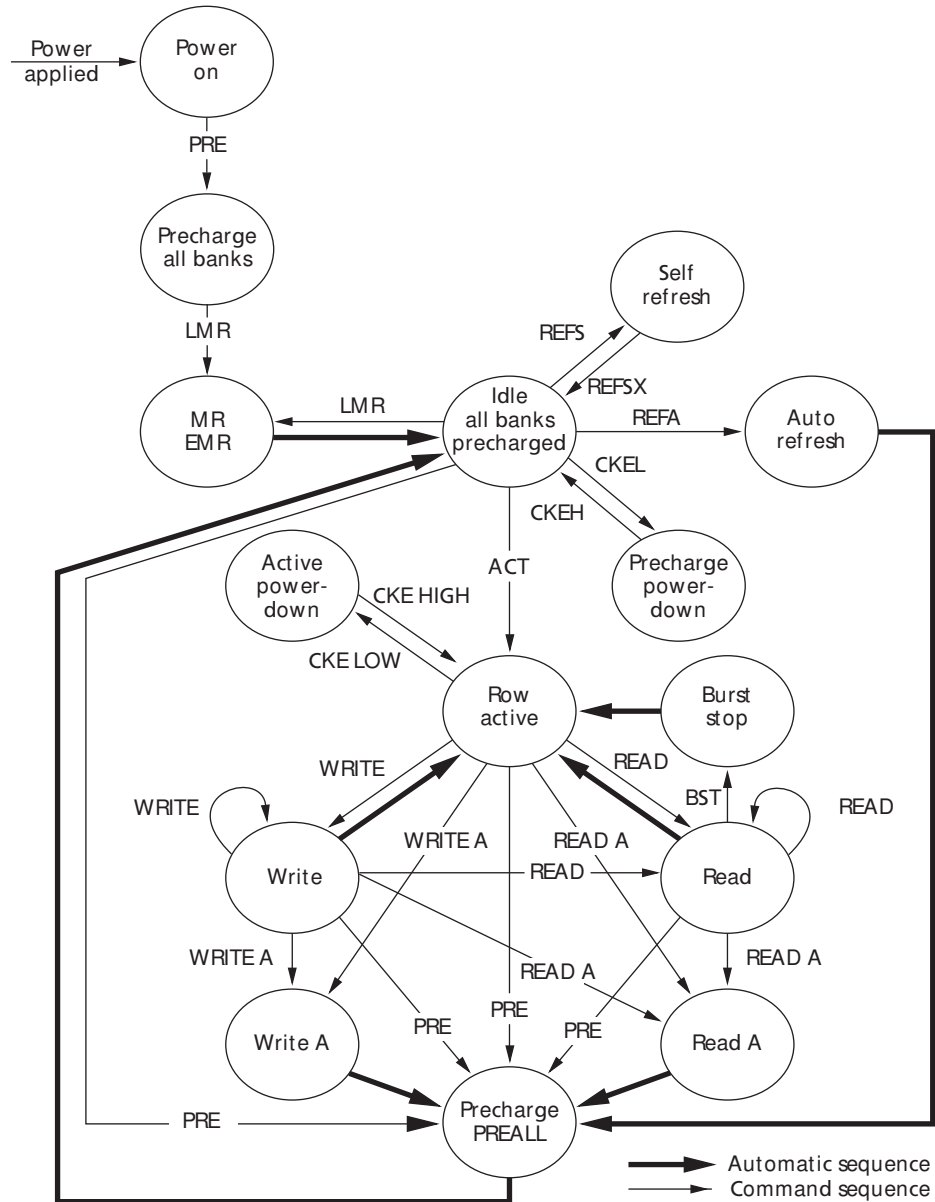
Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: www.micron.com.

Table of Contents

State Diagram	4
Functional Description	5
General Notes	5
Functional Block Diagrams	6
Pin and Ball Assignments and Descriptions	8
Package Dimensions	12
Electrical Specifications – IDD	15
Electrical Specifications – DC and AC	20
Notes	37
Commands	45
DESELECT	49
NO OPERATION (NOP)	49
LOAD MODE REGISTER (LMR)	49
ACTIVE (ACT)	50
READ	51
WRITE	52
PRECHARGE (PRE)	53
BURST TERMINATE (BST)	53
AUTO REFRESH (AR)	53
SELF REFRESH	53
Operations	54
INITIALIZATION	54
REGISTER DEFINITION	57
ACTIVE	61
READ	62
WRITE	74
PRECHARGE	87
AUTO REFRESH	89
SELF REFRESH	90
Power-down (CKE Not Active)	92

State Diagram

Figure 2: Simplified State Diagram



ACT = ACTIVE
 BST = BURST TERMINATE
 CKEH = Exit power-down
 CKEL = Enter power-down
 EMR = Extended mode register
 LMR = LOAD MODE REGISTER
 MR = Mode register

PRE = PRECHARGE
 PREALL = PRECHARGE all banks
 READ A = READ with auto precharge
 REFA = AUTO REFRESH
 REFS = Enter self refresh
 REFSX = Exit self refresh
 WRITE A = WRITE with auto precharge

Note: This diagram represents operations within a single bank only and does not capture concurrent operations in other banks.

Functional Description

The DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which may then be followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC standard for SSTL_2. All full-drive option outputs are SSTL_2, Class II compatible.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ0–DQ7) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15) DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

Functional Block Diagrams

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a 4-bank DRAM.

Figure 3: 128 Meg x 4 Functional Block Diagram

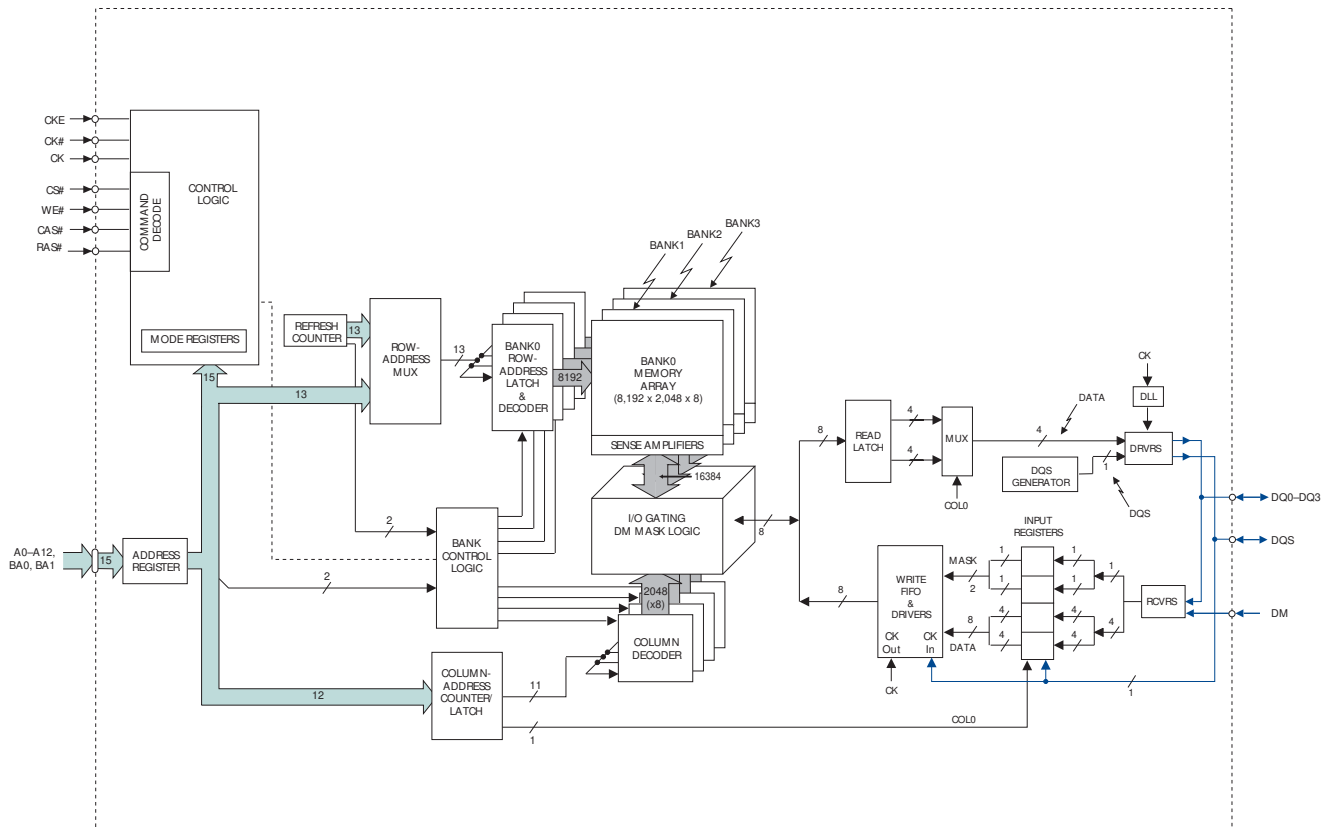


Figure 4: 64 Meg x 8 Functional Block Diagram

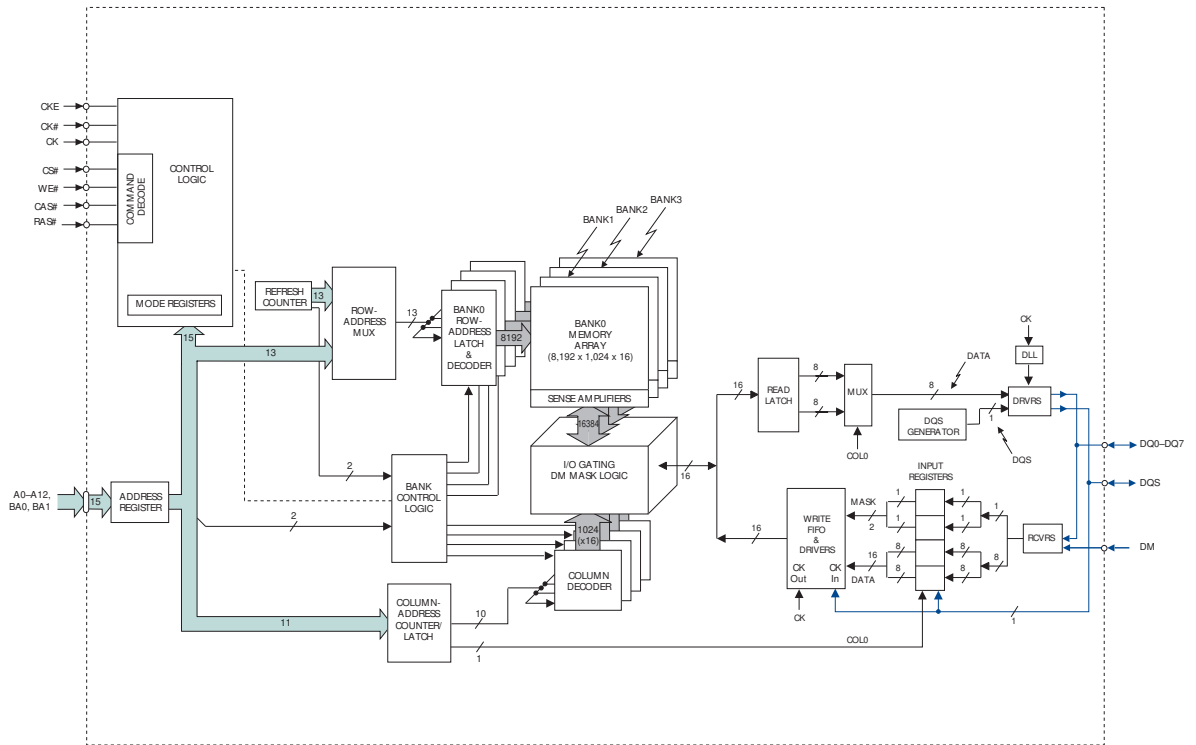
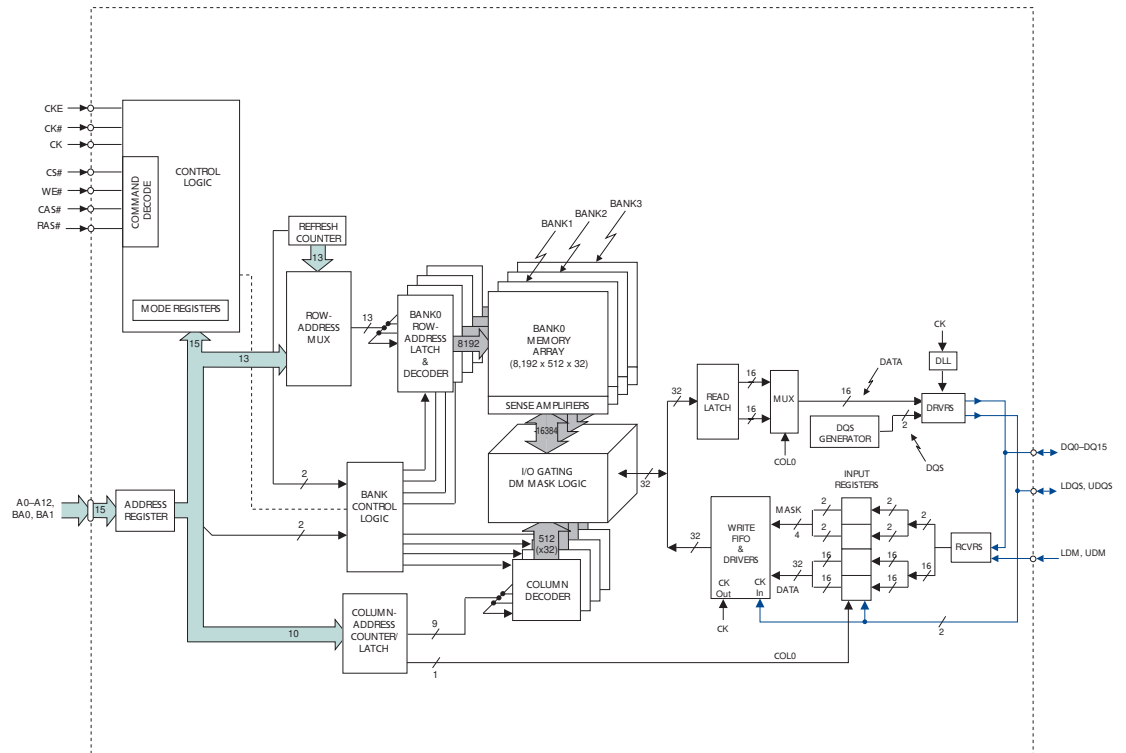


Figure 5: 32 Meg x 16 Functional Block Diagram



Pin and Ball Assignments and Descriptions

Figure 6: 66-Pin TSOP Pin Assignment (Top View)

x4	x8	x16				x16	x8	x4
V _{DD}	V _{DD}	V _{DD}	□	1	•	66	V _{SS}	V _{SS}
NF	DQ0	DQ0	□	2		65	DQ15	DQ7
V _{DDQ}	V _{DDQ}	V _{DDQ}	□	3		64	V _{SSQ}	V _{SSQ}
NC	NC	DQ1	□	4		63	DQ14	NC
DQ0	DQ1	DQ2	□	5		62	DQ13	DQ6
V _{SSQ}	V _{SSQ}	V _{SSQ}	□	6		61	V _{DDQ}	V _{DDQ}
NC	NC	DQ3	□	7		60	DQ12	NC
NF	DQ2	DQ4	□	8		59	DQ11	DQ5
V _{DDQ}	V _{DDQ}	V _{DDQ}	□	9		58	V _{SSQ}	V _{SSQ}
NC	NC	DQ5	□	10		57	DQ10	NC
DQ1	DQ3	DQ6	□	11		56	DQ9	DQ4
V _{SSQ}	V _{SSQ}	V _{SSQ}	□	12		55	V _{DDQ}	V _{DDQ}
NC	NC	DQ7	□	13		54	DQ8	NC
NC	NC	NC	□	14		53	NC	NC
V _{DDQ}	V _{DDQ}	V _{DDQ}	□	15		52	V _{SSQ}	V _{SSQ}
NC	NC	LDQS	□	16		51	UDQS	DQS
NC	NC	NC	□	17		50	DNU	DNU
V _{DD}	V _{DD}	V _{DD}	□	18		49	V _{REF}	V _{REF}
DNU	DNU	DNU	□	19		48	V _{SS}	V _{SS}
NC	NC	LDM	□	20		47	UDM	DM
WE#	WE#	WE#	□	21		46	CK#	CK#
CAS#	CAS#	CAS#	□	22		45	CK	CK
RAS#	RAS#	RAS#	□	23		44	CKE	CKE
CS#	CS#	CS#	□	24		43	NC	NC
NC	NC	NC	□	25		42	A12	A12
BA0	BA0	BA0	□	26		41	A11	A11
BA1	BA1	BA1	□	27		40	A9	A9
A10/AP	A10/AP	A10/AP	□	28		39	A8	A8
A0	A0	A0	□	29		38	A7	A7
A1	A1	A1	□	30		37	A6	A6
A2	A2	A2	□	31		36	A5	A5
A3	A3	A3	□	32		35	A4	A4
V _{DD}	V _{DD}	V _{DD}	□	33		34	V _{SS}	V _{SS}

Figure 7: 60-Ball FBGA Ball Assignment (Top View)

x4 (Top View)

1	2	3	4	5	6	7	8	9
VssQ	NF	Vss	●	A	●	VDD	NF	VDDQ
NC	VDDQ	DQ3	●	B	●	DQ0	VssQ	NC
NC	VssQ	NF	●	C	●	NF	VDDQ	NC
NC	VDDQ	DQ2	●	D	●	DQ1	VssQ	NC
NC	VssQ	DQS	●	E	●	NC	VDDQ	NC
VREF	Vss	DM	●	F	●	NC	VDD	DNU
	CK	CK#	●	G	●	WE#	CAS#	
	A12	CKE	●	H	●	RAS#	CS#	
	A11	A9	●	J	●	BA1	BA0	
	A8	A7	●	K	●	A0	A10	
	A6	A5	●	L	●	A2	A1	
	A4	Vss	●	M	●	VDD	A3	

x8 (Top View)

1	2	3	4	5	6	7	8	9
VssQ	DQ7	Vss	●	A	●	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	●	B	●	DQ1	VssQ	NC
NC	VssQ	DQ5	●	C	●	DQ2	VDDQ	NC
NC	VDDQ	DQ4	●	D	●	DQ3	VssQ	NC
NC	VssQ	DQS	●	E	●	NC	VDDQ	NC
VREF	Vss	DM	●	F	●	NC	VDD	DNU
	CK	CK#	●	G	●	WE#	CAS#	
	A12	CKE	●	H	●	RAS#	CS#	
	A11	A9	●	J	●	BA1	BA0	
	A8	A7	●	K	●	A0	A10	
	A6	A5	●	L	●	A2	A1	
	A4	Vss	●	M	●	VDD	A3	

x16 (Top View)

1	2	3	4	5	6	7	8	9
VssQ	DQ15	Vss	●	A	●	VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13	●	B	●	DQ2	VssQ	DQ1
DQ12	VssQ	DQ11	●	C	●	DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9	●	D	●	DQ6	VssQ	DQ5
DQ8	VssQ	UDQS	●	E	●	LDQS	VDDQ	DQ7
VREF	Vss	UDM	●	F	●	LDM	VDD	DNU
	CK	CK#	●	G	●	WE#	CAS#	
	A12	CKE	●	H	●	RAS#	CS#	
	A11	A9	●	J	●	BA1	BA0	
	A8	A7	●	K	●	A0	A10	
	A6	A5	●	L	●	A2	A1	
	A4	Vss	●	M	●	VDD	A3	

Table 4: Pin and Ball Descriptions

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
K7, L8, L7, M8, M2, L3, L2, K3, K2, J3, K8, J2, H2	29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 28 41, 42	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
J8, J7	26, 27	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER (LMR) command.
G2, G3	45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
H3	44	CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V _{DD} is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only.
H8	24	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F3 F7, F3	47 20, 47	DM LDM, UDM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16, LDM is DM for DQ0–DQ7 and UDM is DM for DQ8–DQ15. Pin 20 is a NC on x4 and x8.
H7, G8, G7	23, 22, 21	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
A8, B9, B7, C9, C7, D9, D7, E9, E1, D3, D1, C3, C1, B3, B1, A2	2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0–DQ2 DQ3–DQ5 DQ6–DQ8 DQ9–DQ11 DQ12–DQ14 DQ15	I/O	Data input/output: Data bus for x16.
A8, B7, C7, D7, D3, C3, B3, A2	2, 5, 8, 11, 56, 59, 62, 65	DQ0–DQ2 DQ3–DQ5 DQ6, DQ7	I/O	Data input/output: Data bus for x8.
B7, D7, D3, B3	5, 11, 56, 62	DQ0–DQ2 DQ3	I/O	Data input/output: Data bus for x4.

Table 4: Pin and Ball Descriptions (continued)

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
E3 E7 E3	51 16 51	DQS LDQS UDQS	I/O	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For the x16, LDQS is DQS for DQ0–DQ7 and UDQS is DQS for DQ8–DQ15. Pin 16 (E7) is NC on x4 and x8.
F8, M7, A7	1, 18, 33	VDD	Supply	Power supply: +2.5V ±0.2V. (+2.6V ±0.1V for DDR400).
B2, D2, C8, E8, A9	3, 9, 15, 55, 61	VDDQ	Supply	DQ power supply: +2.5V ±0.2V (+2.6V ±0.1V for DDR400). Isolated on the die for improved noise immunity.
F1	49	VREF	Supply	SSTL_2 reference voltage.
A3, F2, M3	34, 48, 66	VSS	Supply	Ground.
A1, C2, E2, B8, D8	6, 12, 52, 58, 64	VSSQ	Supply	DQ ground: Isolated on the die for improved noise immunity.
–	14, 17, 25, 43, 53	NC	–	No connect for x16: These pins should be left unconnected.
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7	4, 7, 10, 13, 14, 16, 17, 20, 25, 43, 53, 54, 57, 60, 63	NC	–	No connect for x8: These pins should be left unconnected.
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7	4, 7, 10, 13, 14, 16, 17, 20, 25, 43, 53, 54, 57, 60, 63	NC	–	No connect for x4: These pins should be left unconnected.
A2, A8, C3, C7	2, 8, 59, 65	NF	–	No function for x4: These pins should be left unconnected.
F9	19, 50	DNU	–	Do not use: Must float to minimize noise on VREF.

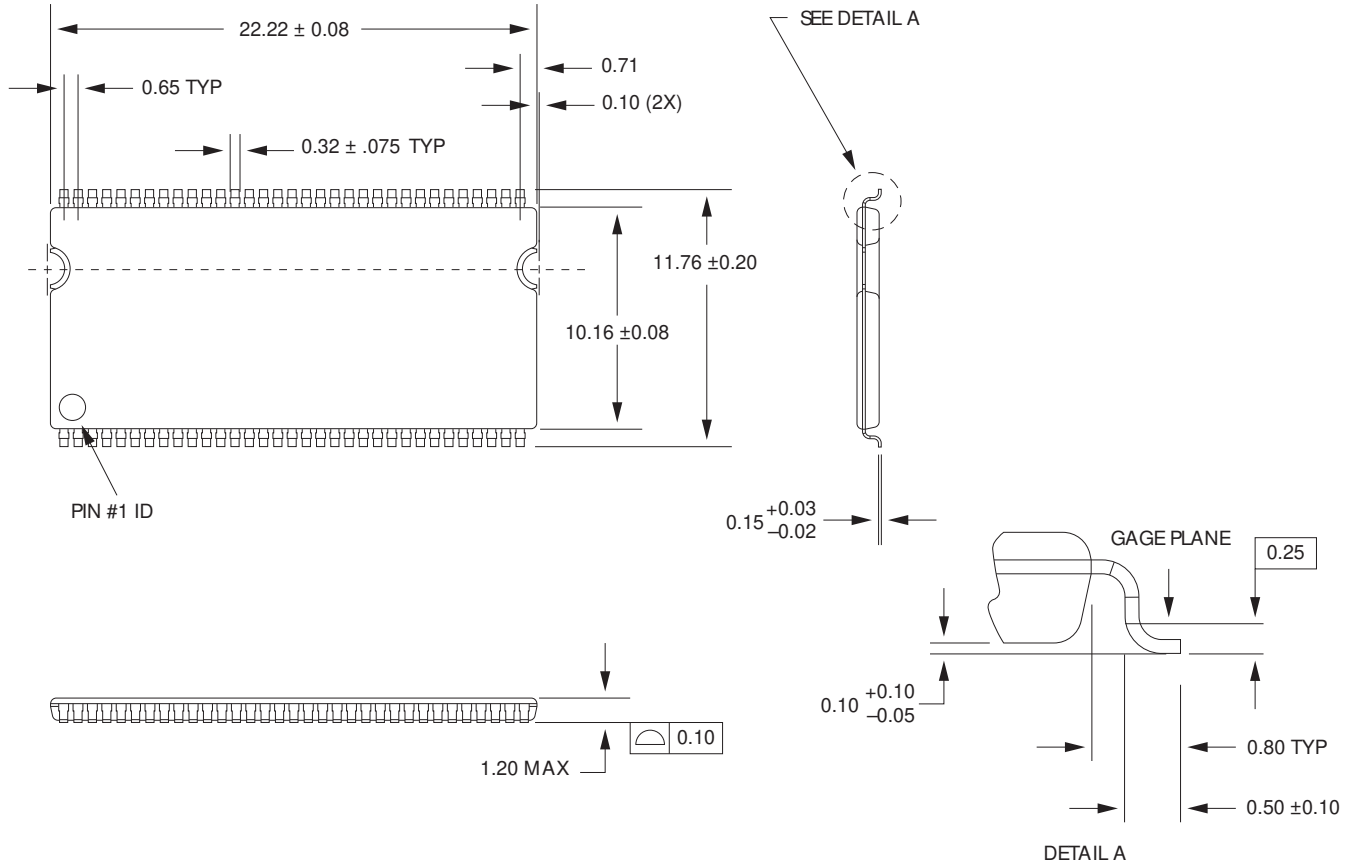
Table 5: Reserved NC Pin and Ball Descriptions

NC pins not listed may also be reserved for other uses; this table defines NC pins of importance

TSOP Numbers	Symbol	Type	Description
17	A13	Input	Address input A13 for 1Gb devices.

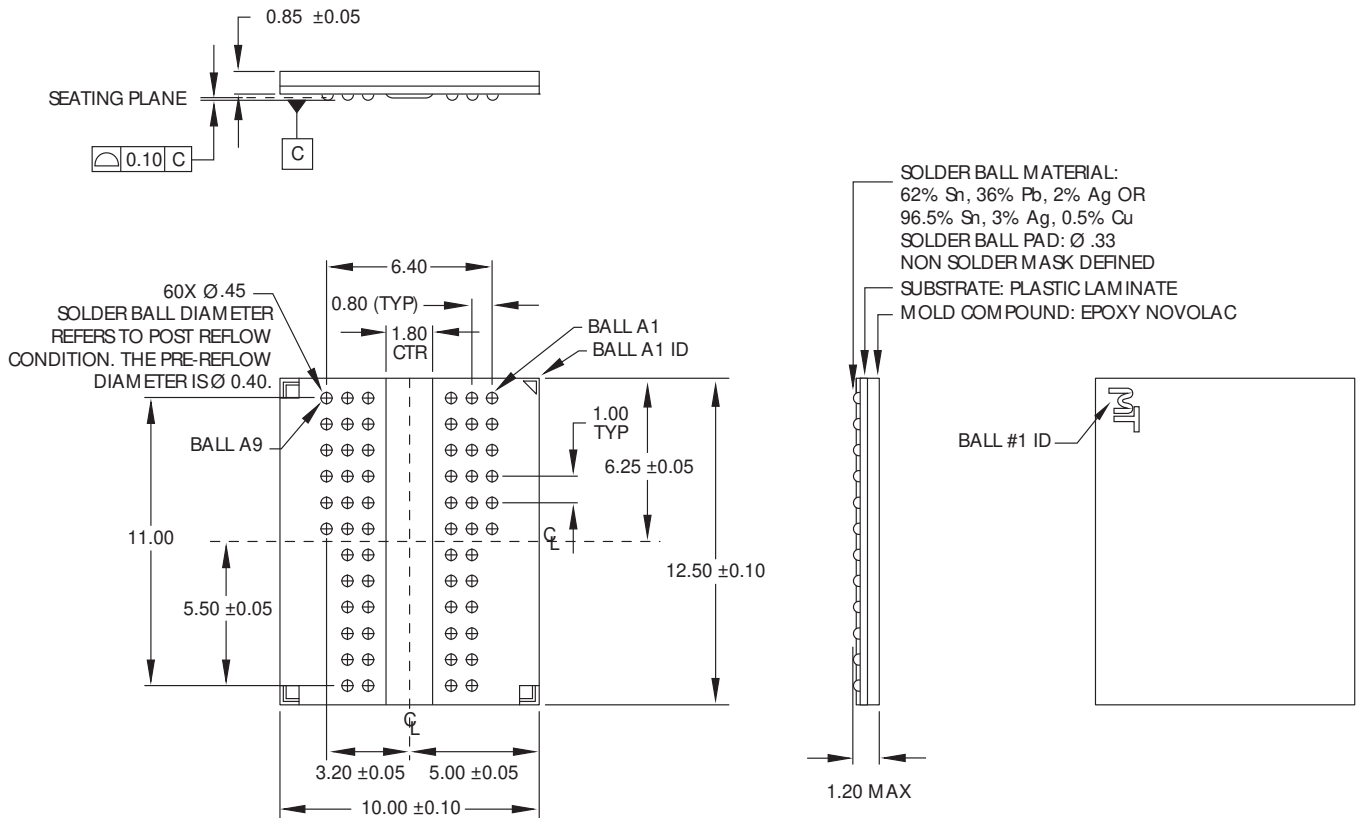
Package Dimensions

Figure 8: 66-Pin Plastic TSOP (400 mil)



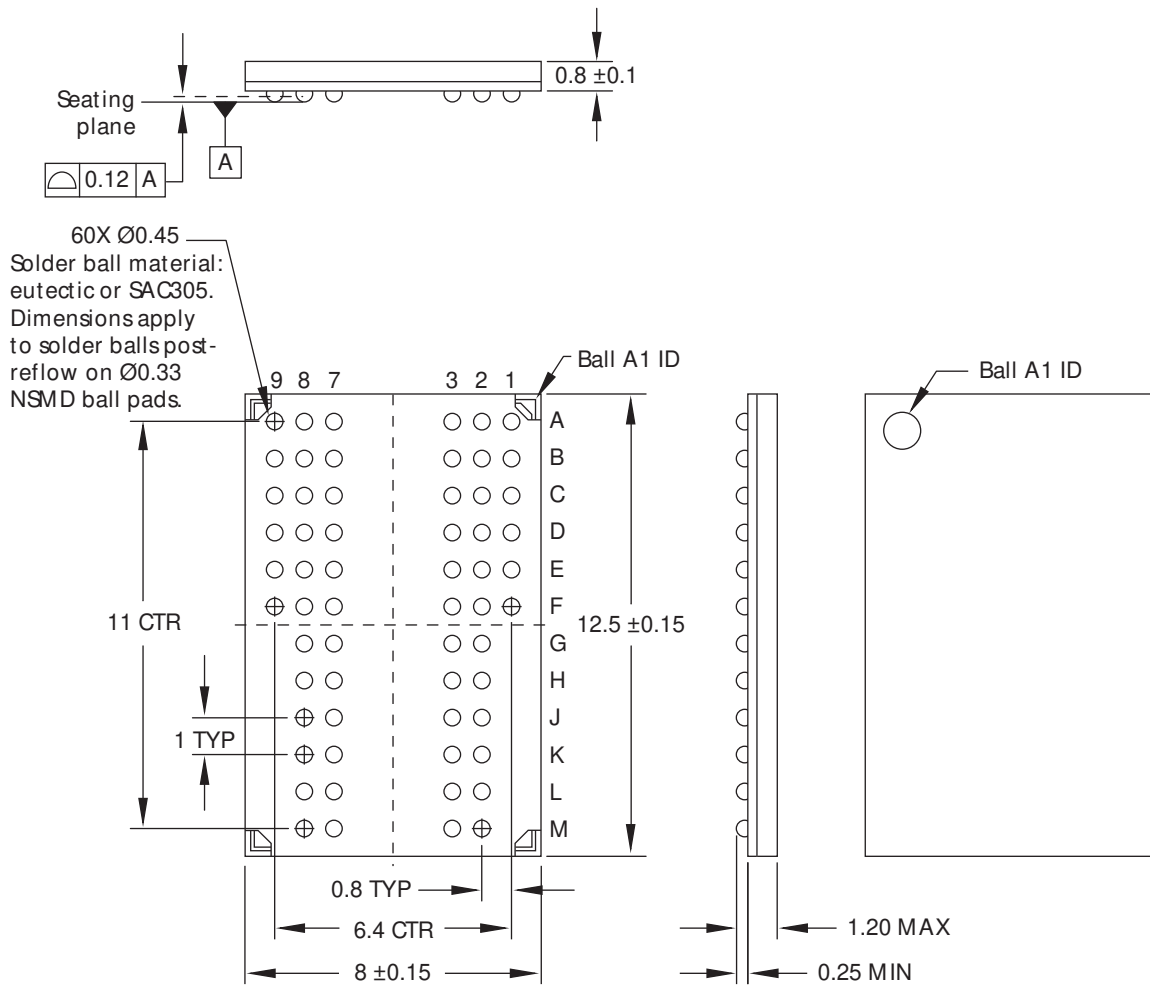
- Notes:
1. All dimensions are in millimeters.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
 3. Not all packages will have the half moon shaped notches as shown.

Figure 9: 60-Ball FBGA (10mm x 12.5mm)



- Notes: 1. All dimensions are in millimeters.
2. Topside part marking decoder can be found on Micron's Web site.

Figure 10: 60-Ball FBGA (8mm x 12.5mm)



- Notes: 1. All dimensions are in millimeters.
2. Topside part marking decoder can be found on Micron's Web site.

Electrical Specifications – IDD

Table 6: IDD Specifications and Conditions (x4, x8) Die Revision F Only

V_{DDQ} = +2.6V ±0.1V, V_{DD} = +2.6V ±0.1V (-5B); V_{DDQ} = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V (-6, -6T, -75E, -75Z, -75);
 0°C ≤ T_A ≤ +70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

Parameter/Condition	Symbol	-5B	-6/6T	-75E	-75Z/-75	Units	Notes	
Operating one-bank active-precharge current: t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	155	130	130	115	mA	23, 48	
Operating one-bank active-read-precharge current: Burst = 4; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1}	185	160	160	145	mA	23, 48	
Precharge power-down standby current: All banks idle; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = (LOW)	I _{DD2P}	5	5	5	5	mA	24, 33	
Idle standby current: CS# = HIGH; All banks are idle; t _{CK} = t _{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DQS, and DM	I _{DD2F}	55	45	45	40	mA	51	
Active power-down standby current: One bank active; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	I _{DD3P}	45	35	35	30	mA	24, 33	
Active standby current: CS# = HIGH; CKE = HIGH; One bank active; t _{RC} = t _{RAS} (MAX); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N}	60	50	50	45	mA	23	
Operating burst read current: Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA	I _{DD4R}	190	165	165	145	mA	23, 48	
Operating burst write current: Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W}	195	175	155	135	mA	23	
Auto refresh burst current:	t _{RFC} = t _{RFC} (MIN)	I _{DD5}	345	290	290	280	mA	50
	t _{RFC} = 7.8μs	I _{DD5A}	11	10	10	10	mA	28, 50
Self refresh current: CKE ≤ 0.2V	Standard	I _{DD6}	5	5	5	5	mA	12
	Low power (L)	I _{DD6A}	3	3	3	3	mA	12
Operating bank interleave read current: Four bank interleaving READs (burst = 4) with auto precharge, t _{RC} = minimum t _{RC} allowed; t _{CK} = t _{CK} (MIN); Address and control inputs change only during active READ or WRITE commands	I _{DD7}	450	405	400	350	mA	23, 49	

Table 7: Idd Specifications and Conditions (x16) Die Revision F Only

VDDQ = +2.6V ±0.1V, VDD = +2.6V ±0.1V (-5B); VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V (-6, -6T, -75E, -75Z, -75);
 0°C ≤ T_A ≤ +70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

Parameter/Condition	Symbol	-5B	-6/6T	-75E	-75Z/-75	Units	Notes	
Operating one-bank active-precharge current: t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	155	130	130	115	mA	23, 48	
Operating one-bank active-read-precharge current: Burst = 4; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1}	195	160	160	145	mA	23, 48	
Precharge power-down standby current: All banks idle; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = (LOW)	I _{DD2P}	5	5	5	5	mA	24, 33	
Idle standby current: CS# = HIGH; All banks are idle; t _{CK} = t _{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DQS, and DM	I _{DD2F}	55	45	45	40	mA	51	
Active power-down standby current: One bank active; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	I _{DD3P}	45	35	35	30	mA	24, 33	
Active standby current: CS# = HIGH; CKE = HIGH; One bank active; t _{RC} = t _{RAS} (MAX); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N}	60	50	50	45	mA	23	
Operating burst read current: Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA	I _{DD4R}	210	165	165	145	mA	23, 48	
Operating burst write current: Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W}	215	195	160	135	mA	23	
Auto refresh burst current:	t _{RFC} = t _{RFC} (MIN)	I _{DD5}	345	290	290	280	mA	50
	t _{RFC} = 7.8μs	I _{DD5A}	11	10	10	10	mA	28, 50
Self refresh current: CKE ≤ 0.2V	Standard	I _{DD6}	6	5	5	5	mA	12
	Low power (L)	I _{DD6A}	4	3	3	3	mA	12
Operating bank interleave read current: Four bank interleaving READs (burst = 4) with auto precharge, t _{RC} = minimum t _{RC} allowed; t _{CK} = t _{CK} (MIN); Address and control inputs change only during active READ or WRITE commands	I _{DD7}	480	405	400	350	mA	23, 49	

Table 8: Idd Specifications and Conditions (x4, x8) Die Revision J Only

VDDQ = +2.6V ±0.1V, VDD = +2.6V ±0.1V (-5B); VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V (-6, -6T);
0°C ≤ T_A ≤ +70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

Parameter/Condition	Symbol	-5B	-6/6T	Units	Notes	
Operating one-bank active-precharge current: t ^{RC} = t ^{RC} (MIN); t ^{CK} = t ^{CK} (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	TBD	TBD	mA	23, 48	
Operating one-bank active-read-precharge current: Burst = 4; t ^{RC} = t ^{RC} (MIN); t ^{CK} = t ^{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1}	TBD	TBD	mA	23, 48	
Precharge power-down standby current: All banks idle; Power-down mode; t ^{CK} = t ^{CK} (MIN); CKE = (LOW)	I _{DD2P}	TBD	TBD	mA	24, 33	
Idle standby current: CS# = HIGH; All banks are idle; t ^{CK} = t ^{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DQS, and DM	I _{DD2F}	TBD	TBD	mA	51	
Active power-down standby current: One bank active; Power-down mode; t ^{CK} = t ^{CK} (MIN); CKE = LOW	I _{DD3P}	TBD	TBD	mA	24, 33	
Active standby current: CS# = HIGH; CKE = HIGH; One bank active; t ^{RC} = t ^{RAS} (MAX); t ^{CK} = t ^{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N}	TBD	TBD	mA	23	
Operating burst read current: Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; t ^{CK} = t ^{CK} (MIN); I _{OUT} = 0mA	I _{DD4R}	TBD	TBD	mA	23, 48	
Operating burst write current: Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; t ^{CK} = t ^{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W}	TBD	TBD	mA	23	
Auto refresh burst current:	t ^{RFC} = t ^{RFC} (MIN)	I _{DD5}	TBD	TBD	mA	50
	t ^{RFC} = 7.8μs	I _{DD5A}	TBD	TBD	mA	28, 50
Self refresh current: CKE ≤ 0.2V	Standard	I _{DD6}	TBD	TBD	mA	12
	Low power (L)	I _{DD6A}	TBD	TBD	mA	12
Operating bank interleave read current: Four bank interleaving READs (burst = 4) with auto precharge, t ^{RC} = minimum t ^{RC} allowed; t ^{CK} = t ^{CK} (MIN); Address and control inputs change only during active READ or WRITE commands	I _{DD7}	TBD	TBD	mA	23, 49	

Table 9: IDD Specifications and Conditions (x16) Die Revision J Only

VDDQ = +2.6V ±0.1V, VDD = +2.6V ±0.1V (-5B); VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V (-6, -6T);
 0°C ≤ T_A ≤ +70°C; Notes: 1–5, 11, 13, 15, 47; Notes appear on pages 37–42; See also Table 10 on page 20

Parameter/Condition	Symbol	-5B	-6/6T	Units	Notes
Operating one-bank active-precharge current: t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	IDD0	TBD	TBD	mA	23, 48
Operating one-bank active-read-precharge current: Burst = 4; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	IDD1	TBD	TBD	mA	23, 48
Precharge power-down standby current: All banks idle; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = (LOW)	IDD2P	TBD	TBD	mA	24, 33
Idle standby current: CS# = HIGH; All banks are idle; t _{CK} = t _{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DQS, and DM	IDD2F	TBD	TBD	mA	51
Active power-down standby current: One bank active; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	IDD3P	TBD	TBD	mA	24, 33
Active standby current: CS# = HIGH; CKE = HIGH; One bank active; t _{RC} = t _{RAS} (MAX); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	TBD	TBD	mA	23
Operating burst read current: Burst = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA	IDD4R	TBD	TBD	mA	23, 48
Operating burst write current: Burst = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	TBD	TBD	mA	23
Auto refresh burst current:	t _{RFC} = t _{RFC} (MIN)	IDD5	TBD	mA	50
	t _{RFC} = 7.8μs	IDD5A	TBD	mA	28, 50
Self refresh current: CKE ≤ 0.2V	Standard	IDD6	TBD	mA	12
	Low power (L)	IDD6A	TBD	mA	12
Operating bank interleave read current: Four bank interleaving READs (burst = 4) with auto precharge, t _{RC} = minimum t _{RC} allowed; t _{CK} = t _{CK} (MIN); Address and control inputs change only during active READ or WRITE commands	IDD7	TBD	TBD	mA	23, 49



Table 10: IDD Test Cycle Times

Values reflect number of clock cycles for each test

IDD Test	Speed Grade	Clock Cycle Time	t _{RRD}	t _{RCD}	t _{RAS}	t _{RP}	t _{RC}	t _{RFC}	t _{REFI}	CL
IDD0	-75/75Z	7.5ns	n/a	n/a	6	3	9	n/a	n/a	n/a
	-75E	7.5ns	n/a	n/a	6	2	8	n/a	n/a	n/a
	-6/-6T	6ns	n/a	n/a	7	3	10	n/a	n/a	n/a
	-5B	5ns	n/a	n/a	8	3	11	n/a	n/a	n/a
IDD1	-75	7.5ns	n/a	n/a	6	3	9	n/a	n/a	2.5
	-75Z	7.5ns	n/a	n/a	6	3	9	n/a	n/a	2
	-75E	7.5ns	n/a	n/a	6	2	8	n/a	n/a	2
	-6/-6T	6ns	n/a	n/a	7	3	10	n/a	n/a	2.5
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	3
IDD4R	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2.5
	-75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2.5
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	3
IDD4W	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
IDD5	-75/75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	10	10	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	9	9	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	12	12	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	14	14	n/a
IDD5A	-75/75Z	7.5ns	n/a	n/a	n/a	n/a	n/a	10	1,029	n/a
	-75E	7.5ns	n/a	n/a	n/a	n/a	n/a	10	1,029	n/a
	-6/-6T	6ns	n/a	n/a	n/a	n/a	n/a	12	1,288	n/a
	-5B	5ns	n/a	n/a	n/a	n/a	n/a	14	1,546	n/a
IDD7	-75	7.5ns	2	3	n/a	3	10	n/a	n/a	2.5
	-75Z	7.5ns	2	3	n/a	3	10	n/a	n/a	2
	-75E	7.5ns	2	3	n/a	2	8	n/a	n/a	2
	-6/-6T	6ns	2	3	n/a	3	10	n/a	n/a	2.5
	-5B	5ns	2	3	n/a	3	11	n/a	n/a	3

Electrical Specifications – DC and AC

Stresses greater than those listed in Table 11 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 11: Absolute Maximum Ratings

Parameter	Min	Max	Units
VDD supply voltage relative to VSS	-1V	+3.6V	V
VDDQ supply voltage relative to VSS	-1V	+3.6V	V
VREF and inputs voltage relative to VSS	-1V	+3.6V	V
I/O pins voltage relative to VSS	-0.5V	VDDQ + 0.5V	V
Storage temperature (plastic)	-55	+150	°C
Short circuit output current	-	50	mA

Table 12: DC Electrical Characteristics and Operating Conditions (-5B)

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 37; VDDQ = +2.6V ±0.1V, VDD = +2.6V ±0.1V

Parameter/Condition	Symbol	Min	Max	Units	Notes	
Supply voltage	VDD	+2.5	+2.7	V	37, 42	
I/O supply voltage	VDDQ	+2.5	+2.7	V	37, 42, 45	
I/O reference voltage	VREF	0.49 × VDDQ	0.51 × VDDQ	V	7, 45	
I/O termination voltage (system)	VTT	VREF - 0.04	VREF + 0.04	V	8, 45	
Input high (logic 1) voltage	VIH(DC)	VREF + 0.15	VDD + 0.3	V	29	
Input low (logic 0) voltage	VIL(DC)	-0.3	VREF - 0.15	V	29	
Input leakage current: Any input 0V ≤ VIN ≤ VDD, VREF pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	II	-2	+2	µA		
Output leakage current: (DQ are disabled; 0V ≤ VOUT ≤ VDDQ)	Ioz	-5	+5	µA		
Full-drive option output levels (x4, x8, x16):	High current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)	IOH	-16.8	-	mA	38, 40
	Low current (VOUT = 0.373V, maximum VREF, maximum VTT)	IOL	+16.8	-	mA	
Reduced-drive option output levels:	High current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)	IOHR	-9	-	mA	39, 40
	Low current (VOUT = 0.373V, maximum VREF, maximum VTT)	IOLR	+9	-	mA	
Ambient operating temperatures	Commercial	TA	0	+70	°C	
	Industrial	TA	-40	+85	°C	



Table 13: DC Electrical Characteristics and Operating Conditions (-6, -6T, -75E, -75Z, -75)

Notes: 1–5, 17 apply to the entire table; Notes appear on page 37; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V

Parameter/Condition	Symbol	Min	Max	Units	Notes	
Supply voltage	VDD	+2.3	+2.7	V	37, 42	
I/O supply voltage	VDDQ	+2.3	+2.7	V	37, 42, 45	
I/O reference voltage	VREF	0.49 × VDDQ	0.51 × VDDQ	V	7, 45	
I/O termination voltage (system)	VTT	VREF - 0.04	VREF + 0.04	V	8, 45	
Input high (logic 1) voltage	VIH(DC)	VREF + 0.15	VDD + 0.3	V	29	
Input low (logic 0) voltage	VIL(DC)	-0.3	VREF - 0.15	V	29	
Input leakage current: Any input 0V ≤ VIN ≤ VDD, VREF pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	II	-2	+2	μA		
Output leakage current: (DQ are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	-5	+5	μA		
Full-drive option output levels (x4, x8, x16):	High current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)	IOH	-16.8	-	mA	38, 40
	Low current (VOUT = 0.373V, maximum VREF, maximum VTT)	IOL	+16.8	-	mA	
Reduced-drive option output levels:	High current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)	IOHR	-9	-	mA	39, 40
	Low current (VOUT = 0.373V, maximum VREF, maximum VTT)	IOLR	+9	-	mA	
Ambient operating temperatures	Commercial	TA	0	+70	°C	
	Industrial	TA	-40	+85	°C	

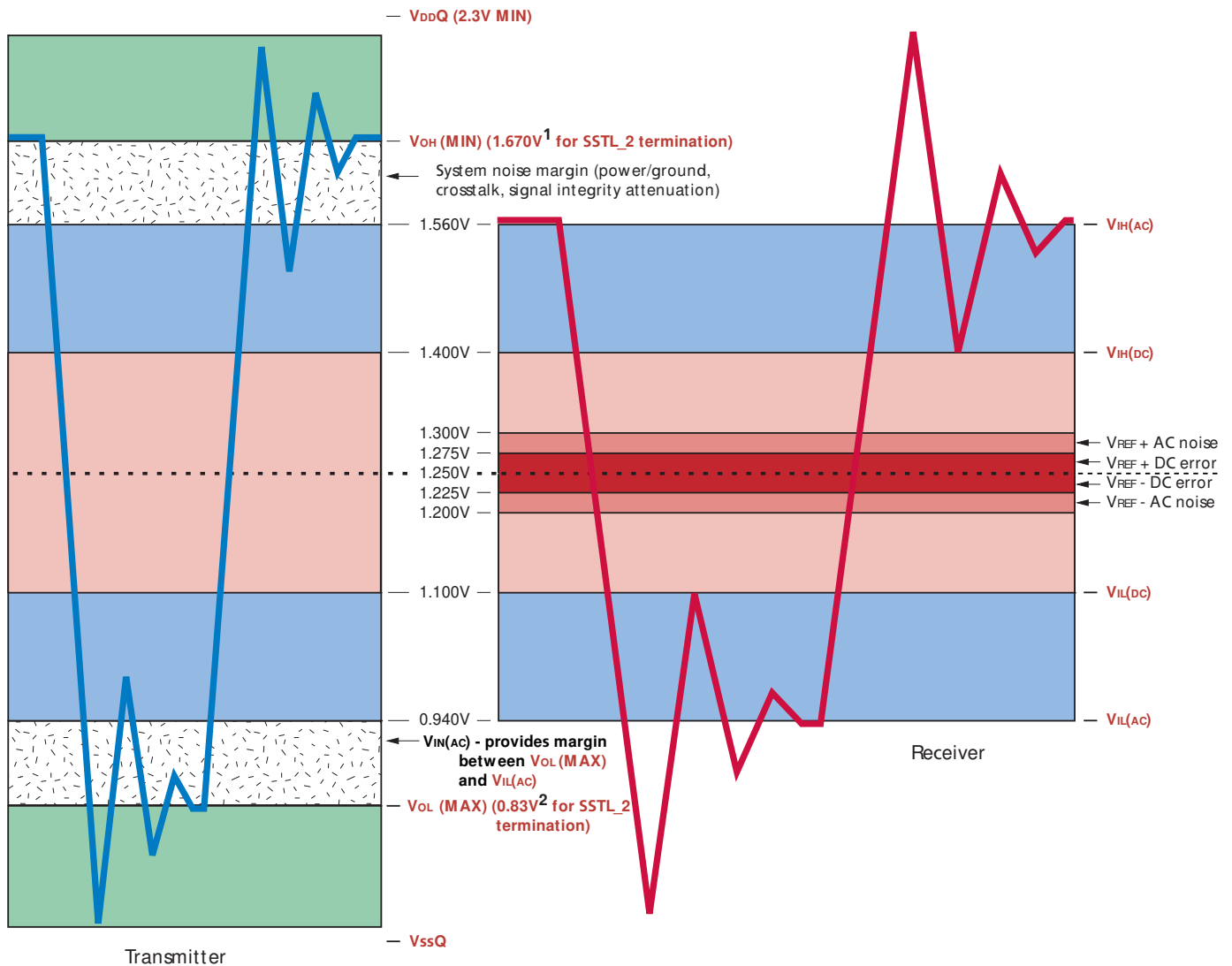
Table 14: AC Input Operating Conditions

Notes: 1–5, 17 apply to the entire table; Notes appear on page 37;

0°C ≤ TA ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V (VDDQ = +2.6V ±0.1V, VDD = +2.6V ±0.1V for -5B)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage	VIH(AC)	VREF + 0.310	-	V	15, 29, 41
Input low (logic 0) voltage	VIL(AC)	-	VREF - 0.310	V	15, 29, 41
I/O reference voltage	VREF(AC)	0.49 × VDDQ	0.51 × VDDQ	V	7

Figure 11: Input Voltage Waveform



- Notes:
1. V_{OH} (MIN) with test load is 1.927V.
 2. V_{OL} (MAX) with test load is 0.373V.
 3. Numbers in diagram reflect nominal values utilizing circuit below for all devices other than -5B.

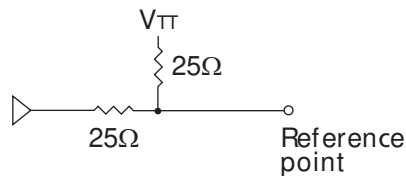


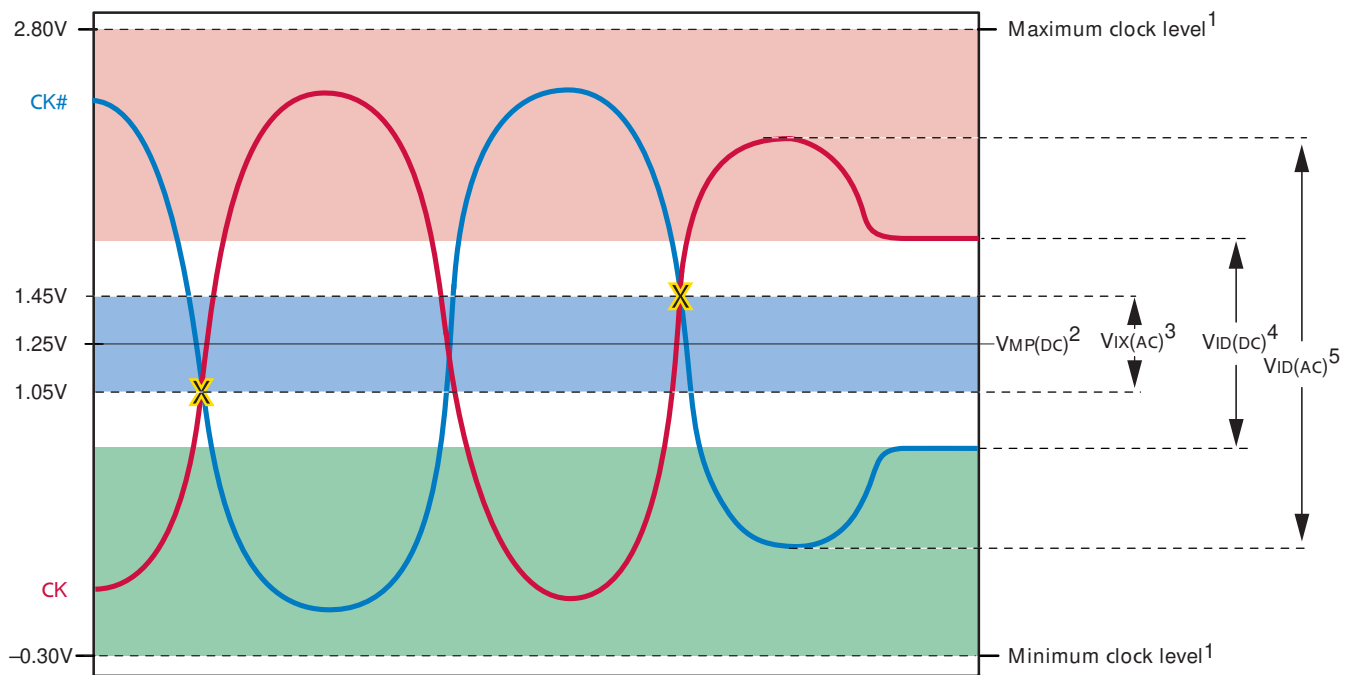
Table 15: Clock Input Operating Conditions

Notes: 1–5, 16, 17, 31 apply to the entire table; Notes appear on page 37;

$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$, $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ ($V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$, $V_{DD} = +2.6\text{V} \pm 0.1\text{V}$ for -5B)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input mid-point voltage: CK and CK#	VMP(DC)	1.15	1.35	V	7, 10
Clock input voltage level: CK and CK#	VIN(DC)	-0.3	$V_{DDQ} + 0.3$	V	7
Clock input differential voltage: CK and CK#	VID(DC)	0.36	$V_{DDQ} + 0.6$	V	7, 9
Clock input differential voltage: CK and CK#	VID(AC)	0.7	$V_{DDQ} + 0.6$	V	9
Clock input crossing point voltage: CK and CK#	VIX(AC)	$0.5 \times V_{DDQ} - 0.2$	$0.5 \times V_{DDQ} + 0.2$	V	10

Figure 12: SSTL_2 Clock Input



- Notes:
1. CK or CK# may not be more positive than $V_{DDQ} + 0.3\text{V}$ or more negative than $V_{SS} - 0.3\text{V}$.
 2. This provides a minimum of 1.15V to a maximum of 1.35V and is always half of V_{DDQ} .
 3. CK and CK# must cross in this region.
 4. CK and CK# must meet at least VID(DC) MIN when static and is centered around VMP(DC).
 5. CK and CK# must have a minimum 700mV peak-to-peak swing.
 6. For AC operation, all DC clock requirements must also be satisfied.
 7. Numbers in diagram reflect nominal values for all devices other than -5B.

Table 16: Capacitance (x4, x8 TSOP)

Note: 14 applies to the entire table; Notes appear on page 37

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ0–DQ3 (x4), DQ0–DQ7 (x8)	DC _{Io}	–	0.50	pF	25
Delta input capacitance: Command and address	DC _{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC _{I2}	–	0.25	pF	30
Input/output capacitance: DQ, DQS, DM	Q _o	4.0	5.0	pF	
Input capacitance: Command and address	Q ₁	2.0	3.0	pF	
Input capacitance: CK, CK#	Q ₂	2.0	3.0	pF	
Input capacitance: CKE	Q ₃	2.0	3.0	pF	

Table 17: Capacitance (x4, x8 FBGA)

Note: 14 applies to the entire table; Notes appear on page 37

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ, DQS, DM	DC _{Io}	–	0.50	pF	25
Delta input capacitance: Command and address	DC _{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC _{I2}	–	0.25	pF	30
Input/output capacitance: DQ, DQS, DM	Q _o	3.5	4.5	pF	
Input capacitance: Command and address	Q ₁	1.5	2.5	pF	
Input capacitance: CK, CK#	Q ₂	1.5	2.5	pF	
Input capacitance: CKE	Q ₃	1.5	2.5	pF	

Table 18: Capacitance (x16 TSOP)

Note: 14 applies to the entire table; Notes appear on page 37

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ0–DQ7, LDQS, LDM	DC _{IoL}	–	0.50	pF	25
Delta input/output capacitance: DQ8–DQ15, UDQS, UDM	DC _{IoU}	–	0.50	pF	25
Delta input capacitance: Command and address	DC _{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC _{I2}	–	0.25	pF	30
Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM	Q _o	4.0	5.0	pF	
Input capacitance: Command and address	Q ₁	2.0	3.0	pF	
Input capacitance: CK, CK#	Q ₂	2.0	3.0	pF	
Input capacitance: CKE	Q ₃	2.0	3.0	pF	

Table 19: Capacitance (x16 FBGA)

Note: 14 applies to the entire table; Notes appear on page 37

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ0–DQ7, LDQS, LDM	DC _{IoL}	–	0.50	pF	25
Delta input/output capacitance: DQ8–DQ15, UDQS, UDM	DC _{IoU}	–	0.50	pF	25
Delta input capacitance: Command and address	DC _{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC _{I2}	–	0.25	pF	30
Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM	Q _o	3.5	4.5	pF	
Input capacitance: Command and address	Q ₁	1.5	2.5	pF	
Input capacitance: CK, CK#	Q ₂	1.5	2.5	pF	
Input capacitance: CKE	Q ₃	1.5	2.5	pF	

Table 20: Electrical Characteristics and Recommended AC Operating Conditions (-5B)

Notes 1–6, 16–18, 34 apply to the entire table; Notes appear on page 37;
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$, $V_{DD} = +2.6\text{V} \pm 0.1\text{V}$

AC Characteristics		-5B		Units	Notes	
Parameter	Symbol	Min	Max			
Access window of DQ from CK/CK#	t_{AC}	-0.70	+0.70	ns		
CK high-level width	t_{CH}	0.45	0.55	t_{CK}	31	
Clock cycle time	CL = 3	$t_{CK} (3)$	5	7.5	ns	52
	CL = 2.5	$t_{CK} (2.5)$	6	13	ns	46, 52
	CL = 2	$t_{CK} (2)$	7.5	13	ns	46, 52
CK low-level width	t_{CL}	0.45	0.55	t_{CK}	31	
DQ and DM input hold time relative to DQS	t_{DH}	0.40	–	ns	27, 32	
DQ and DM input pulse width (for each input)	t_{DIPW}	1.75	–	ns	32	
Access window of DQS from CK/CK#	t_{DQSK}	-0.60	+0.60	ns		
DQS input high pulse width	t_{DQSH}	0.35	–	t_{CK}		
DQS input low pulse width	t_{DQSL}	0.35	–	t_{CK}		
DQS-DQ skew, DQS to last DQ valid, per group, per access	t_{DQSQ}	–	0.40	ns	26, 27	
WRITE command to first DQS latching transition	t_{DQSS}	0.72	1.28	t_{CK}		
DQ and DM input setup time relative to DQS	t_{DS}	0.40	–	ns	27, 32	
DQS falling edge from CK rising – hold time	t_{DSH}	0.2	–	t_{CK}		
DQS falling edge to CK rising – setup time	t_{DSS}	0.2	–	t_{CK}		
Half-clock period	t_{HP}	t_{CH}, t_{CL}	–	ns	35	
Data-out High-Z window from CK/CK#	t_{HZ}	–	+0.70	ns	19, 43	
Address and control input hold time (slew rate ≥ 0.5 V/ns)	t_{IH_F}	0.60	–	ns	15	
Address and control input pulse width (for each input)	t_{IPW}	2.2	–	ns		
Address and control input setup time (slew rate ≥ 0.5 V/ns)	t_{IS_F}	0.60	–	ns	15	
Data-out Low-Z window from CK/CK#	t_{LZ}	-0.70	–	ns	19, 43	
LOAD MODE REGISTER command cycle time	t_{MRD}	10	–	ns		
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	$t_{HP} - t_{QHS}$	–	ns	26, 27	
Data hold skew factor	t_{QHS}	–	0.50	ns		
ACTIVE-to-READ with auto precharge command	t_{RAP}	15	–	ns		
ACTIVE-to-PRECHARGE command	t_{RAS}	40	70,000	ns	36	
ACTIVE-to-ACTIVE/AUTO REFRESH command period	t_{RC}	55	–	ns		
ACTIVE-to-READ or WRITE delay	t_{RCD}	15	–	ns		
REFRESH-to-REFRESH command interval	t_{REFC}	–	70.3	μs	24	
Average periodic refresh interval	t_{REFI}	–	7.8	μs	24	
AUTO REFRESH command period	t_{RFC}	70	–	ns	50	
PRECHARGE command period	t_{RP}	15	–	ns		
DQS read preamble	t_{RPRE}	0.9	1.1	t_{CK}	44	
DQS read postamble	t_{RPST}	0.4	0.6	t_{CK}	44	
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	10	–	ns		
Terminating voltage delay to VDD	t_{VTD}	0	–	ns		
DQS write preamble	t_{WPRE}	0.25	–	t_{CK}		
DQS write preamble setup time	t_{WPRES}	0	–	ns	21, 22	
DQS write postamble	t_{WPST}	0.4	0.6	t_{CK}	20	
Write recovery time	t_{WR}	15	–	ns		
Internal WRITE-to-READ command delay	t_{WTR}	2	–	t_{CK}		