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DDR2 SDRAM

MT47H256M4 – 32 Meg x 4 x 8 banks
MT47H128M8 – 16 Meg x 8 x 8 banks
MT47H64M16 – 8 Meg x 16 x 8 banks

For the latest data sheet, refer to Micron's Web site: http://www.micron.com/ddr2

Features

- RoHS compliant
- V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Supports JEDEC clock jitter specification

Options

Options	Marking
• Configuration	
256 Meg x 4 (32 Meg x 4 x 8 banks)	256M4
128 Meg x 8 (16 Meg x 8 x 8 banks)	128M8
64 Meg x 16 (8 Meg x 16 x 8 banks)	64M16
• FBGA package (lead-free)	
92-ball FBGA (11mm x 19mm) (:A)	BT
84-ball FBGA (10mm x 16.5mm) (:D)	B7
68-ball FBGA (10mm x 16.5mm) (:D)	B7
• Timing – cycle time	
5.0ns @ CL = 3 (DDR2-400)	-5E
3.75ns @ CL = 4 (DDR2-533)	-37E
3.0ns @ CL = 5 (DDR2-667)	-3
3.0ns @ CL = 4 (DDR2-667)	-3E
2.5ns @ CL = 6 (DDR2-800)	-25
2.5ns @ CL = 5 (DDR2-800)	-25E
• Self refresh	
Standard	None
Low-power	L
• Operating temperature	
Commercial (0°C ≤ T_C ≤ 85°C)	None
Industrial (–40°C ≤ T_C ≤ 95°C; –40°C ≤ T_A ≤ 85°C)	IT
• Revision	:A/:D

Table 1: Configuration Addressing

Architecture	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 4 x 8 banks	8 Meg x 16 x 8 banks
Refresh Count	8K	8K	8K
Row Addr.	16K (A0–A13)	16K (A0–A13)	8K (A0–A12)
Bank Addr.	8 (BA0–BA2)	8 (BA0–BA2)	8 (BA0–BA2)
Column Addr.	2K (A0–A9, A11)	1K (A0–A9)	1K (A0–A9)

Table 2: Key Timing Parameters

Speed Grade	Data Rate (MHz)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6			
-5E	400	400	N/A	N/A	15	15	55
-37E	400	533	N/A	N/A	15	15	55
-3	400	533	667	N/A	15	15	55
-3E	N/A	667	667	N/A	12	12	54
-25	N/A	N/A	667	800	15	15	55
-25E	N/A	533	800	N/A	12.5	12.5	55

Note: CL = CAS latency.

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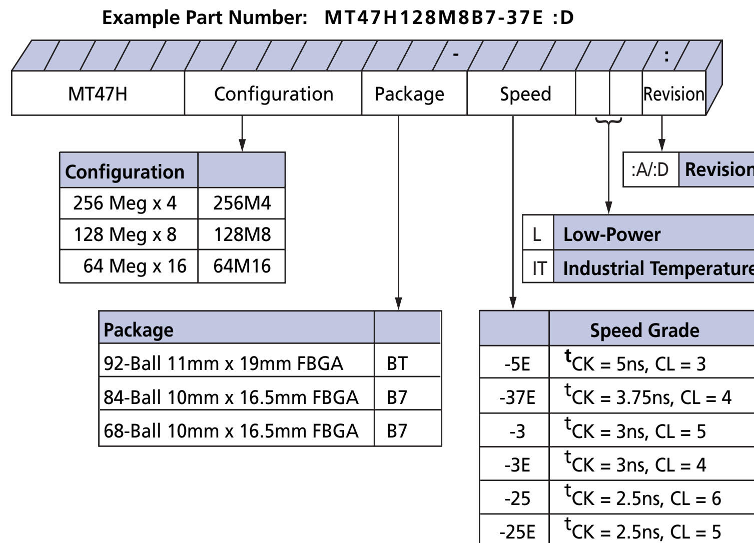
Part Numbers

Figure 1: 1Gb DDR2 Part Numbers



Note: Not all speeds and configurations are available. Contact Micron sales for current revision.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA Part Marking Decoder is available at www.micron.com/decoder.

General Description

The 1Gb DDR2 SDRAM is a high-speed CMOS, dynamic random access memory containing 1,073,741,824 bits. It is internally configured as an 8-bank DRAM. The functional block diagrams of the all device configurations are shown in "Functional Description" on page 18. Ball assignments and signal descriptions are shown in "Ball Assignment and Description" on page 9.

The 1Gb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 1Gb DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

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The 1Gb DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Industrial Temperature

The industrial temperature (IT) device has two simultaneous requirements: ambient temperature surrounding the device cannot exceed –40°C or +85°C, and the case temperature cannot exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when the T_C is < 0°C or > 85°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes, the lower byte and upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

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Ball Assignment and Description

Figure 2: 84-Ball FBGA (x16)
10mm x 16.5mm (top view)

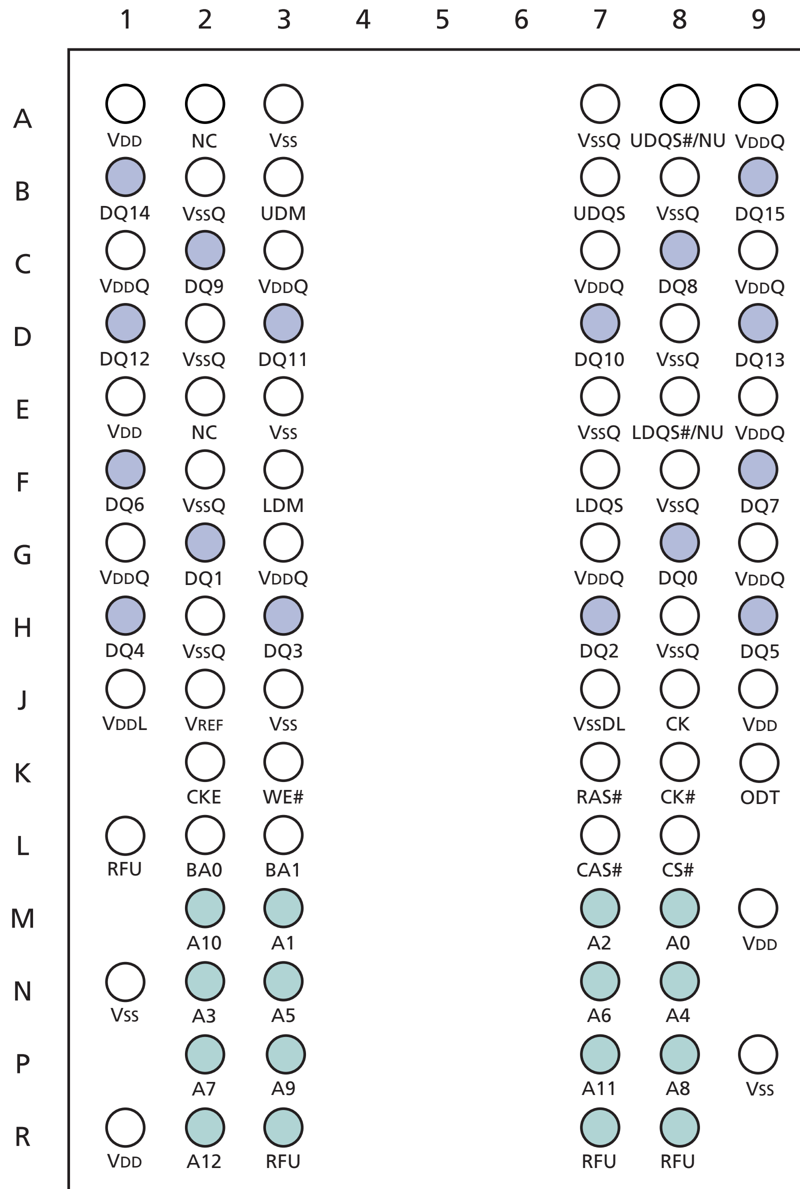

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Figure 3: 68-Ball FBGA (x4, x8)
10mm x 16.5mm (top view)

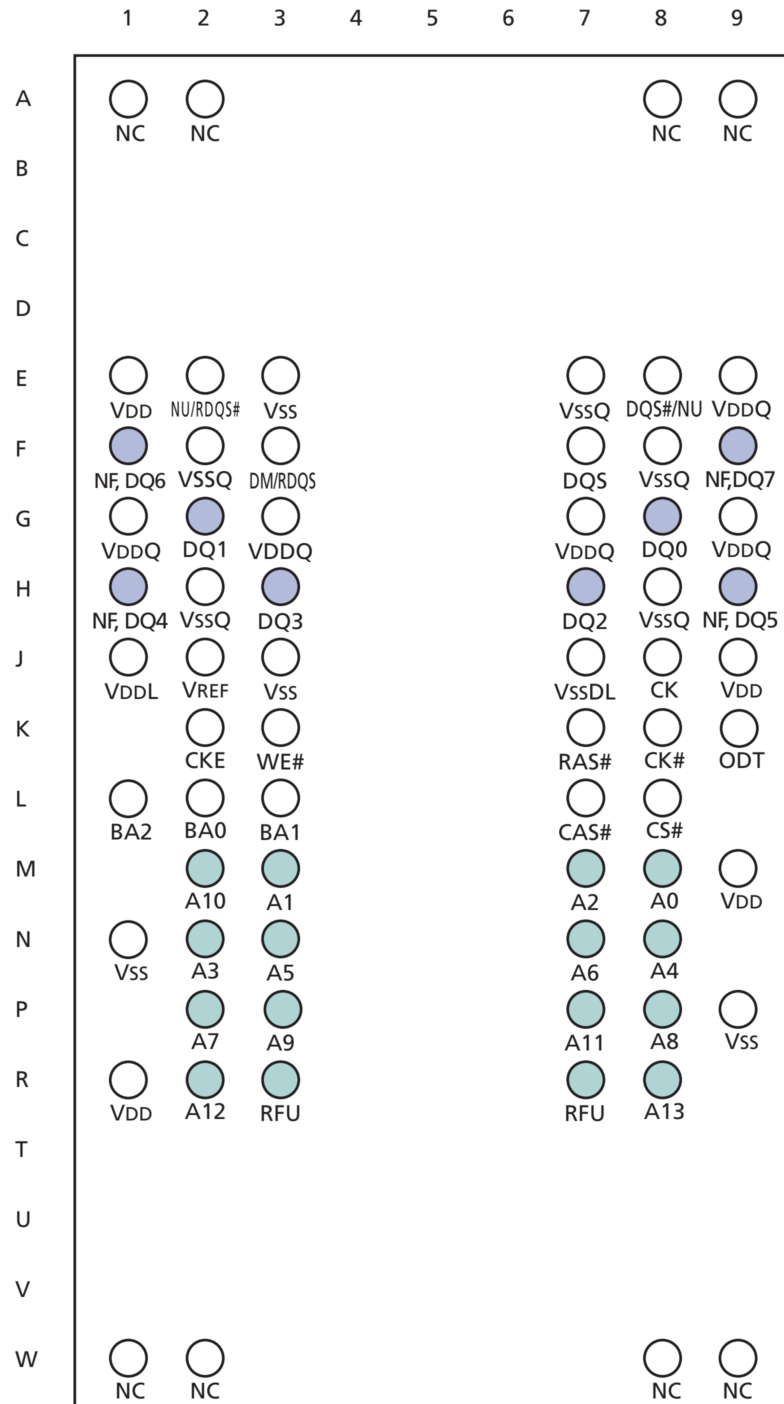

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Table 3: 84-/68-Ball Descriptions – 256 Meg x 4, 128 Meg x 8, 64 Meg x 16

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
K9	K9	ODT	Input	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
J8, K8	J8, K8	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
K2	K2	CKE	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down mode and SELF REFRESH operation (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for self refresh entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation, V_{REF} must be maintained.
L8	L8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
K7, L7, K3	K7, L7, K3	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F3, B3	F3	LDM, UDM (DM)	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is concurrently sampled HIGH during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
L2, L3, L1	L2, L3, L1	BA0–BA2	Input	Bank address inputs: BA0–BA2 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
M8, M3, M7, N2, N8, N3, N7, P2, P8, P3, M2, P7, R2	M8, M3, M7, N2, N8, N3, N7, P2, P8, P3, M2, P7, R2 R8	A0–A2, A3–A5, A6–A7, A8–A10, A11–A12 A13 (x4, x8)	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA2–BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.

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Table 3: 84-/68-Ball Descriptions – 256 Meg x 4, 128 Meg x 8, 64 Meg x 16 (Continued)

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
G8, G2, H7, H3, H1, H9, F1, F9, C8, C2, D7, D3, D1, D9, B1, B9	–	DQ0–DQ3, DQ4–DQ7, DQ8–DQ10, DQ11–DQ13, DQ14–DQ15	I/O	Data input/output: Bidirectional data bus for 64 Meg x 16.
–	G8, G2, H7, H3, H1, H9, F1, F9	DQ0–DQ3 DQ4–DQ7	I/O	Data input/output: Bidirectional data bus for 128 Meg x 8.
–	G8, G2, H7, H3	DQ0–DQ2 DQ3	I/O	Data input/output: Bidirectional data bus for 256 Meg x 4.
B7 A8	–	UDQS, UDQS#	I/O	Data strobe for upper byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
F7 E8	–	LDQS, LDQS#	I/O	Data strobe for lower byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	F7, E8	DQS, DQS#	I/O	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	F3, E2	RDQS, RDQS#	Output	Redundant data strobe for 128 Meg x 8 only. RDQS is enabled/ disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball F3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled *and* differential data strobe mode is enabled.
A1, E1, J9, M9, R1	E1, J9, M9, R1	VDD	Supply	Power supply: 1.8V ±0.1V.
J1	J1	VDDL	Supply	DLL power supply: 1.8V ±0.1V.
A9, C1, C3, C7, C9, E9, G1, G3, G7, G9	E9, G1, G3, G7, G9	VDDQ	Supply	DQ power supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity.
J2	J2	VREF	Supply	SSTL_18 reference voltage.
A3, E3, J3, N1, P9	J3, E3, N1, P9	VSS	Supply	Ground.
J7	J7	VSSDL	Supply	DLL ground. Isolated on the device from VSS and VSSQ.
A7, B2, B8, D2, D8, E7, F2, F8, H2, H8	E7, F2, F8, H2, H8	VSSQ	Supply	DQ ground. Isolated on the device for improved noise immunity.
A2, E2	W1, W2, W8, W9, A1, A2, A8, A9	NC	–	No connect: These balls should be left unconnected.
A8, E8	–	NU	–	Not used: Not used only on x16. If EMR[E10] = 0, A8 and E8 are UDQS# and LDQS#. If EMR[E10] = 1, then A8 and E8 are not used.
–	E2, E8	NU	–	Not used: Not used only on x8. If EMR[E10] = 0, E2 and E8 are RDQS# and DQS#. If EMR[E10] = 1, then E2 and E8 are not used.
–	F1, F9, H1, H9, E2	NF	–	Not funtion: Not used only on x4. These are data lines on the x8.
R8, R3, R7	R3, R7	RFU	–	Reserved for future use: Row address bits A14 (R3) and A13 (R8).

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Figure 4: 92-Ball FBGA (x16)
11mm x 19mm top (view)

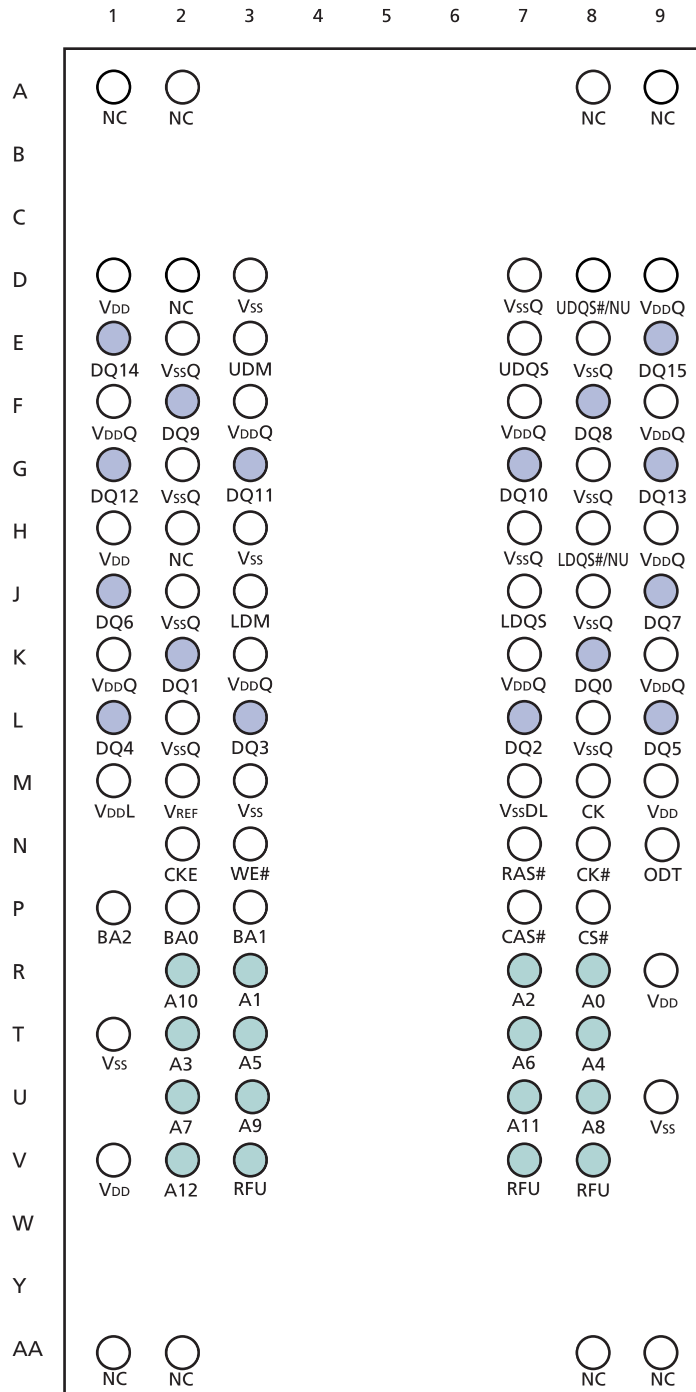

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Figure 5: 92-Ball FBGA (x4/x8)
11mm x 19mm top (view)

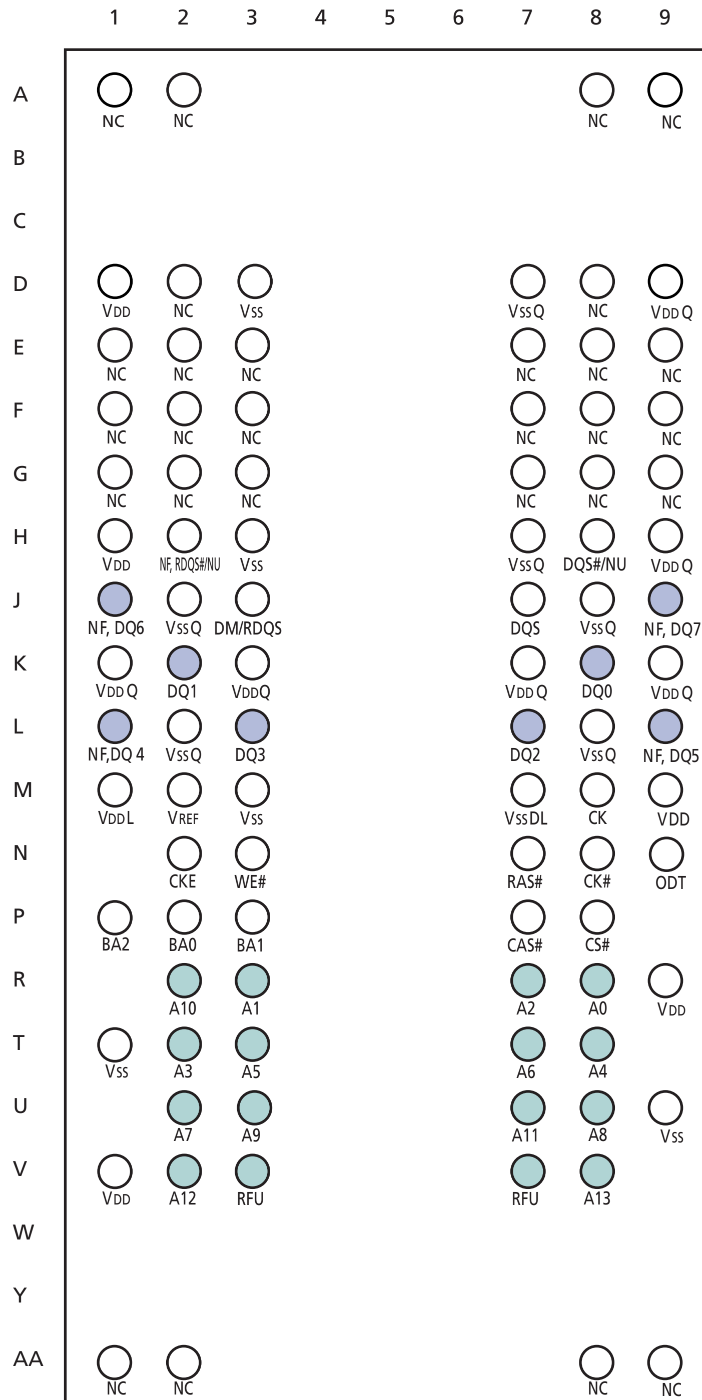

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Table 4: 92-Ball Descriptions – 256 Meg x 4, 128 Meg x 8, 64 Meg x 16

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
N9	N9	ODT	Input	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
M8, N8	M8, N8	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
N2	N2	CKE	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down mode and SELF REFRESH operation (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and self refresh entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation, V_{REF} must be maintained.
P8	P8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
N7, P7, N3	N7, P7, N3	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
J3, E3	J3	LDM, UDM, (DM)	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is concurrently sampled HIGH during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
P2, P3, P1	P2, P3, P1	BA0–BA2	Input	Bank address inputs: BA0–BA2 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
R8, R3, R7, T2, T8, T3, T7, U2, U8, U3, R2, U7, V2	–	A0–A2, A3–A6, A7–A9, A10–A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA2–BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.

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Table 4: 92-Ball Descriptions – 256 Meg x 4, 128 Meg x 8, 64 Meg x 16

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
–	R8, R3, R7, T2, T8, T3, T7, U2, U8, U3, R2, U7, V2, V8	A0–A3, A4–A7, A8–A10, A11–A13	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/ WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA2–BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
K8, K2, L7, L3, L1, L9, J1, J9, F8, F2, G7, G3, G1, G9, E1, E9	–	DQ0–DQ3, DQ4–DQ7, DQ8–DQ10, DQ11–DQ13, DQ14–DQ15	I/O	Data input/output: Bidirectional data bus for 64 Meg x 16.
–	K8, K2, L7, L3, L1, L9, J1, J9	DQ0–DQ3, DQ4–DQ7	I/O	Data input/output: Bidirectional data bus for 128 Meg x 8.
–	K8, K2, L7, L3	DQ0–DQ3	I/O	Data input/output: Bidirectional data bus for 256 Meg x 4.
E7, D8	–	UDQS, UDQS#	I/O	Data strobe for upper byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
J7, H8	–	LDQS, LDQS#	I/O	Data strobe for lower byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	J7, H8	DQS, DQS#	I/O	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	J3, H2	RDQS, RDQS#	Output	Redundant data strobe for 128 Meg x 8 only. RDQS is enabled/ disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball J3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled *and* differential data strobe mode is enabled.
D1, H1, M9, R9, V1	D1, H1, M9, R9, V1	V_{DD}	Supply	Power Supply: 1.8V ±0.1V.
M1	M1	V_{DDL}	Supply	DLL Power supply: 1.8V ±0.1V.
D9, F1, F3, F7, F9, H9, K1, K3, K7, K9	D9, H9, K1, K3, K7, K9	V_{DDQ}	Supply	DQ Power supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity.
M2	M2	V_{REF}	Supply	SSTL_18 reference voltage.
D3, H3, M3, T1, U9	D3, H3, M3, T1, U9	V_{SS}	Supply	Ground.
M7	M7	V_{SSDL}	Supply	DLL ground: Isolated on the device from V_{SS} and V_{SSQ}.
D7, E2, E8, G2, G8, H7, J2, J8, L2, L8	D7, H7,J 2, J8, L2, L8	V_{SSQ}	Supply	DQ ground: Isolated on the device for improved noise immunity.

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Table 4: 92-Ball Descriptions – 256 Meg x 4, 128 Meg x 8, 64 Meg x 16

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
A1, A2, A8, A9 D2, H2, AA1, AA2, AA8, AA9	A1, A2, A8, A9, D2, D8, E1–E3, E7–E9, F1–F3, F7–F9, G1–G3, G7–G9, AA1, AA2, AA8, AA9	NC	–	No connect: These balls should be left unconnected.
–	J1, J9, L1, L9, H2,	NF	–	No function: These balls are used as DQ4–DQ7 on the 128 Meg x8 , but are NF (no function) on the 256 Meg x 4 configuration.
D8, H8	–	NU	–	Not used: Not used only on x16. If EMR[E10] = 0, D8 and H8 are UDQS# and LDQS#. If EMR[E10] = 1, then D8 and H8 are not used.
–	H2, H8	NU	–	Not used: Not used only on x8. If EMR[E10] = 0, H2 and H8 are RDQS# and DQS#. If EMR[E10] = 1, then H2 and H8 are not used.
V3, V7, V8	V3, V7	RFU	–	Reserved for future use: Row address bits A13 (V8), A14(V3), and A15(V7) are reserved.

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Functional Description

The 1Gb DDR2 SDRAM is a high-speed CMOS dynamic random access memory containing 1,073,741,824 bits. The 1Gb DDR2 SDRAM is internally configured as an 8-bank DRAM.

The 1Gb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The DDR2 architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 1Gb DDR2 SDRAM consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit- wide, one-half-clock-cycle data transfers at the I/O balls.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Figure 9 on page 20 shows a simplified state diagram to provide the basic command flow. It is not comprehensive and does not identify all timing requirements or possible command restrictions.

Figure 6: Functional Block Diagram – 64 Meg x 16

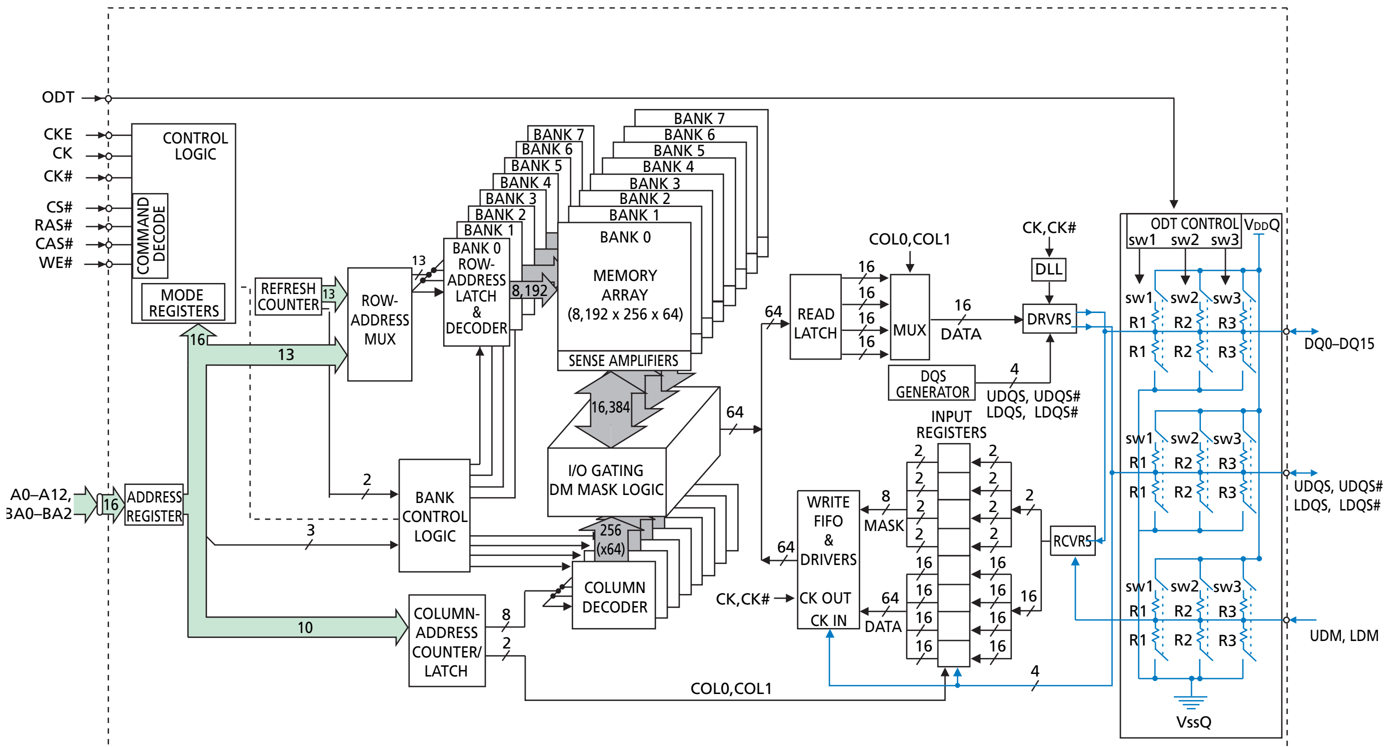

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Figure 7: Functional Block Diagram – 128 Meg x 8

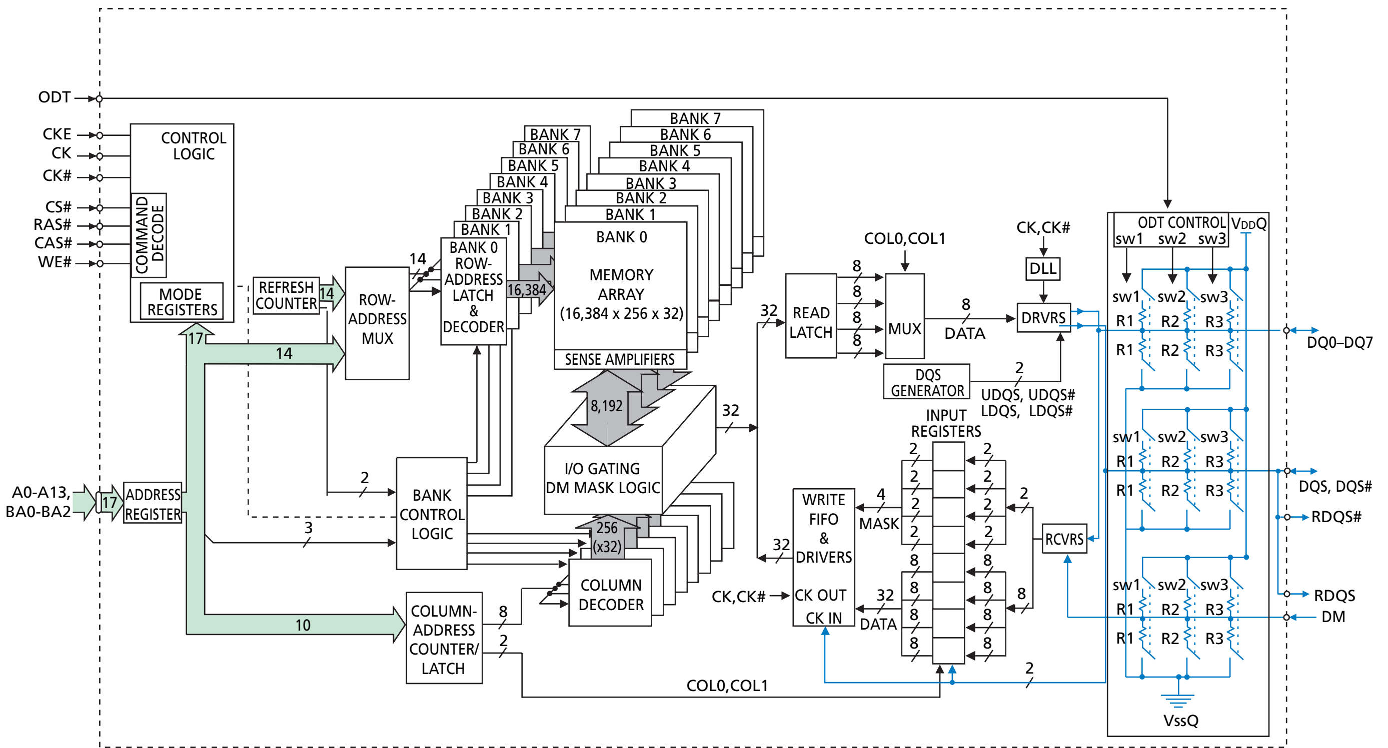
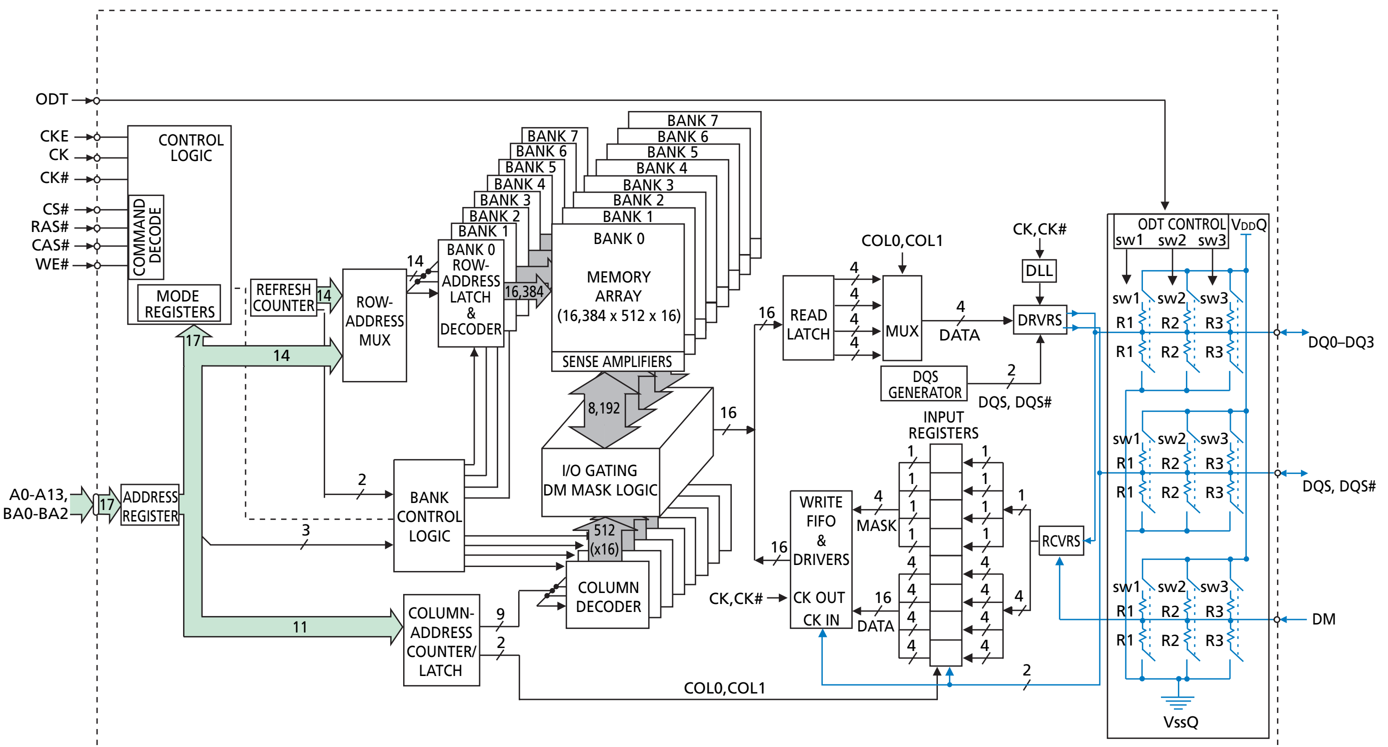


Figure 8: Functional Block Diagram – 256 Meg x 4



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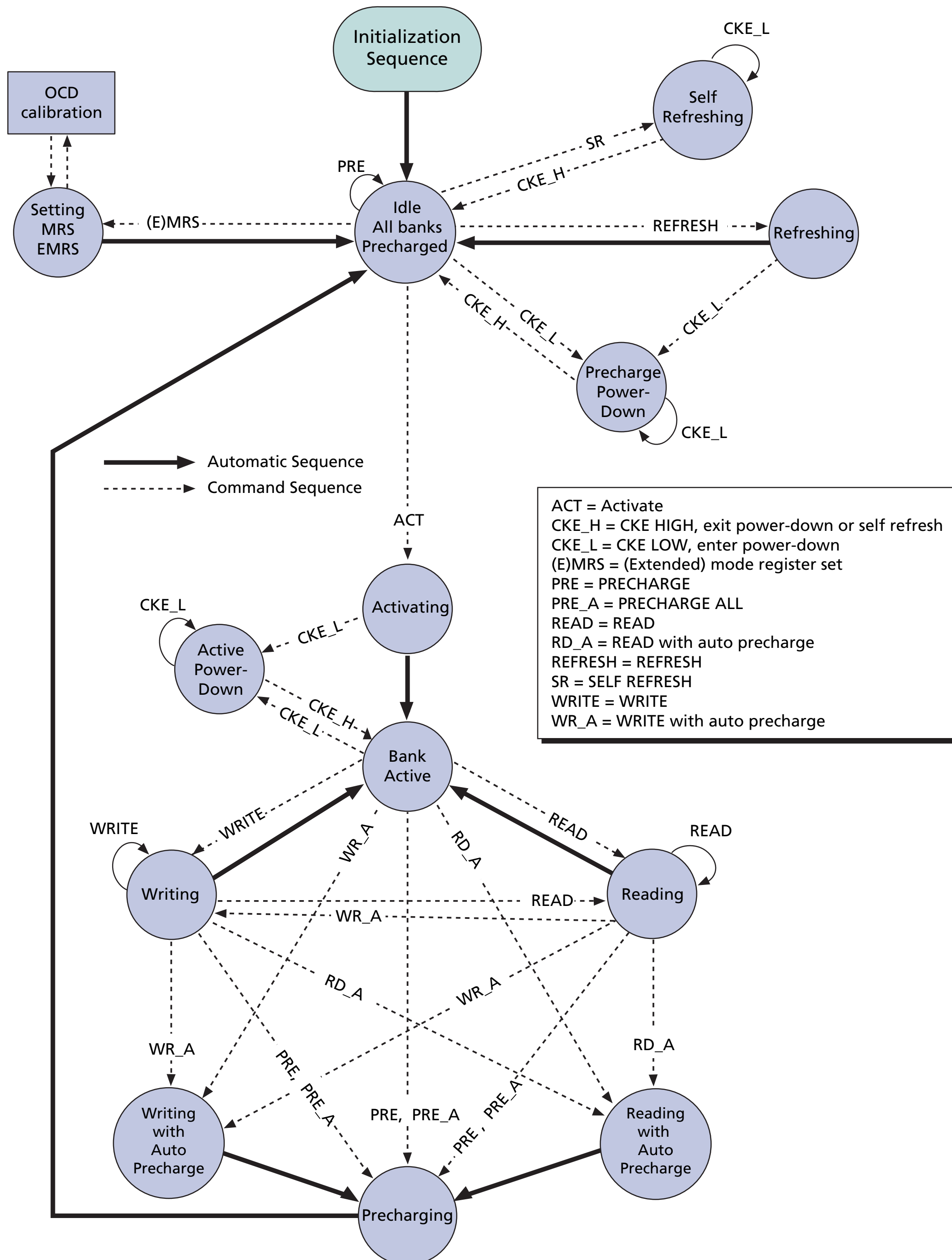
State Diagram

Figure 9 shows a simplified state diagram to provide the basic command flow. It is not comprehensive and does not identify all timing requirements or possible command restrictions.

Figure 9: Simplified State Diagram



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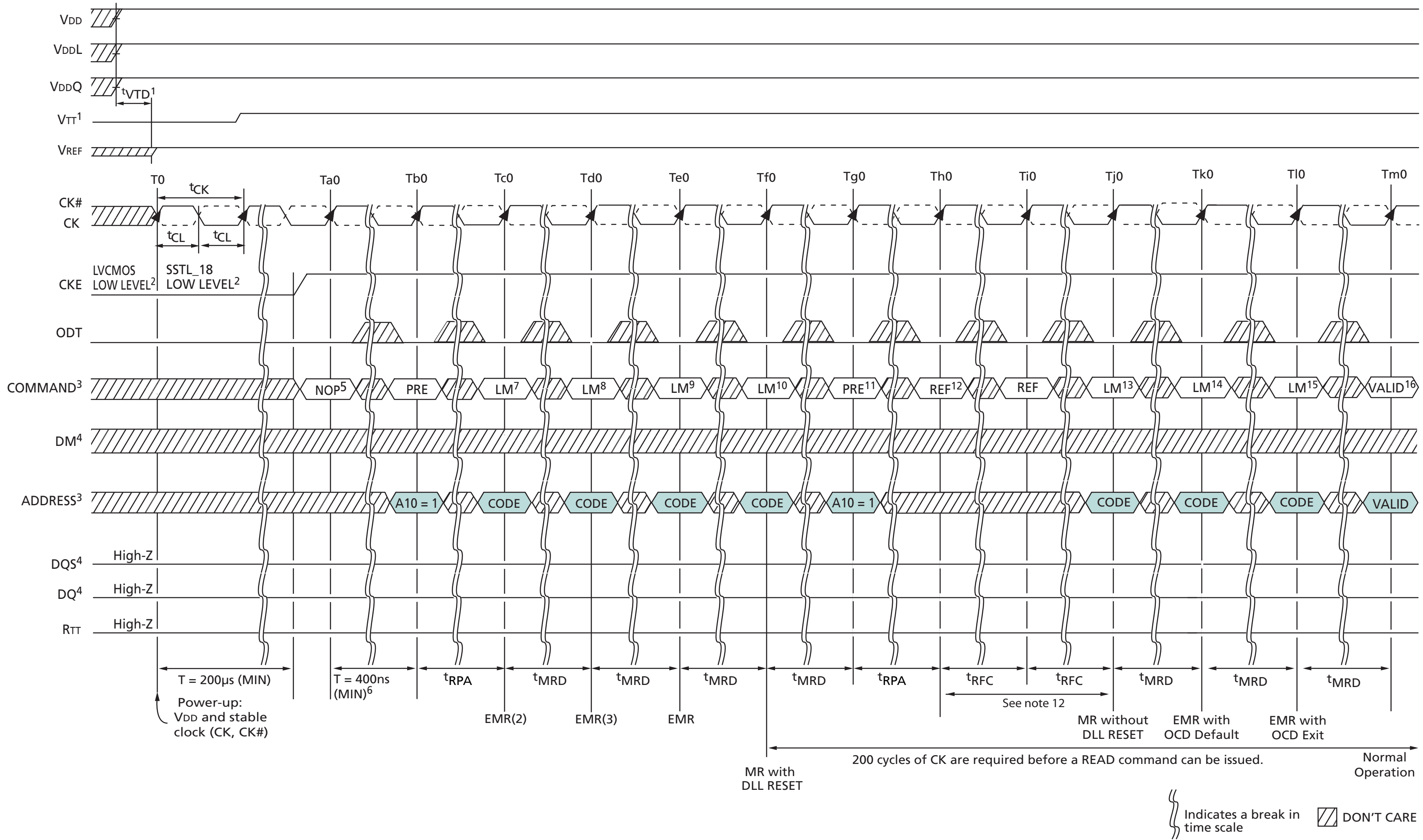
Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Figure 10 illustrates the sequence required for power-up and initialization.

Figure 10: DDR2 Power-up and Initialization

Notes appear on page 22



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Notes:

1. Applying power; if CKE is maintained below 0.2 x V_{DDQ}, outputs remain disabled. To guarantee R_{TT} (ODT resistance) is off, V_{REF} must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined; I/Os and outputs must be less than V_{DDQ} during voltage ramp time to avoid DDR2 SDRAM device latch-up). V_{TT} is not applied directly to the device; however, $^{t}V_{TT}$ should be ≥0 to avoid device latch-up. At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as V_{DD}, V_{DDL}, V_{DDQ}, V_{REF}, and V_{TT} are between their minimum and maximum values as stated in Table 20 on page 89):

   A. Single power source: The V_{DD} voltage ramp from 300mV to V_{DD} (MIN) must take no longer than 200ms; during the V_{DD} voltage ramp, $|V_{DD} - V_{DDQ}| \leq 0.3V$. Once supply voltage ramping is complete (when V_{DDQ} crosses V_{DD} [MIN]), Table 20 specifications apply.
      - V_{DD}, V_{DDL}, and V_{DDQ} are driven from a single power converter output
      - V_{TT} is limited to 0.95V MAX
      - V_{REF} tracks $V_{DDQ}/2$; V_{REF} must be within ±0.3V with respect to $V_{DDQ}/2$ during supply ramp time
      - $V_{DDQ} \geq V_{REF}$ at all times

   B. Multiple power sources: $V_{DD} \geq V_{DDL} \geq V_{DDQ}$ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (V_{DDQ} crosses V_{DD} [MIN]). Once supply voltage ramping is complete, Table 20 specifications apply.
      - Apply V_{DD} and V_{DDL} before or at the same time as V_{DDQ}; V_{DD}/V_{DDL} voltage ramp time must be ≤200ms from when V_{DD} ramps from 300mV to V_{DD} (MIN)
      - Apply V_{DDQ} before or at the same time as V_{TT}; the V_{DDQ} voltage ramp time from when V_{DD} (MIN) is achieved to when V_{DDQ} (MIN) is achieved must be ≤500ms; while V_{DD} is ramping, current can be supplied from V_{DD} through the device to V_{DDQ}
      - V_{REF} must track $V_{DDQ}/2$; V_{REF} must be within ±0.3V with respect to $V_{DDQ}/2$ during supply ramp time; $V_{DDQ} \geq V_{REF}$ must be met at all times
      - Apply V_{TT}; the V_{TT} voltage ramp time from when V_{DDQ} (MIN) is achieved to when V_{TT} (MIN) is achieved must be no greater than 500ms

2. CKE uses LVCMOS input levels prior to state T0 to ensure DQs are High-Z during device power-up prior to V_{REF} being stable. After state T0, CKE is required to have SSTL_18 input levels. Once CKE transitions to a high level, it must stay HIGH for the duration of the initialization sequence.
3. PRE = PRECHARGE command, LM = LOAD MODE command, MR = Mode Register, EMR = extended mode register, EMR2 = extended mode register 2, EMR3 = extended mode register 3, REF = REFRESH command, ACT = ACTIVE command, A10 = PRECHARGE ALL, CODE = desired values for mode registers (bank addresses are required to be decoded), VALID - any valid command/address, RA = row address, bank address.
4. DM represents DM for x4, x8 configurations and UDM, LDM for x16 configuration; DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16); DQ represents DQ0–DQ3 for x4, DQ–DQ7 for x8, and DQ0–DQ15 for x16.
5. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands, then take CKE HIGH.
6. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
7. Issue a LOAD MODE command to the EMR(2). (To issue an EMR(2) command, provide LOW to BA2 and BA0, and provide HIGH to BA1.) Set register E7 to "0" or "1;" all others must be "0."
8. Issue a LOAD MODE command to the EMR(3). (To issue an EMR(3) command, provide HIGH to BA0 =1, BA1 = 1, and BA2 = 0.) Set all registers to "0."
9. Issue a LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1, BA2, and A0; provide HIGH to BA0. Bits E7, E8, and E9 can be set to "0" or "1;" Micron recommends setting them to "0."
10. Issue a LOAD MODE command for DLL RESET. 200 cycles of clock input is required to lock the DLL. (To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA2 = BA1 = BA0 = 0.) CKE must be HIGH the entire time.
11. Issue PRECHARGE ALL command.
12. Issue two or more REFRESH commands.

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13. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL). To access the mode registers, BA0 = 0, BA1 = 0, BA2 = 0.
14. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters. To access the extended mode register, BA2 = 0, BA1 = 0, BA0 = 1.
15. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters. To access the extended mode registers, BA2 = 0, BA1 = 0, BA0 = 1.
16. The DDR2 SDRAM is now initialized and ready for normal operation 200 clock cycles after the DLL RESET at Tf0.

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Mode Register (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and power-down mode, as shown in Figure 11 on page 25. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M13 for x4 and x8 or M0–M12 for x16) must be programmed when the command is issued.

The MR is programmed via the LM command (bits BA2–BA0 = 0, 0, 0) and other bits (M13–M0 for x4 and x8, M12–M0 for x16) will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

Burst Length

Burst length is defined by bits M0–M3, as shown in Figure 11 on page 25. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when BL = 4 and by A3–A*i* when BL = 8 (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

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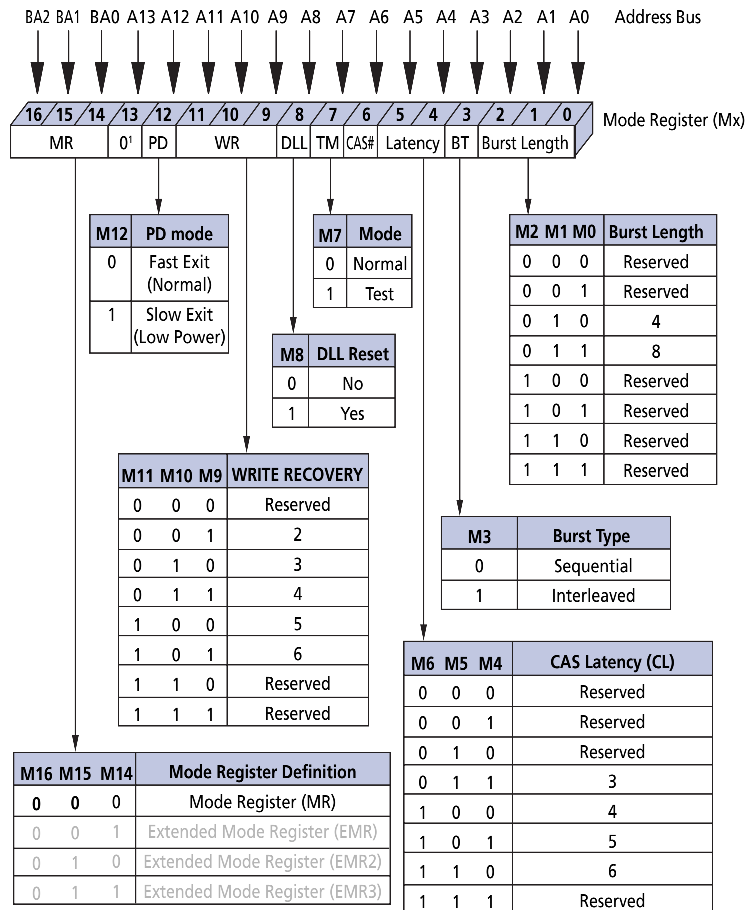
Figure 11: Mode Register (MR) Definition



Notes:
1. M13 (A13) is reserved for future use and must be programmed to "0." A13 is not used in x16 configuration.
2. Not all listed CL options are supported in any individual speed grade.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 11. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 5 on page 26. DDR2 SDRAM supports 4-bit burst mode and 8-bit burst mode only. For 8-bit burst mode, full, interleaved address ordering is supported; however, sequential address ordering is nibble-based.

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