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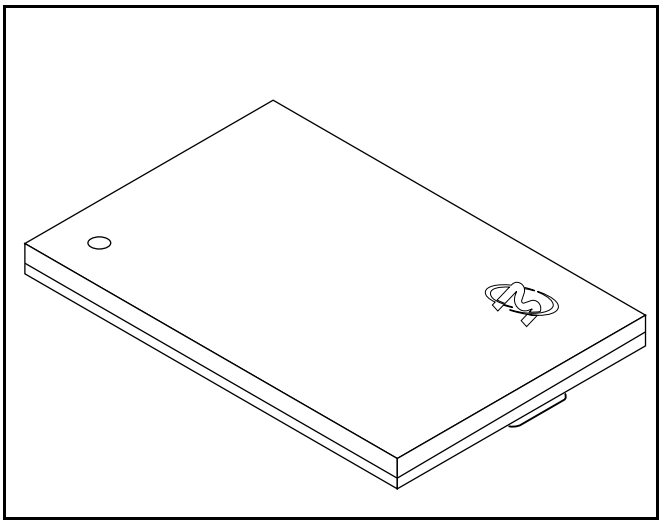
DDR2 SDRAM

MT47H128M4–32 MEG X 4 X 4 BANKS
MT47H64M8–16 MEG X 8 X 4 BANKS
MT47H32M16–8 MEG X 16 X 4 BANKS

For the latest data sheet, please refer to the Micron Web site: http://www.micron.com/datasheets

Features

- VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8 configuration
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Programmable CAS Latency (CL): 3 and 4
- Posted CAS additive latency (AL): 0, 1, 2, 3, and 4
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)



Options	Designation
• Configuration	
128 Meg x 4 (32 Meg x 4 x 4 banks)	128M4
64 Meg x 8 (16 Meg x 8 x 4 banks)	64M8
32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
• FBGA Package Lead-Free	
92-ball FBGA (11mm x 19mm)	BT
• Timing – Cycle Time	
5.0ns @ CL = 3 (DDR2-400)	-5E
3.75ns @ CL = 4 (DDR2-533)	-37E

ARCHITECTURE	128 MEG X 4	64 MEG X 8	32 MEG X 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh Count	8K	8K	8K
Row Addressing	16K (A0-A12)	16K (A0-A13)	8K (A0-A12)
Bank Addressing	4 (BA0 - BA1)	4 (BA0 - BA1)	4 (BA0 - BA1)
Column Addressing	2K (A0-A9, A11)	1K (A0-A9)	1K (A0-A9)

Table 1: Key Timing Parameters

SPEED GRADE	DATA RATE (MHz)		tRCD (ns)	tRP (ns)	tRC (ns)
	CL = 3	CL = 4			
-5E	400	400	15	15	55
-37E	400	533	15	15	60

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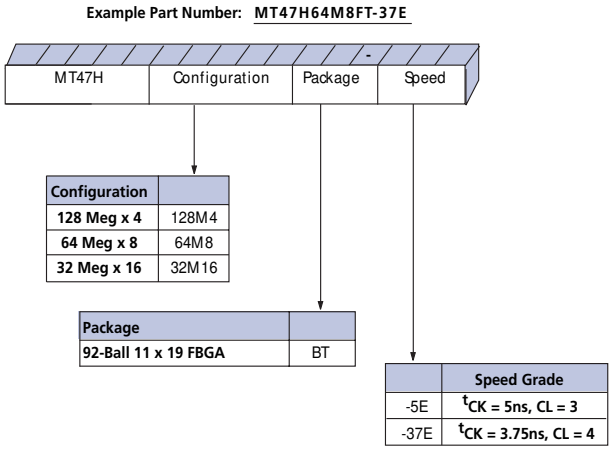
Part Numbers

Figure 1: 512Mb DDR2 Part Numbers



NOTE: Not all speeds and configurations are available.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's new FBGA Part Marking Decoder makes it easier to understand that part marking. Visit the web site at www.micron.com/decoder.

General Description

The 512Mb DDR2 SDRAM is a high-speed, CMOS dynamic random-access memory containing 5,368,709 bits. It is internally configured as a quad-bank DRAM. The functional block diagrams of the 32 Meg x 16, 64 Meg x 8, and 128 Meg x 4 devices, respectively are shown in the Functional Description section. Ball assignments for the 128 Meg x 4 are shown in Figure 2 and signal descriptions are shown in Table 1. Ball assignments for the 64 Meg x 8 and 128 Meg x 4 are shown in Figure 2 and signal descriptions are shown in Table 2.

The 512Mb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The 512Mb DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

NOTE: 1. The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.

2. Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ

collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ0 through DQ7) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8 through DQ15) DM refers to UDM and DQS refers to UDQS.

3. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
4. Any specific requirement takes precedence over a general statement.

Figure 2: 92-ball FBGA Ball Assignment (x16), 11mm x 19mm (Top View)

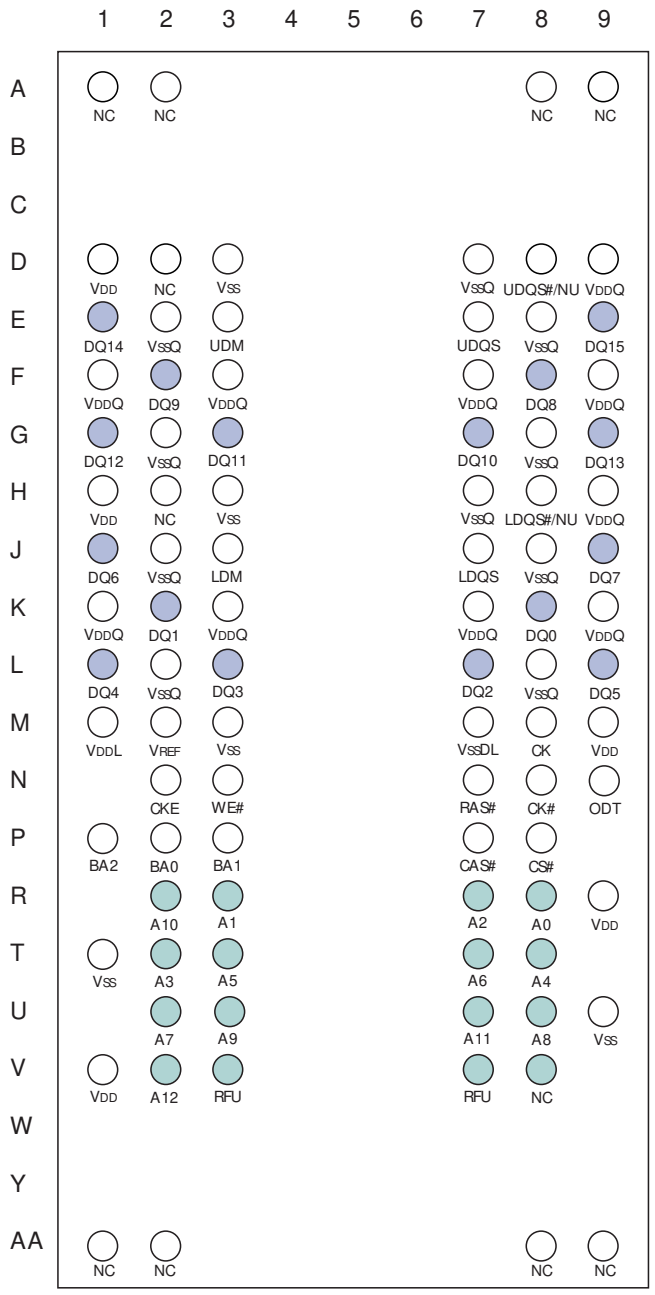


Figure 3: 92-Ball FBGA Ball Assignment (x 4, x 8), 11mm x 19mm (Top View)

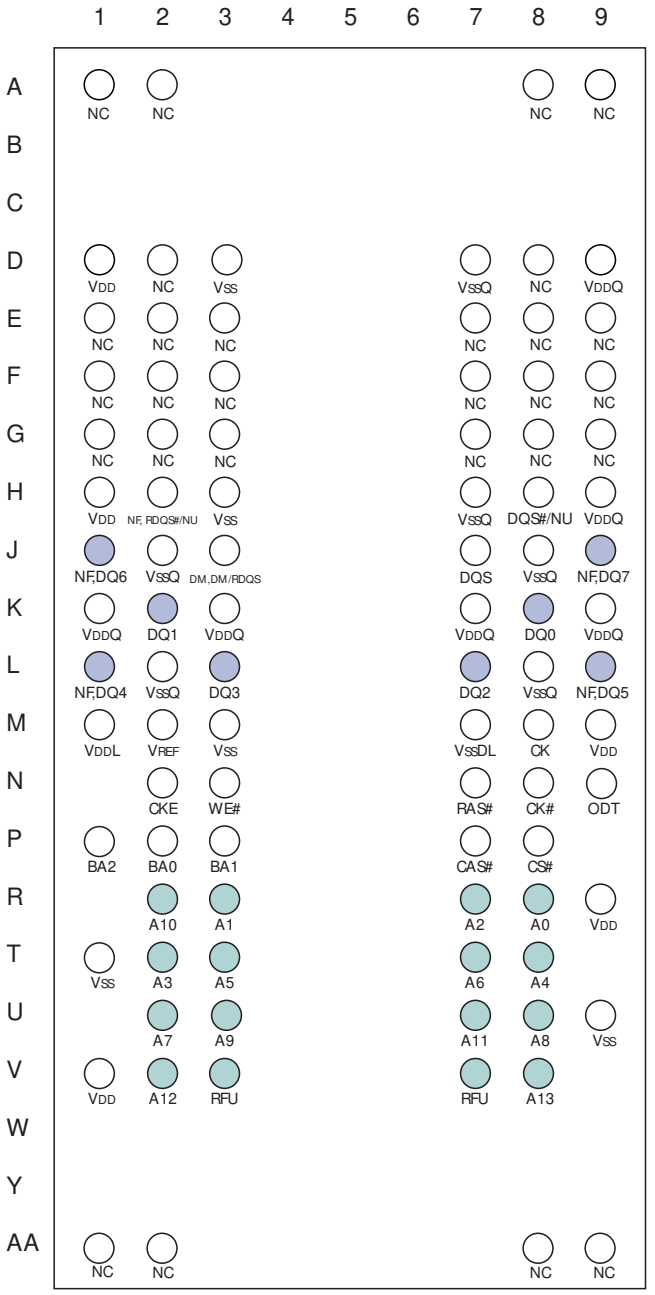


Table 2: FBGA Ball Descriptions 128 Meg x 4, 64 Meg x 8, 32 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
N9	N9	ODT	Input	On-Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0-DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0-DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
M8, N8	M8, N8	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
N2	N2	CKE	Input	Clock Enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry, POWER-DOWN exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation V_{REF} must be maintained.
P8	P8	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
N7, P7, N3	N7, P7, N3	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
J3, E3	J3	LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
P2, P3	P2, P3	BA0-BA1	Input	Bank Address Inputs: BA0-BA2 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0-BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.

Table 2: FBGA Ball Descriptions 128 Meg x 4, 64 Meg x 8, 32 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
R8,R3,R7,T2, T8,T3,T7,U2, U8,U3,R2,U7, V2	–	A0–A3 A4–A7 A8–A11 A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/ Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA1-BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
–	R8,R3,R7,T2, T8,T3,T7,U2, U8,U3,R2,U7, V2,V8	A0–A3 A4–A7 A8–A11 A12-A13	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/ Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA1-BA0) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
K8,K2,L7,L3, L1,L9,J1,J9, F8,F2,G7,G3, G1,G9,E1,E9	–	DQ0–DQ3 DQ4–DQ7 DQ8–DQ11 DQ12–DQ15	I/O	Data Input/Output: Bidirectional data bus for 32 Meg x 16.
–	K8,K2,L7,L3, L1,L9,J1,J9	DQ0–DQ3 DQ4–DQ7	I/O	Data Input/Output: Bidirectional data bus for 64 Meg x 8.
–	K8,K2,L7,L3	DQ0–DQ3	I/O	Data Input/Output: Bidirectional data bus for 128 Meg x 4.
E7,D8	–	UDQS, UDQS#	I/O	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
J7,H8	–	LDQS, LDQS#	I/O	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	J7,H8	DQS, DQS#	I/O	Data Strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	J3,H2	RDQS, RDQS#	Output	Redundant Data Strobe for 64 Meg x 8 only. RDQS is enabled/ disabled via the LOAD MODE command to the Extended Mode Register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, pin J3 becomes Data Mask (see DM pin). RDQS# is only used when RDQS is enabled AND differential data strobe mode is enabled.
D1,H1,M9,R9, V1	D1,H1,M9,R9, V1	V_{DD}	Supply	Power Supply: 1.8V ±0.1V.
M1	M1	V_{DDL}	Supply	DLL Power Supply: 1.8V ±0.1V.

Table 2: FBGA Ball Descriptions 128 Meg x 4, 64 Meg x 8, 32 Meg x 16

x16 FBGA BALL ASSIGNMENT	x4, x8 FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
D9,F1,F3,F7, F9,H9,K1,K3, K7,K9	D9,H9,K1, K3,K7,K9	V_{DDQ}	Supply	DQ Power Supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity.
M2	M2	V_{REF}	Supply	SSTL_18 reference voltage.
D3,H3,M3,T1, U9	D3,H3,M3,T1, U9	V_{SS}	Supply	Ground.
M7	M7	V_{SSDL}	Supply	DLL Ground. Isolated on the device from V_{SS} and V_{SSQ}.
D7,E2,E8,G2, G8,H7, J2,J8, L2,L8	D7,H7,J2, J8,L2,L8	V_{SSQ}	Supply	DQ Ground. Isolated on the device for improved noise immunity.
A1,A2,A8,A9 D2,H2,V8, AA1,AA2,AA8, AA9	A1,A2,A8,A9, D2,D8,E1-E3, E7-E9,F1-F3, F7-F9, G1-G3, G7-G9, AA1,AA2,AA8, AA9	NC	–	No Connect: These pins should be left unconnected.
–	J1, J9, L1, L9, H2,	NF	–	No Function: These pins are used as DQ4-DQ7 on the 64 Meg x 8, but are NF (No Function) on the 128 Meg x 4 configuration.
D8, H8	-	NU	–	x16 only Not Used: If EMR[E10] = 0, D8 and H8 are UDQS# and LDQS#. If EMR[E10] = 1, then D8 and H8 are Not Used.
-	H2, H8	NU	–	X8 only Not Used: If EMR[E10] = 0, H2 and H8 are RDQS# and DQS#. If EMR[E10] = 1, then H2 and H8 are Not Used.
V3, V7	V3, V7	RFU	–	Reserved for Future Use; Row address bits A14(V3) and A15(V7) are reserved for 2Gb and 4Gb densities.

Figure 4: Functional Description

The 512Mb DDR2 SDRAM is a high-speed, CMOS dynamic random-access memory containing 1,073,741,824 bits. The 512Mb DDR2 SDRAM is internally configured as a four-bank DRAM.

The 512Mb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The DDR2 architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR2 SDRAM consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Figure 5: Functional Block Diagram (32 Meg x 16)

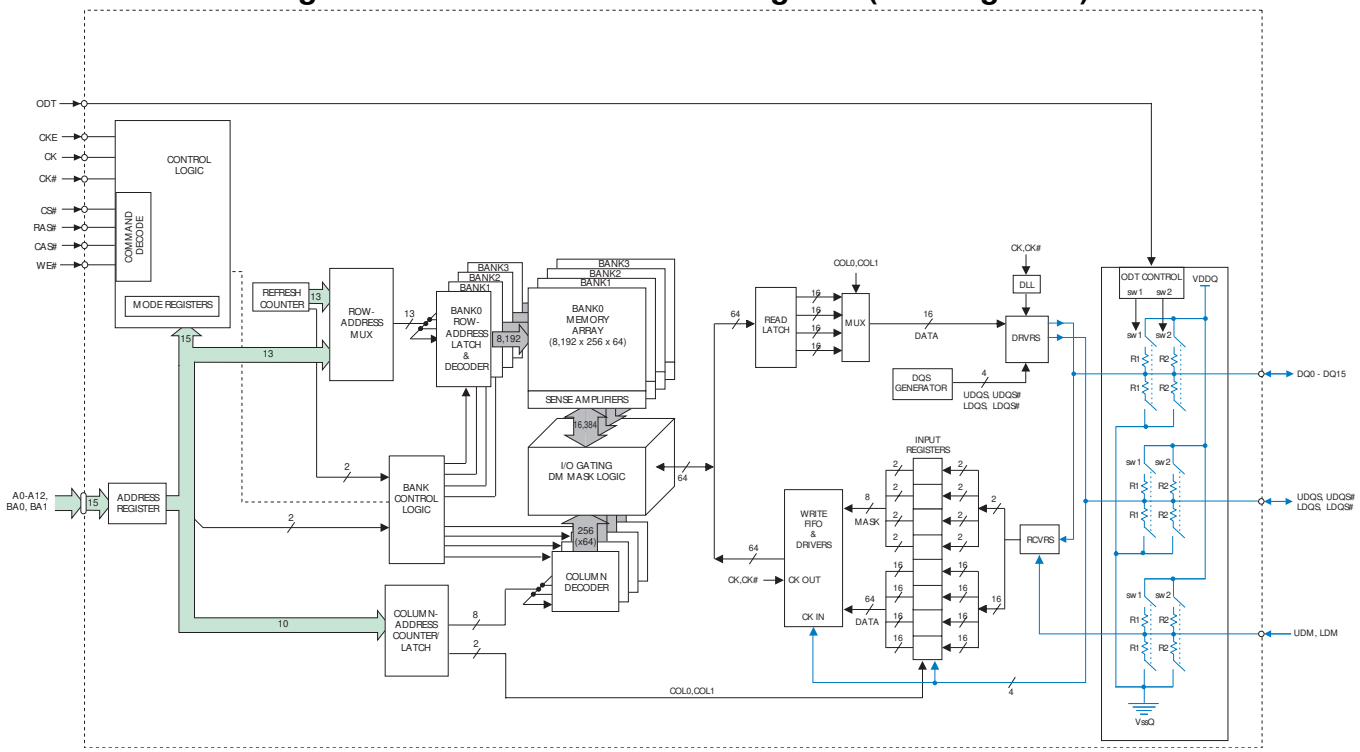


Figure 6: Functional Block Diagram (64 Meg x 8)

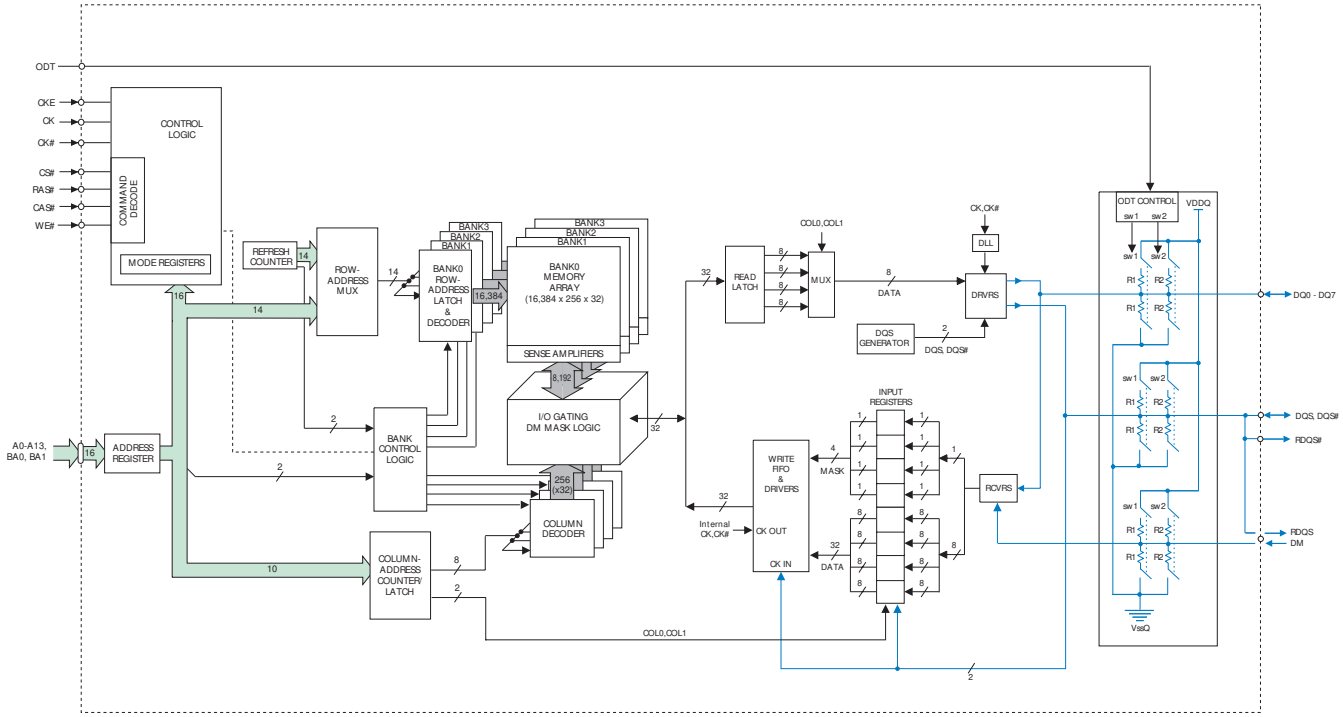
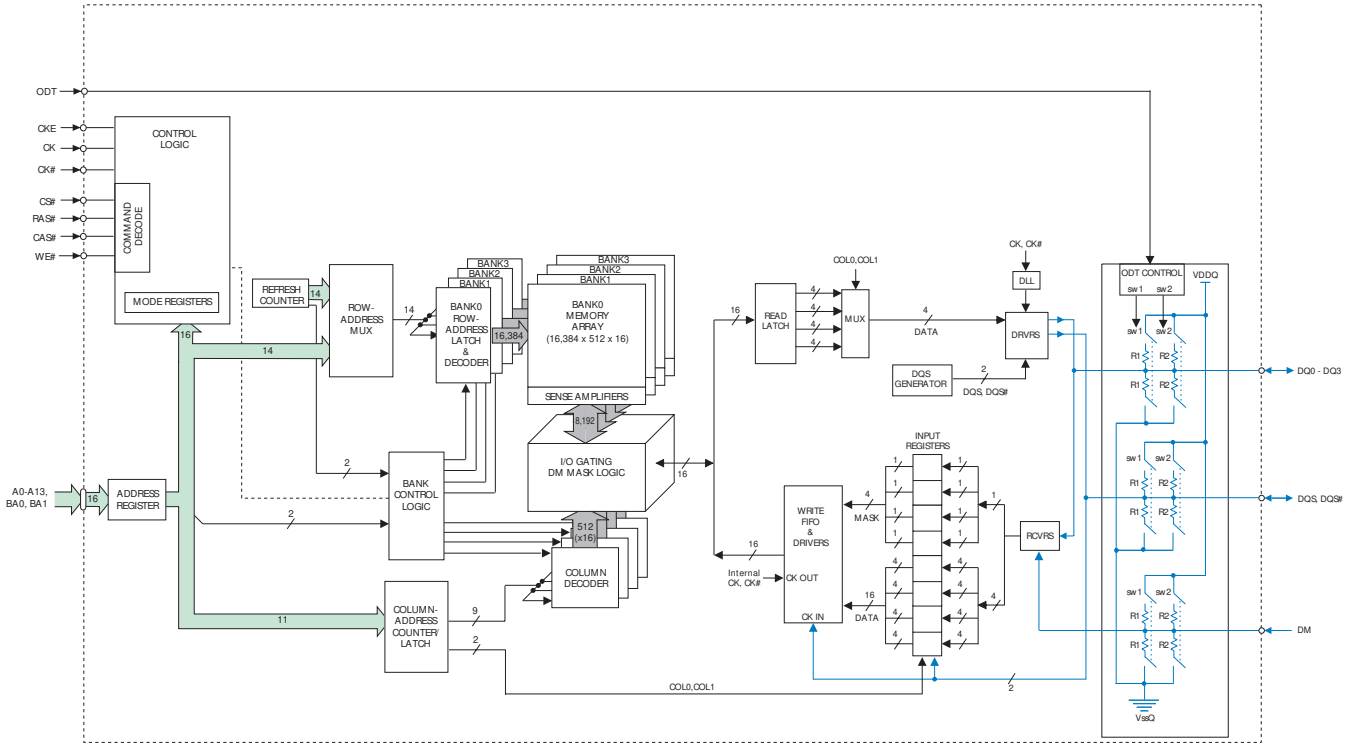


Figure 7: Functional Block Diagram (128 Meg x 4)



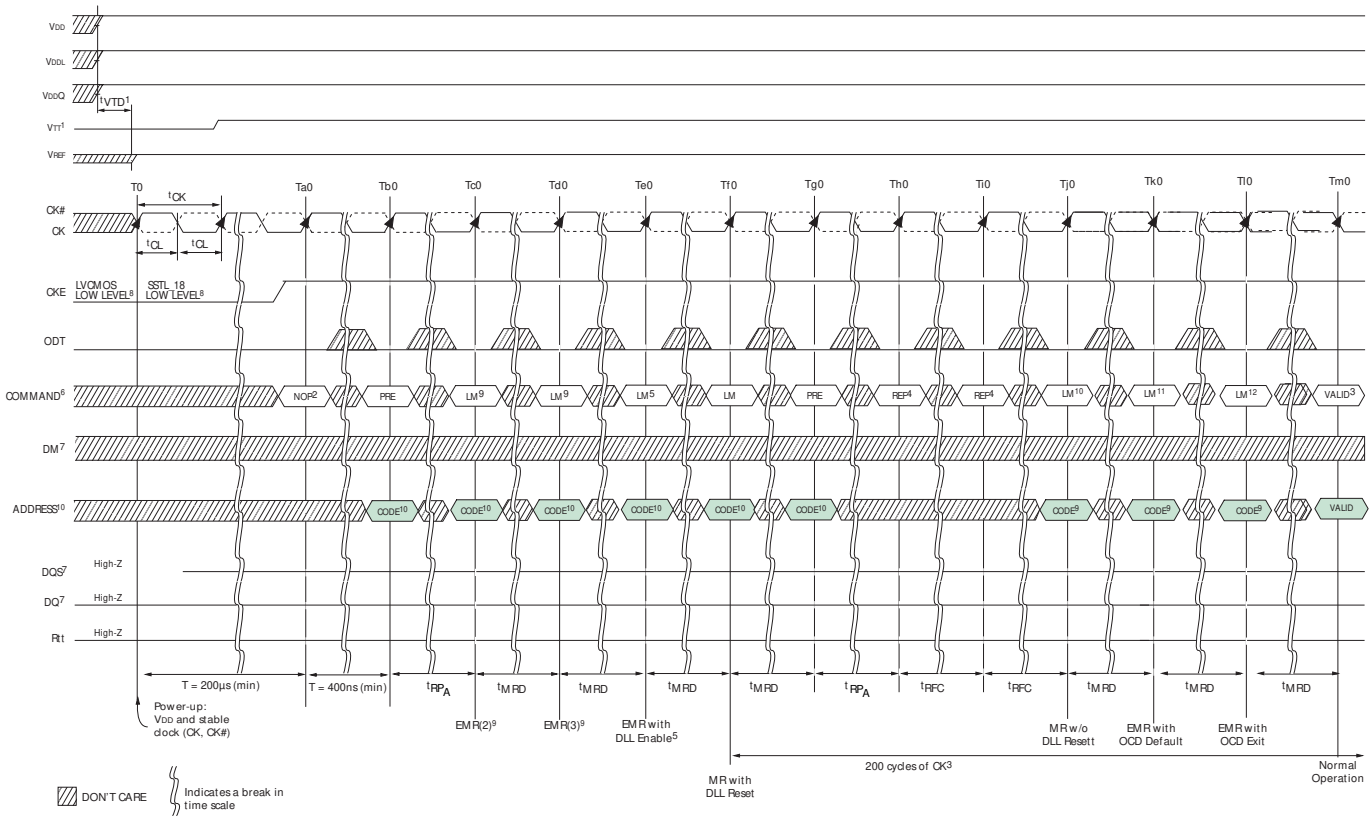
Initialization

The following sequence is required for power-up and initialization and is shown in Figure 8.

1. Apply power; if CKE is maintained below 0.2* $V_{DD}Q$, outputs remain disabled. To guarantee RTT (ODT Resistance) is off, V_{REF} must be valid and a low level must be applied to the ODT pin (all other inputs may be undefined). The time from when V_{DD} first starts to power-up to the completion of $V_{DD}Q$ must be equal to or less than 10ms. At least one of the following two sets of conditions (A or B) must be met:
   A. CONDITION SET A
   - V_{DD}, $V_{DD}L$ and $V_{DD}Q$ are driven from a single power converter output
   - V_{TT} is limited to 0.95V MAX
   - V_{REF} tracks $V_{DD}Q/2$.

   B. CONDITION SET B
   - Apply V_{DD} before or at the same time as $V_{DD}L$.
   - Apply $V_{DD}L$ before or at the same time as $V_{DD}Q$.
   - Apply $V_{DD}Q$ before or at the same time as V_{TT} and V_{REF}.
   - The voltage difference between any V_{DD} supply can not exceed 0.5V. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.
2. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
3. Issue an LOAD MODE command to the EMR(2) register. (To issue an EMR(2) command, provide LOW to BA0, provide HIGH to BA1.)
4. Issue a LOAD MODE command to the EMR(3) register. (To issue an EMR(3) command, provide HIGH to BA0 and BA1.)
5. Issue an LOAD MODE command to the EMR register to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0, provide HIGH to BA0. Bits E7, E8, and E9 must all be set to 0.
6. Issue a LOAD MODE command for DLL Reset. 200 cycles of clock input is required to lock the DLL. (To issue a DLL Reset, provide HIGH to A8 and provide LOW to BA1 and BA0.) CKE must be HIGH the entire time.
7. Issue PRECHARGE ALL command.
8. Issue two or more REFRESH commands.
9. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).
10. Issue a LOAD MODE command to the EMR to enable OCD default by setting Bits E7, E8, and E9 to 1 and set all other desired parameters.
11. Issue a LOAD MODE command to the EMR to enable OCD exit by setting Bits E7, E8, and E9 to 0 and set all other desired parameters.
12. The DDR2 SDRAM is now intialized and ready for normal operation 200 clocks after DLL Reset in step 6.

Figure 8: DDR2 Power-Up and Initialization



NOTE:

1. VTT is not applied directly to the device; however, tVTD should be greater than or equal to zero to avoid device latch-up. The time from when VDD first starts to power-up to the completion of VDDQ must be equal to or less than 10ms. One of the following two conditions (a or b) MUST be met:
   a) VDD, VDDL, and VDDQ are driven from a single power converter output.
   VTT may be 0.95V maximum during power up.
   VREF tracks VDDQ/2.
   b) Apply VDD before or at the same time as VDDL.
   Apply VDDL before or at the same time as VDDQ.
   Apply VDDQ before or at the same time as VTT and VREF. The voltage difference between any VDD supply can not exceed 0.5V.
2. Either a NOP or DESELECT command may be applied.
3. 200 cycles of clock (CK, CK#) are required before a READ command can be issued. CKE must be HIGH the entire time.
4. Two or more REFRESH commands are required.
5. Bits E7, E8, and E9 must all be set to 0 with all other operating parameters of EMRS set as required.
6. PRE = PRECHARGE command, LM = LOAD MODE command, REF = REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address.
7. DM represents DM for x4, x8 configuration and UDM, LDM for x16 configuration. DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16). DQ represents DQ0–DQ3 for x4, DQ0–DQ7 for x8, and DQ0–DQ15 for x16.
8. CKE pin uses LVCMOS input levels prior to state T0. After state T0, CKE pin uses SSTL_18 input levels.
9. ADDRESS represents A12-A0 for x4, x8, and A12-A0 for x16, BA0-BA1. A10 should be HIGH at states Tb0 and Tg0 to ensure a PRECHARGE (all banks) command is issued.
10. Bits E7, E8, and E9 must be set to 1 to set OCD default.
11. Bits E7, E8, and E9 must be set to 0 to set OCD exit and all other operating parameters of EMRS set as required.

Mode Register (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL reset, write recovery, and power-down mode as shown in Figure 9. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the LOAD MODE command is issued.

The mode register is programmed via the LM command (bits BA1-BA0 = 0, 0) and other bits (M13 - M0 for x4 and x8, M12 - M0 for x16) will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

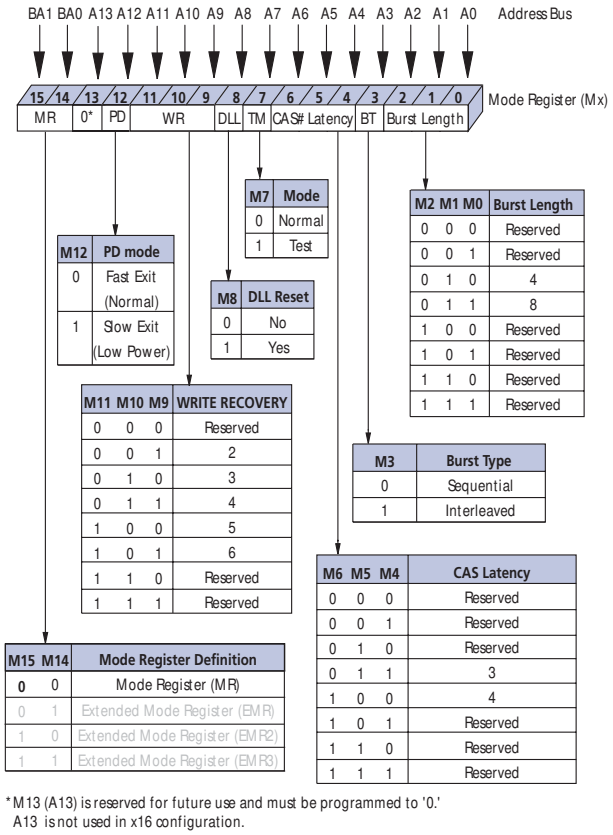
The LOAD MODE command can only be issued (or reissued) when all banks are in the precharged state. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

Burst Length

Burst length is defined by bits M0–M3 as shown in Figure 9. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when the burst length is set to four and by A3–A*i* when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Figure 9: Mode Register (MR) Definition



*M13 (A13) is reserved for future use and must be programmed to '0.'
A13 is not used in x16 configuration.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3 as shown in Figure 9. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address as shown in Table 3. DDR2 SDRAM supports 4-bit burst and 8-bit burst modes only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.

Table 3: Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS (A2, A1, A0)	ORDER OF ACCESSES WITHIN A BURST	
		BURST TYPE = SEQUENTIAL	BURST TYPE = INTERLEAVED
4	0 0 0	0,1,2,3	0,1,2,3
	0 0 1	1,2,3,0	1,0,3,2
	0 1 0	2,3,0,1	2,3,0,1
	0 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6
	0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5
	0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2
	1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1
	1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE command with bit M7 set to zero, and all other bits set to the desired values as shown in Figure 9. When bit M7 is '1,' no other bits of the mode register are programmed. Programming bit M7 to '1' places the DDR2 SDRAM into a test mode that is only used by the Manufacturer and should NOT be used. No operation or functionality is guaranteed if M7 bit is '1.'

DLL Reset

DLL reset is defined by bit M8 as shown in Figure 9. Programming bit M8 to '1' will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of '0' after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Write Recovery

Write recovery (WR) time is defined by bits M9–M11 as shown in Figure 9. The WR Register is used by the DDR2 SDRAM during WRITE with AUTO PRECHARGE operation. During WRITE with AUTO PRECHARGE operation, the DDR2 SDRAM delays the internal AUTO PRECHARGE operation by WR clocks (programmed in bits M9–M11) from the last data burst. An example of Write with AUTO PRECHARGE is shown in Figure 26 on page 30.

Write Recovery (WR) values of 2, 3, 4, 5, or 6 clocks may be used for programming bits M9–M11. The user is required to program the value of write recovery, which is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up a noninteger value to the next integer; WR [cycles] = ^{t}WR [ns] / ^{t}CK [ns]. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Power-Down Mode

Active power-down (PD) mode is defined by bit M12 as shown in Figure 9. PD mode allows the user to determine the active power-down mode, which determines performance vs. power savings. PD mode bit M12 does not apply to precharge power-down mode.

When bit M12 = 0, standard Active Power-down mode or 'fast-exit' active power-down mode is enabled. The ^{t}XARD parameter is used for 'fast-exit' active power-down exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower power active power-down mode or 'slow-exit' active power-down mode is enabled. The ^{t}XARDS parameter is used for 'slow-exit' active power-down exit timing. The DLL can be enabled, but 'frozen' during active power-down mode since the exit-to-READ command timing is relaxed. The power difference expected between PD 'normal' and PD 'low-power' mode is defined in the IDD table.

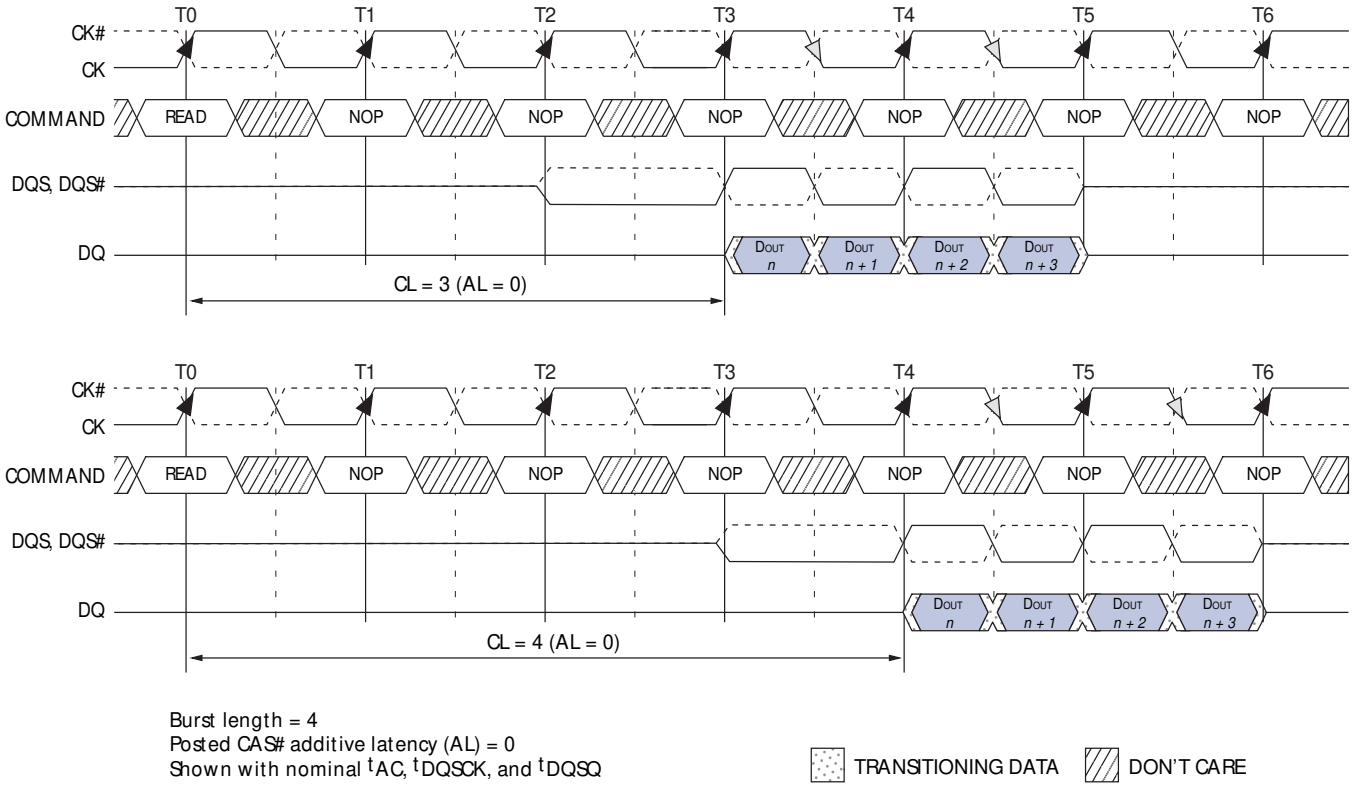
CAS Latency (CL)

The CAS Latency (CL) is defined by bits M4–M6 as shown in Figure 9. CAS Latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CAS Latency can be set to 3 or 4 clocks. CAS Latency of 2 or 5 clocks are JEDEC optional features and may be enabled in future speed grades. DDR2 SDRAM does not support any half clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DDR2 SDRAM also supports a feature called Posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD(MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks. The AL feature is described in more detail in the Extended Mode Register (EMR) and Operational sections.

Examples of CL = 3 and CL = 4 are shown in Figure 10; both assume AL = 0. If a READ command is registered at clock edge *n*, and the CAS Latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m* (this assumes AL = 0).

Figure 10: CAS Latency (CL)



Burst length = 4
Posted CAS# additive latency (AL) = 0
Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ

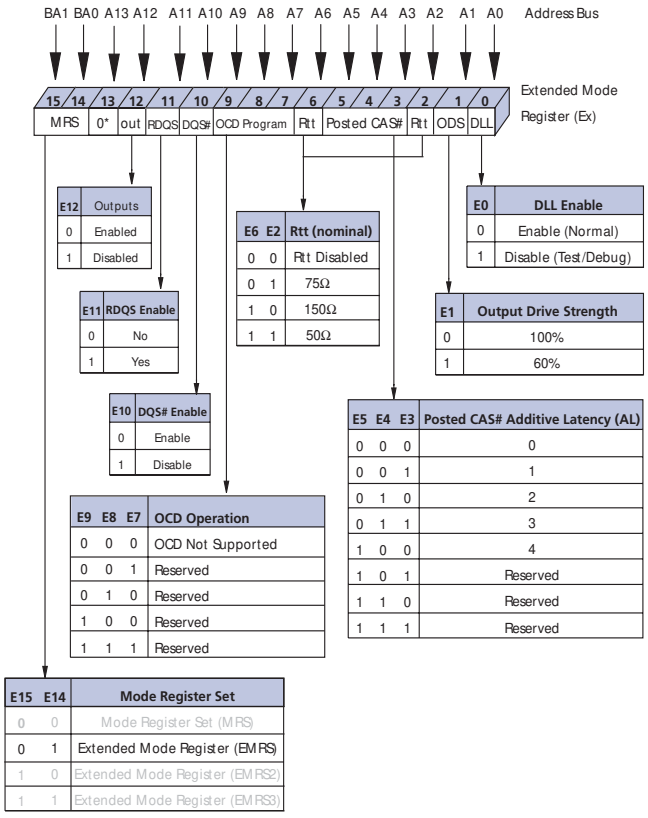
TRANSITIONING DATA DON'T CARE

Extended Mode Register (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT (RTT), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT disable/enable. These functions are controlled via the bits shown in Figure 11. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 11: Extended Mode Register Definition



*E13 (A13) is not used on the x16 configuration.

DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LOAD MODE command as shown in Figure 11. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using a LOAD MODE command.

The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled and reset upon exit of self refresh operation.

Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Output Drive Strength

The output drive strength is defined by bit E1 as shown in Figure 11. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (100 percent) drive strength for all outputs. Selecting a reduced drive strength option (bit E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of the lighter load and/or point-to-point environments.

DQS# Enable/Disable

The DQS# enable function is defined by bit E10. When enabled (bit E10 = 0), DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (bit E10 = 1), DQS is used in a single-ended mode and the DQS# pin is disabled. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

RDQS Enable/Disable

The RDQS enable function is defined by bit E11 as shown in Figure 11. This feature is only applicable to the x8 configuration. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the DDR2 SDRAM.

Output Enable/Disable

The OUTPUT enable function is defined by bit E12 as shown in Figure 11. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM outputs (DQs, DQS, DQS#, RDQS, RDQS#) are disabled removing output buffer current. The OUTPUT disable feature is intended to be used during IDD characterization of read current.

On Die Termination (ODT)

ODT effective resistance RTT(EFF) is defined by bits E2 and E6 of the EMR as shown in Figure 11. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. RTT effective resistance values of 75Ω and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signals. A functional representation of ODT is shown in block diagrams in "Functional Description" on page 13. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off 'sw1' or 'sw2'. The ODT effective resistance value is selected by enabling switch 'sw1,' which enables all 'R1' values that are 150Ω each, enabling an effective resistance of 75Ω (RTT1(EFF) = 'R1' / 2). Similarly, if 'sw2' is enabled, all 'R2' values that are 300Ω each, enable an effective ODT resistance of 150Ω (RTT2(EFF) = 'R2'/2). Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The ODT control pin is used to determine when RTT(EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input pin are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation. If SELF REFRESH operation is used, RTT(EFF) should *always* be disabled and the ODT input pin is disabled by the DDR2 SDRAM. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until the EMR command is issued to enable the ODT feature, at which point the ODT pin will determine the RTT(EFF) value. See "ODT Timing" on page 9 for ODT timing diagrams.

Off-Chip Driver (OCD) Impedance Calibration

The OCD function is no longer supported and must be set to the default state. See "Initialization" on page 15 to properly set OCD defaults.

Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL as shown in Figure 11. Bits E3–E5 allow the user to program the DDR2 SDRAM with a CAS# Additive latency of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD(MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1 x ^{t}CK. The READ or WRITE command is held for the time of the additive latency (AL) before it is issued internally to the DDR2 SDRAM device. READ Latency (RL) is controlled by the sum of the Posted CAS additive latency (AL) and CAS Latency (CL); RL = AL + CL. Write latency (WL) is equal to READ latency minus one clock; WL = AL + CL - 1 x ^{t}CK. An example of a READ latency is shown in Figure 12. An example of a WRITE latency is shown in Figure 13.

Figure 12: READ Latency

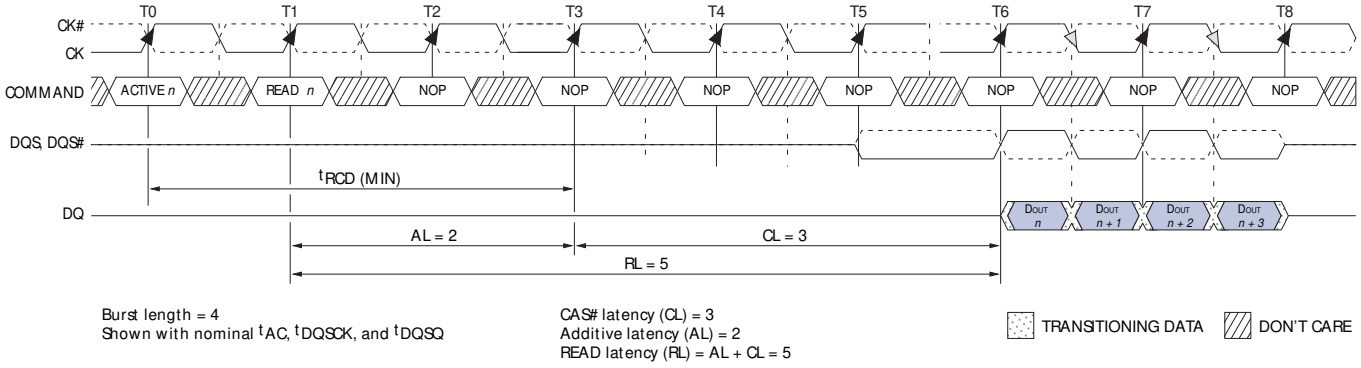
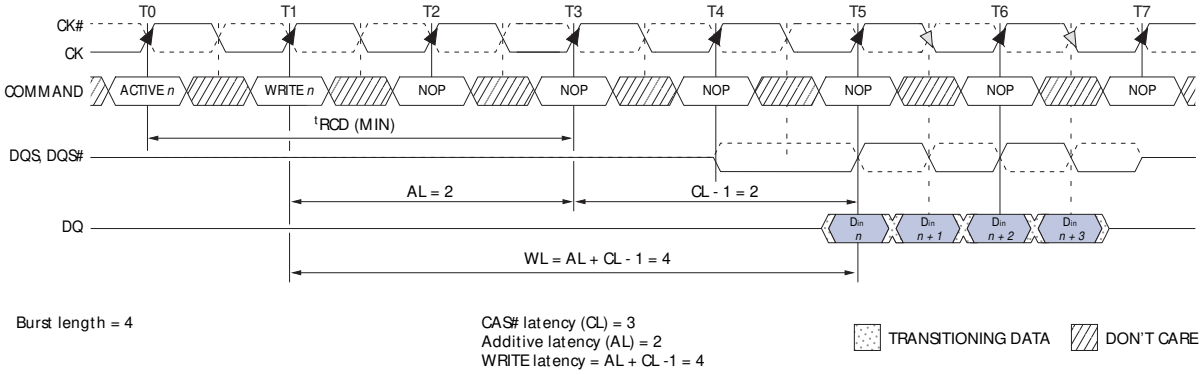


Figure 13: Write Latency

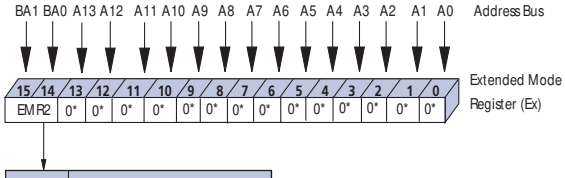


Extended Mode Register 2 (EMR2)

The Extended Mode Register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved as shown in Figure 14. The EMR2 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 14: Extended Mode Register 2 (EMR2) Definition



M15	M14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

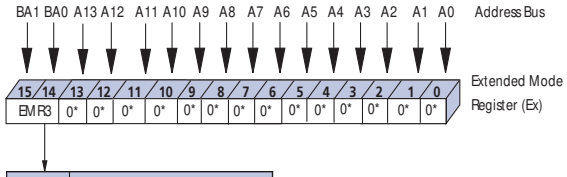
* E13 (A13) - E0 (A0) are reserved for future use and must all be programmed to '0'.
A13 is not used in x16 configuration.

Extended Mode Register 3 (EMR3)

The Extended Mode Register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved as shown in Figure 15. The EMR3 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 15: Extended Mode Register 3 (EMR3) Definition



M15	M14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

* E13 (A13) - E0 (A0) are reserved for future use and must all be programmed to '0'.
A13 is not used in x16 configuration.

Command Truth Tables

The following tables provide a quick reference of DDR2 SDRAM available commands, including CKE power-down modes, and bank-to-bank commands.

Table 4: Truth Table – DDR2 Commands

Notes: 1, 5, and 6 apply to the entire Table.

FUNCTION	CKE		CS#	RAS#	CAS#	WE#	BA1 BA0	A12 A11	A10	A9–A0	NOTES
	PREVIOUS CYCLE	CURRENT CYCLE									
Load Mode	H	H	L	L	L	L	BA	OP Code			2
Refresh	H	H	L	L	L	H	X	X	X	X	
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	2
ALL Banks Precharge	H	H	L	L	H	L	X	X	H	X	
Bank Activate	H	H	L	L	H	H	BA	Row Address			
Write	H	H	L	H	L	L	BA	Column Address	L	Column Address	2, 3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column Address	H	Column Address	2, 3
Read	H	H	L	H	L	H	BA	Column Address	L	Column Address	2, 3
Read with Auto Precharge	H	H	L	H	L	H	BA	Column Address	H	Column Address	2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Power-Down Entry	H	L	H	X	X	X	X	X	X	X	4
			L	H	H	H					
Power-Down Exit	L	H	H	X	X	X	X	X	X	X	4
			L	H	H	H					

NOTE:

1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
2. Bank addresses (BA) BA1-BA0 determine which bank is to be operated upon. BA during a Load Mode command selects which mode register is programmed.
3. Burst reads or writes at BL = 4 cannot be terminated or interrupted. See sections "Read Interrupted by a Read" and "Write Interrupted by a Write" for other restrictions and details.
4. The Power Down Mode does not perform any refresh operations. The duration of power-down is therefore limited by the refresh requirements outlined in the AC parametric section.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See the ODT section for details.
6. "X" means "H or L" (but a defined logic level).
7. Self refresh exit is asynchronous.

Table 5: Truth Table – Current State Bank *n* - Command to Bank *n*

Notes: 1–6; notes appear below and on next page.

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	REFRESH	7
	L	L	L	L	LOAD MODE	7
Row Active	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled	L	H	L	H	READ (select column and start new READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9, 11
	L	L	H	L	PRECHARGE (start precharge)	8
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	9, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (start precharge)	8, 10

NOTE:

1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH (see Table 5) and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^{t}RP has been met.

   Row Active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank, should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 5, and according to Table 6.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the idle state.

   Row Activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the "row active" state.

   Read with Auto Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

   Write with Auto Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an REFRESH command and ends when ^{t}RFC is met. Once ^{t}RFC is met, the DDR2 SDRAM will be in the all banks idle state.

   Accessing Mode Register: Starts with registration of a LOAD MODE command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the DDR2 SDRAM will be in the all banks idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.