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DDR2 SDRAM

MT47H128M4 – 32 Meg x 4 x 4 banks

MT47H64M8 – 16 Meg x 8 x 4 banks

MT47H32M16 – 8 Meg x 16 x 4 banks

Features

- Vdd = +1.8V ±0.1V, VddQ = +1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 4 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 t_{CK}
- Selectable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Automotive temperature (AT) option
- RoHS compliant
- Supports JEDEC clock jitter specification

Options¹

- | | |
|---|----------|
| • Configuration | |
| – 256 Meg x 4 (32 Meg x 4 x 4 banks) | 128M4 |
| – 128 Meg x 8 (16 Meg x 8 x 4 banks) | 64M8 |
| – 64 Meg x 16 (8 Meg x 16 x 4 banks) | 32M16 |
| • FBGA package (Pb-free) – x16 | |
| – 84-ball FBGA (12mm x 12.5mm) Rev. B | CC |
| – 84-ball FBGA (10mm x 12.5mm) Rev. D | BN |
| – 84-ball FBGA (8mm x 12.5mm) Rev. F | HR |
| • FBGA package (Pb-free) – x4, x8 | |
| – 60-ball FBGA (12mm x 10mm) Rev. B | CB |
| – 60-ball FBGA (10mm x 10mm) Rev. D | B6 |
| – 60-ball FBGA (8mm x 10mm) Rev. F | CF |
| • FBGA package (lead solder) – x16 | |
| – 84-ball FBGA (12mm x 12.5mm) Rev. B | GC |
| – 84-ball FBGA (10mm x 12.5mm) Rev. D | FN |
| – 84-ball FBGA (8mm x 12.5mm) Rev. F | HW |
| • FBGA package (lead solder) – x4, x8 | |
| – 60-ball FBGA (12mm x 10mm) Rev. B | GB |
| – 60-ball FBGA (10mm x 10mm) Rev. D | F6 |
| – 60-ball FBGA (8mm x 10mm) Rev. F | JN |
| • Timing – cycle time | |
| – 2.5ns @ CL = 5 (DDR2-800) | -25E |
| – 2.5ns @ CL = 6 (DDR2-800) | -25 |
| – 3.0ns @ CL = 4 (DDR2-667) | -3E |
| – 3.0ns @ CL = 5 (DDR2-667) | -3 |
| – 3.75ns @ CL = 4 (DDR2-533) | -37E |
| – 5.0ns @ CL = 3 (DDR2-400) | -5E |
| • Self refresh | |
| – Standard | None |
| – Low-power | L |
| • Operating temperature | |
| – Commercial (0°C ≤ T _C ≤ 85°C) | None |
| – Industrial (–40°C ≤ T _C ≤ 95°C;
–40°C ≤ T _A ≤ 85°C) | IT |
| – Automotive, Revision :D only
(–40°C ≤ T _C , T _A ≤ 105°C) | AT |
| • Revision | :B/:D/:F |

Note: 1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for product offerings and availability.

Table 1: Key Timing Parameters

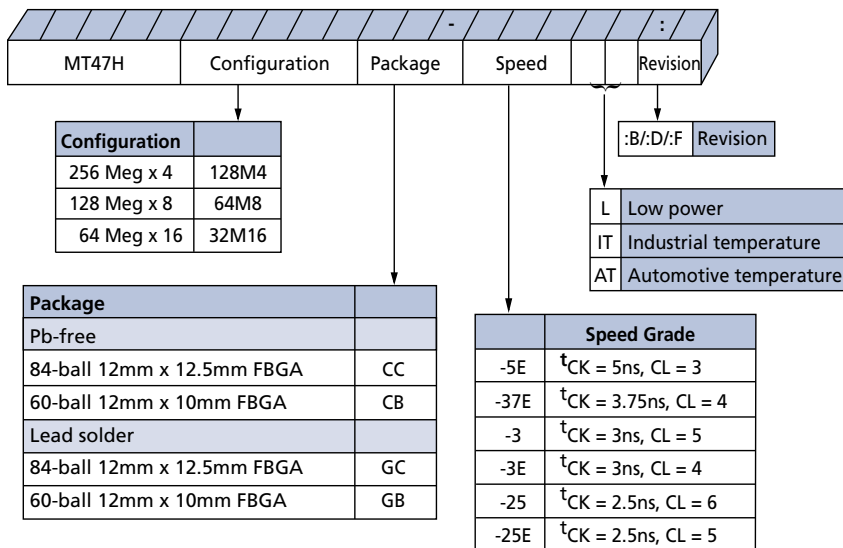
Speed Grade	Data Rate (MT/s)				t _{RC} (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	
-25E	400	533	800	800	55
-25	400	533	667	800	55
-3E	400	667	667	n/a	54
-3	400	533	667	n/a	55
-37E	400	533	n/a	n/a	55
-5E	400	400	n/a	n/a	55

Table 2: Addressing

Parameter	128 Meg x 4	64 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	A[13:0] (16K)	A[13:0] (16K)	A[12:0] (8K)
Bank address	BA[1:0] (4)	BA[1:0] (4)	BA[1:0] (4)
Column address	A[11, 9:0] (2K)	A[9:0] (1K)	A[9:0] (1K)

Figure 1: 512Mb DDR2 Part Numbers

Example Part Number: MT47H128M4B6-25E :D



Note: 1. Not all speeds and configurations are available in all packages.



FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: <http://www.micron.com>.

Contents

State Diagram	9
Functional Description	10
Industrial Temperature	10
Automotive Temperature	11
General Notes	11
Functional Block Diagrams	12
Ball Assignments and Descriptions	15
Packaging	20
Package Dimensions	20
FBGA Package Capacitance	26
Electrical Specifications – Absolute Ratings	27
Temperature and Thermal Impedance	27
Electrical Specifications – Idd Parameters	30
Idd Specifications and Conditions	30
Idd7 Conditions	31
AC Timing Operating Specifications	35
AC and DC Operating Conditions	46
ODT DC Electrical Characteristics	47
Input Electrical Characteristics and Operating Conditions	48
Output Electrical Characteristics and Operating Conditions	51
Output Driver Characteristics	53
Power and Ground Clamp Characteristics	57
AC Overshoot/Undershoot Specification	58
Input Slew Rate Derating	60
Commands	74
Truth Tables	74
DESELECT	78
NO OPERATION (NOP)	79
LOAD MODE (LM)	79
ACTIVATE	79
READ	79
WRITE	79
PRECHARGE	80
REFRESH	80
SELF REFRESH	80
Mode Register (MR)	80
Burst Length	81
Burst Type	81
Operating Mode	83
DLL RESET	83
Write Recovery	84
Power-Down Mode	84
CAS Latency (CL)	85
Extended Mode Register (EMR)	86
DLL Enable/Disable	87
Output Drive Strength	87
DQS# Enable/Disable	87
RDQS Enable/Disable	87
Output Enable/Disable	87
On-Die Termination (ODT)	88



Off-Chip Driver (OCD) Impedance Calibration 88
Posted CAS Additive Latency (AL) 88
Extended Mode Register 2 (EMR2) 90
Extended Mode Register 3 (EMR3) 91
Initialization 92
ACTIVATE 96
READ 98
 READ with Precharge 102
 READ with Auto Precharge 104
WRITE 109
PRECHARGE 119
REFRESH 120
SELF REFRESH 121
Power-Down Mode 123
Precharge Power-Down Clock Frequency Change 130
Reset 131
 CKE Low Anytime 131
ODT Timing 133
 MRS Command to ODT Update Delay 135

List of Tables

Table 1: Key Timing Parameters	2
Table 2: Addressing	2
Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions	17
Table 4: Input Capacitance	26
Table 5: Absolute Maximum DC Ratings	27
Table 6: Temperature Limits	28
Table 7: Thermal Impedance	29
Table 8: General Idd Parameters	30
Table 9: Idd7 Timing Patterns (4-Bank Interleave READ Operation)	31
Table 10: DDR2 Idd Specifications and Conditions	32
Table 11: AC Operating Specifications and Conditions	35
Table 12: Recommended DC Operating Conditions (SSTL_18)	46
Table 13: ODT DC Electrical Characteristics	47
Table 14: Input DC Logic Levels	48
Table 15: Input AC Logic Levels	48
Table 16: Differential Input Logic Levels	49
Table 17: Differential AC Output Parameters	51
Table 18: Output DC Current Drive	51
Table 19: Output Characteristics	52
Table 20: Full Strength Pull-Down Current (mA)	53
Table 21: Full Strength Pull-Up Current (mA)	54
Table 22: Reduced Strength Pull-Down Current (mA)	55
Table 23: Reduced Strength Pull-Up Current (mA)	56
Table 24: Input Clamp Characteristics	57
Table 25: Address and Control Balls	58
Table 26: Clock, Data, Strobe, and Mask Balls	58
Table 27: AC Input Test Conditions	59
Table 28: DDR2-400/533 Setup and Hold Time Derating Values (^t IS and ^t IH)	61
Table 29: DDR2-667/800/1066 Setup and Hold Time Derating Values (^t IS and ^t IH)	62
Table 30: DDR2-400/533 ^t DS, ^t DH Derating Values with Differential Strobe	65
Table 31: DDR2-667/800/1066 ^t DS, ^t DH Derating Values with Differential Strobe	67
Table 32: Single-Ended DQS Slew Rate Derating Values Using ^t DS _b and ^t DH _b	68
Table 33: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at Vref) at DDR2-667	68
Table 34: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at Vref) at DDR2-533	69
Table 35: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at Vref) at DDR2-400	69
Table 36: Truth Table – DDR2 Commands	74
Table 37: Truth Table – Current State Bank <i>n</i> – Command to Bank <i>n</i>	75
Table 38: Truth Table – Current State Bank <i>n</i> – Command to Bank <i>m</i>	77
Table 39: Minimum Delay with Auto Precharge Enabled	78
Table 40: Burst Definition	83
Table 41: READ Using Concurrent Auto Precharge	104
Table 42: WRITE Using Concurrent Auto Precharge	110
Table 43: Truth Table – CKE	125

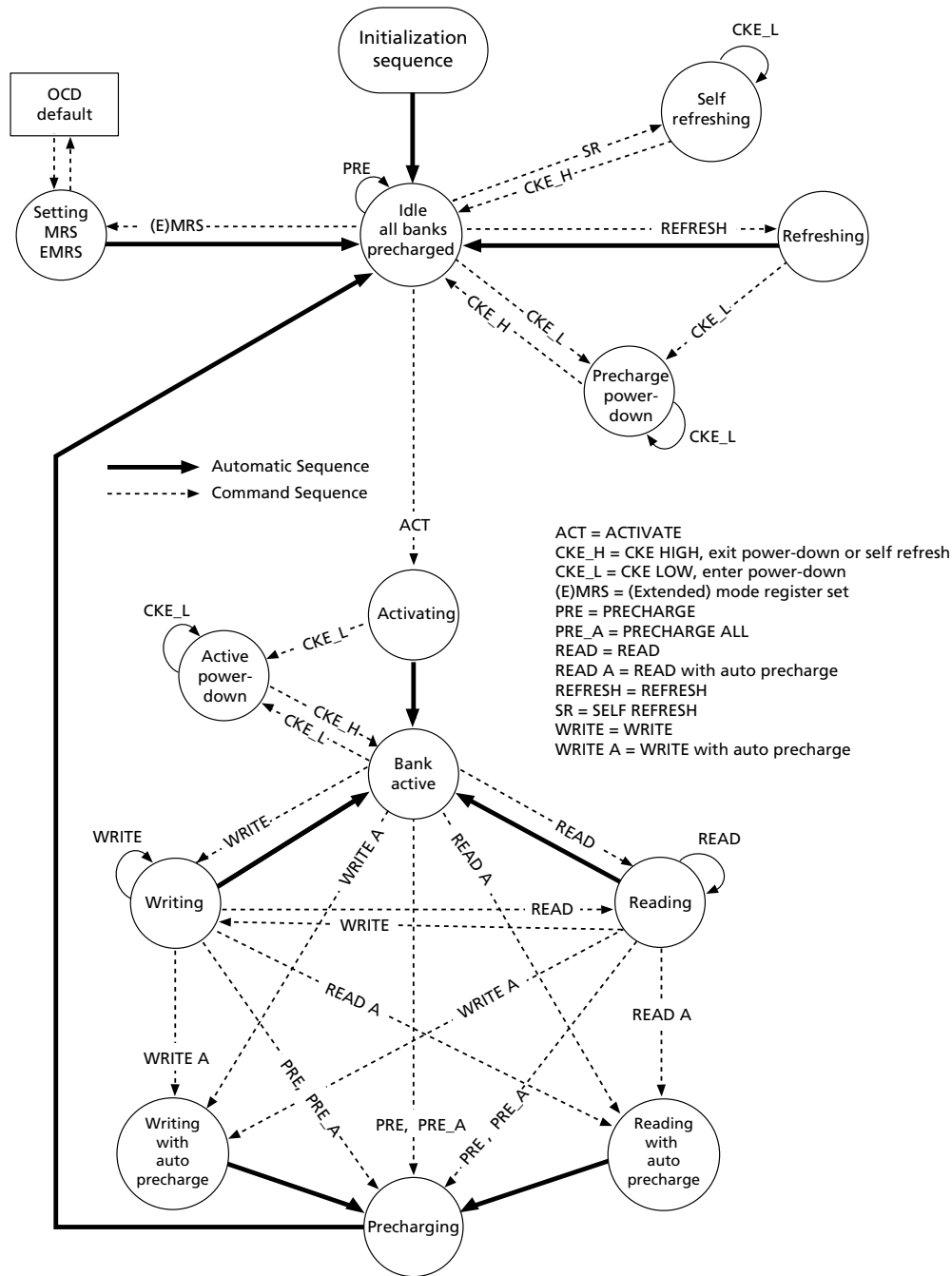
List of Figures

Figure 1: 512Mb DDR2 Part Numbers	2
Figure 2: Simplified State Diagram	9
Figure 3: 128 Meg x 4 Functional Block Diagram	12
Figure 4: 64 Meg x 8 Functional Block Diagram	13
Figure 5: 32 Meg x 16 Functional Block Diagram	14
Figure 6: 60-Ball FBGA – x4, x8 Ball Assignments (Top View)	15
Figure 7: 84-Ball FBGA – x16 Ball Assignments (Top View)	16
Figure 8: 84-Ball FBGA (12mm x 12.5mm) – x16	20
Figure 9: 84-Ball FBGA (10mm x 12.5mm) – x16	21
Figure 10: 84-Ball FBGA (8mm x 12.5mm) – x16	22
Figure 11: 60-Ball FBGA (12mm x 10mm) – x4, x8	23
Figure 12: 60-Ball FBGA (10mm x 10mm) – x4, x8	24
Figure 13: 60-Ball FBGA (8mm x 10mm) – x4, x8	25
Figure 14: Example Temperature Test Point Location	28
Figure 15: Single-Ended Input Signal Levels	48
Figure 16: Differential Input Signal Levels	49
Figure 17: Differential Output Signal Levels	51
Figure 18: Output Slew Rate Load	52
Figure 19: Full Strength Pull-Down Characteristics	53
Figure 20: Full Strength Pull-Up Characteristics	54
Figure 21: Reduced Strength Pull-Down Characteristics	55
Figure 22: Reduced Strength Pull-Up Characteristics	56
Figure 23: Input Clamp Characteristics	57
Figure 24: Overshoot	58
Figure 25: Undershoot	58
Figure 26: Nominal Slew Rate for ^t IS	63
Figure 27: Tangent Line for ^t IS	63
Figure 28: Nominal Slew Rate for ^t IH	64
Figure 29: Tangent Line for ^t IH	65
Figure 30: Nominal Slew Rate for ^t DS	70
Figure 31: Tangent Line for ^t DS	70
Figure 32: Nominal Slew Rate for ^t DH	71
Figure 33: Tangent Line for ^t DH	71
Figure 34: AC Input Test Signal Waveform Command/Address Balls	72
Figure 35: AC Input Test Signal Waveform for Data with DQS, DQS# (Differential)	72
Figure 36: AC Input Test Signal Waveform for Data with DQS (Single-Ended)	73
Figure 37: AC Input Test Signal Waveform (Differential)	73
Figure 38: MR Definition	81
Figure 39: CL	85
Figure 40: EMR Definition	86
Figure 41: READ Latency	89
Figure 42: WRITE Latency	89
Figure 43: EMR2 Definition	90
Figure 44: EMR3 Definition	91
Figure 45: DDR2 Power-Up and Initialization	93
Figure 46: Example: Meeting ^t RRD (MIN) and ^t RCD (MIN)	96
Figure 47: Multibank Activate Restriction	97
Figure 48: READ Latency	99
Figure 49: Consecutive READ Bursts	100
Figure 50: Nonconsecutive READ Bursts	101

Figure 51: READ Interrupted by READ	102
Figure 52: READ-to-WRITE	102
Figure 53: READ-to-PRECHARGE – BL = 4	103
Figure 54: READ-to-PRECHARGE – BL = 8	103
Figure 55: Bank Read – Without Auto Precharge	105
Figure 56: Bank Read – with Auto Precharge	106
Figure 57: x4, x8 Data Output Timing – ^t DQSQ, ^t QH, and Data Valid Window	107
Figure 58: x16 Data Output Timing – ^t DQSQ, ^t QH, and Data Valid Window	108
Figure 59: Data Output Timing – ^t AC and ^t DQSCK	109
Figure 60: Write Burst	111
Figure 61: Consecutive WRITE-to-WRITE	112
Figure 62: Nonconsecutive WRITE-to-WRITE	112
Figure 63: WRITE Interrupted by WRITE	113
Figure 64: WRITE-to-READ	114
Figure 65: WRITE-to-PRECHARGE	115
Figure 66: Bank Write – Without Auto Precharge	116
Figure 67: Bank Write – with Auto Precharge	117
Figure 68: WRITE – DM Operation	118
Figure 69: Data Input Timing	119
Figure 70: Refresh Mode	120
Figure 71: Self Refresh	122
Figure 72: Power-Down	124
Figure 73: READ-to-Power-Down or Self Refresh Entry	126
Figure 74: READ with Auto Precharge-to-Power-Down or Self Refresh Entry	126
Figure 75: WRITE-to-Power-Down or Self Refresh Entry	127
Figure 76: WRITE with Auto Precharge-to-Power-Down or Self Refresh Entry	127
Figure 77: REFRESH Command-to-Power-Down Entry	128
Figure 78: ACTIVATE Command-to-Power-Down Entry	128
Figure 79: PRECHARGE Command-to-Power-Down Entry	129
Figure 80: LOAD MODE Command-to-Power-Down Entry	129
Figure 81: Input Clock Frequency Change During Precharge Power-Down Mode	130
Figure 82: RESET Function	132
Figure 83: ODT Timing for Entering and Exiting Power-Down Mode	134
Figure 84: Timing for MRS Command to ODT Update Delay	135
Figure 85: ODT Timing for Active or Fast-Exit Power-Down Mode	135
Figure 86: ODT Timing for Slow-Exit or Precharge Power-Down Modes	136
Figure 87: ODT Turn-Off Timings When Entering Power-Down Mode	136
Figure 88: ODT Turn-On Timing When Entering Power-Down Mode	137
Figure 89: ODT Turn-Off Timing When Exiting Power-Down Mode	138
Figure 90: ODT Turn-On Timing When Exiting Power-Down Mode	139

State Diagram

Figure 2: Simplified State Diagram



Note: 1. This diagram provides the basic command flow. It is not comprehensive and does not identify all timing requirements or possible command restrictions such as multibank interaction, power down, entry/exit, etc.

Functional Description

The DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$ -prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the DDR2 SDRAM effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR2 SDRAM enables concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Industrial Temperature

The industrial temperature (IT) option, if offered, has two simultaneous requirements: ambient temperature surrounding the device cannot be less than -40°C or greater than $+85^{\circ}\text{C}$, and the case temperature cannot be less than -40°C or greater than $+95^{\circ}\text{C}$. JEDEC specifications require the refresh rate to double when T_C exceeds $+85^{\circ}\text{C}$; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is $< 0^{\circ}\text{C}$ or $> +85^{\circ}\text{C}$.

Automotive Temperature

The automotive temperature (AT) option, if offered, has two simultaneous requirements: ambient temperature surrounding the device cannot be less than -40°C or greater than $+105^{\circ}\text{C}$, and the case temperature cannot be less than -40°C or greater than $+105^{\circ}\text{C}$. JEDEC specifications require the refresh rate to double when T_C exceeds $+85^{\circ}\text{C}$; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is $< 0^{\circ}\text{C}$ or $> +85^{\circ}\text{C}$.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

Functional Block Diagrams

The DDR2 SDRAM is a high-speed CMOS, dynamic random access memory. It is internally configured as a multibank DRAM.

Figure 3: 128 Meg x 4 Functional Block Diagram

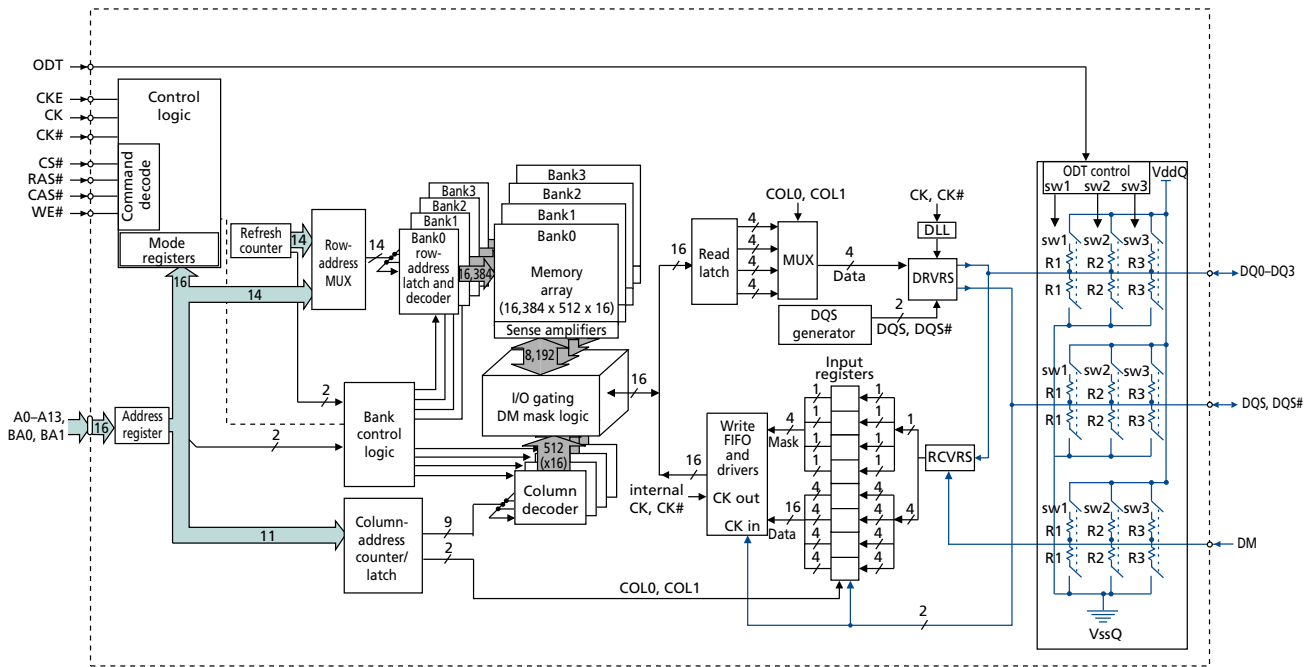


Figure 4: 64 Meg x 8 Functional Block Diagram

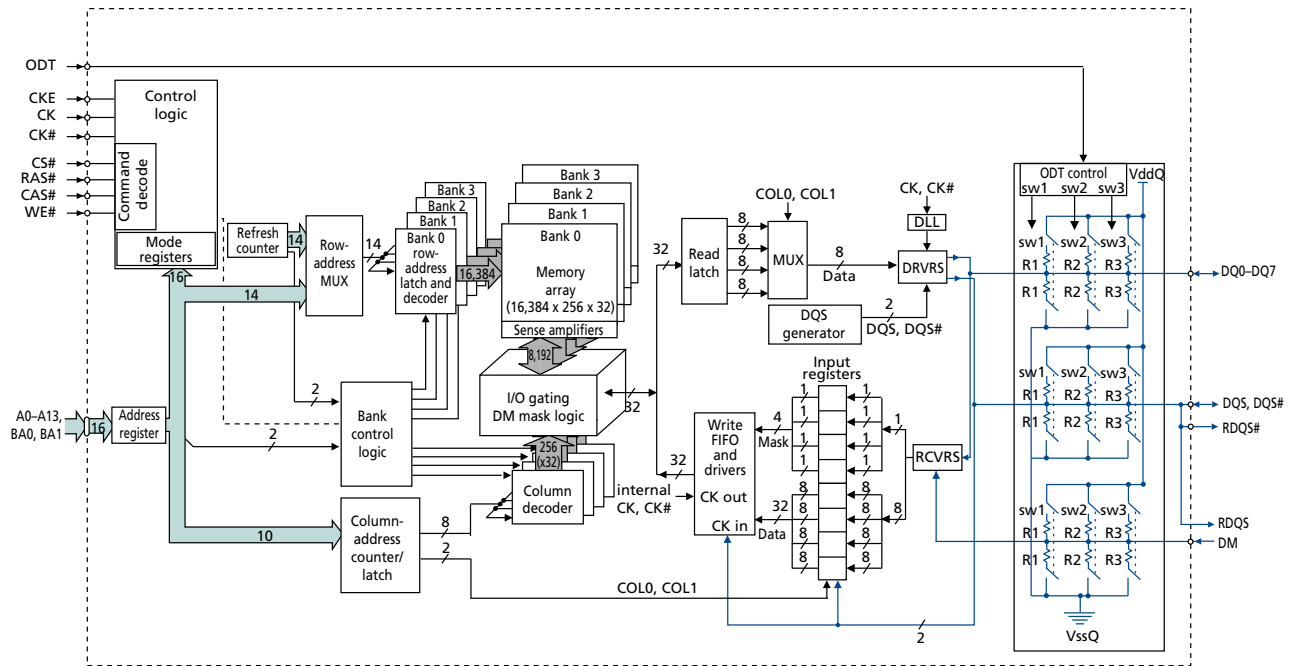
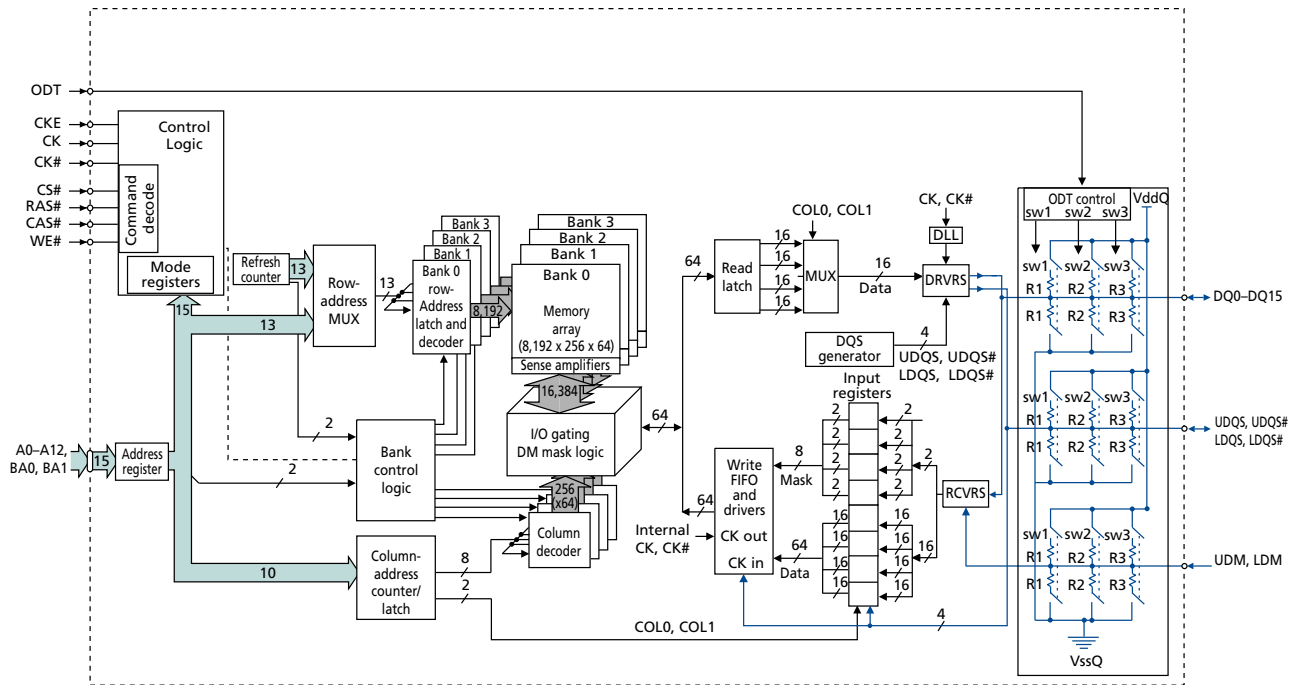


Figure 5: 32 Meg x 16 Functional Block Diagram



Ball Assignments and Descriptions

Figure 6: 60-Ball FBGA – x4, x8 Ball Assignments (Top View)

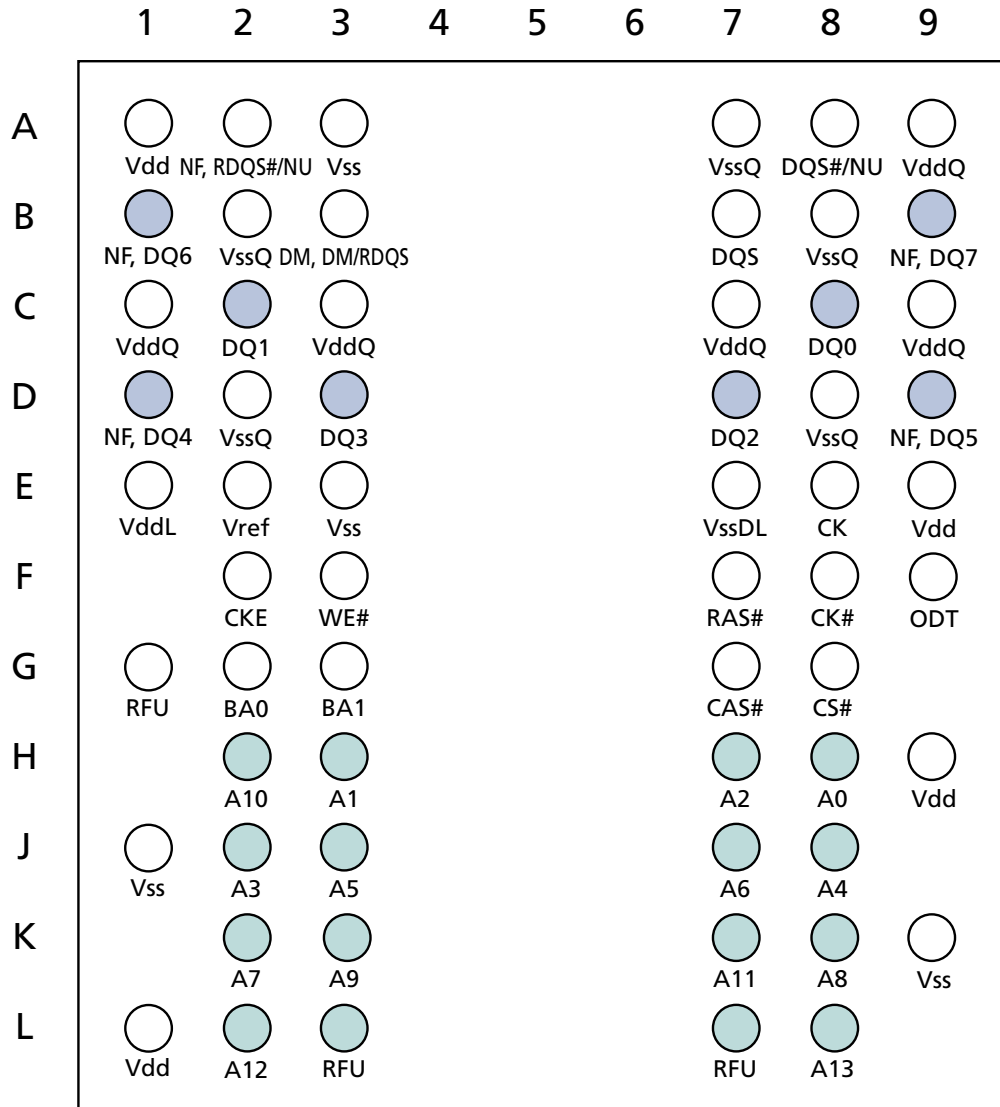


Figure 7: 84-Ball FBGA – x16 Ball Assignments (Top View)

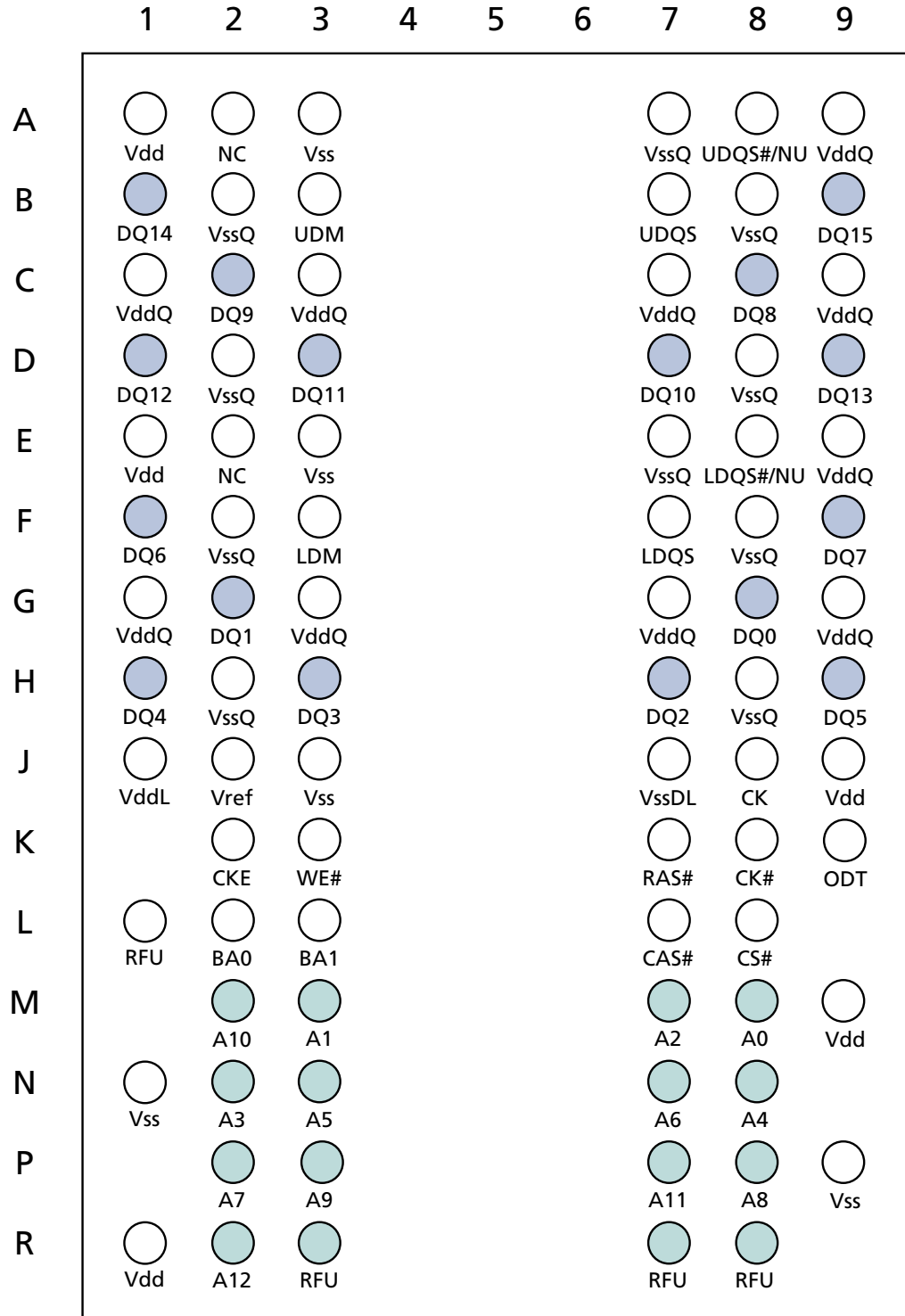


Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
M8, M3, M7, N2, N8, N3, N7, P2, P8, P3, M2, P7, R2	–	A0–A2, A3–A5, A6–A8, A9, A10, A11, A12	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
–	H8, H3, H7, J2, J8, J3, J7, K2, K8, K3, H2, K7, L2, L8	A0–A2, A3–A5, A6–A8, A9, A10, A11, A12, A13	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
L2, L3	G2, G3	BA0, BA1	Input	Bank address inputs: BA[1:0] define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
J8, K8	E8, F8	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
K2	F2	CKE	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides pre-charge power-down and SELF REFRESH operations (all banks idle), or ACTIVATE power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once Vdd is applied during first power-up. After Vref has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, Vref must be maintained.

Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions (Continued)

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
L8	G8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered high. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
F3, B3	B3	LDM, UDM, DM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
K9	F9	ODT	Input	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
K7, L7, K3	F7, G7, F3	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
G8, G2, H7, H3, H1, H9, F1, F9, C8, C2, D7, D3, D1, D9, B1, B9	–	DQ0–DQ2, DQ3–DQ5, DQ6–DQ8, DQ9–DQ11, DQ12–DQ14, DQ15	I/O	Data input/output: Bidirectional data bus for 32 Meg x 16.
–	C8, C2, D7, D3, D1, D9, B1, B9	DQ0–DQ2, DQ3–DQ5, DQ6, DQ7	I/O	Data input/output: Bidirectional data bus for 64 Meg x 8.
–	C8, C2, D7, D3	DQ0–DQ2, DQ3	I/O	Data input/output: Bidirectional data bus for 128 Meg x 4.
–	B7, A8	DQS, DQS#	I/O	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
F7, E8	–	LDQS, LDQS#	I/O	Data strobe for lower byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.

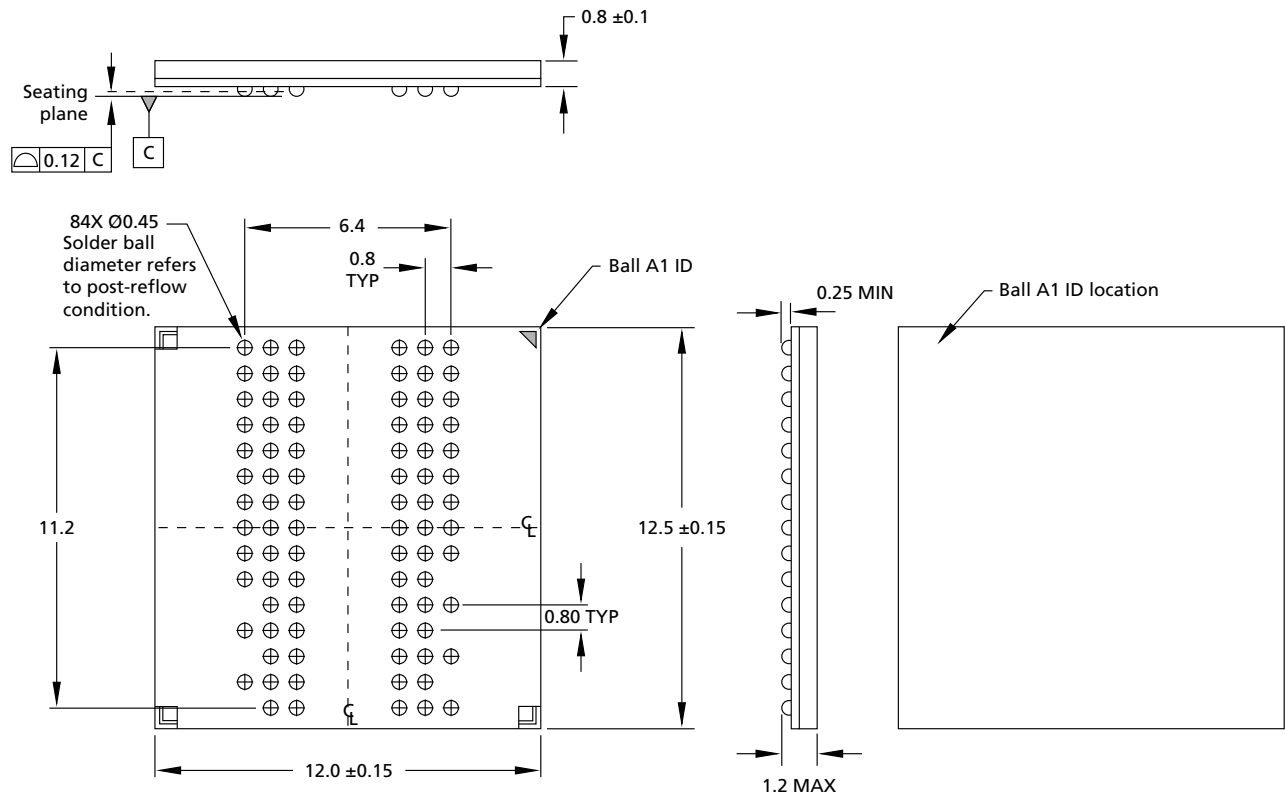
Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions (Continued)

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
B7, A8	–	UDQS, UDQS#	I/O	Data strobe for upper byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	B3, A2	RDQS, RDQS#	Output	Redundant data strobe: For 64 Meg x 8 only. RDQS is enabled/disabled via the load mode command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball B3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled <i>and</i> differential data strobe mode is enabled.
A1, E1, M9, R1, J9	A1, E9, L1, H9	Vdd	Supply	Power supply: 1.8V ±0.1V.
A9, C1, C3, C7, C9, G3, E9, G1, G7, G9	A9, C1, C3, C7, C9	VddQ	Supply	DQ power supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity.
J1	E1	VddL	Supply	DLL power supply: 1.8V ±0.1V.
J2	E2	Vref	Supply	SSTL_18 reference voltage (VddQ/2).
A3, E3, J3, N1, P9	A3, E3, J1, K9	Vss	Supply	Ground.
J7	E7	VssDL	Supply	DLL ground: Isolated on the device from Vss and VssQ.
A7, B2, B8, D2, D8, E7, F2, F8, H2, H8	A7, B2, B8, D2, D8	VssQ	Supply	DQ ground: Isolated on the device for improved noise immunity.
A2, E2	–	NC	–	No connect: These balls should be left unconnected.
–	B1, B9, D1, D9	NF	–	No function: x8: these balls are used as DQ4–DQ7; x4: they are no function.
A8, E8	A2, A8	NU	–	Not used: If EMR(E10) = 0: x16, A8 = UDQS# and E8 = LDQS#; x8, A2 = RDQS# and A8 = DQS#; x4, A2 = NU and A8 = NU. If EMR(E10) = 1: x16, A8 = NU and E8 = NU; x8, A2 = NU and A8 = NU; x4, A2 = NU and A8 = NU.
L1, R8, R3, R7	G1, L3, L7	RFU	–	Reserved for future use: Bank address BA2, row address bits A13 (x16 only), A14, and A15.

Packaging

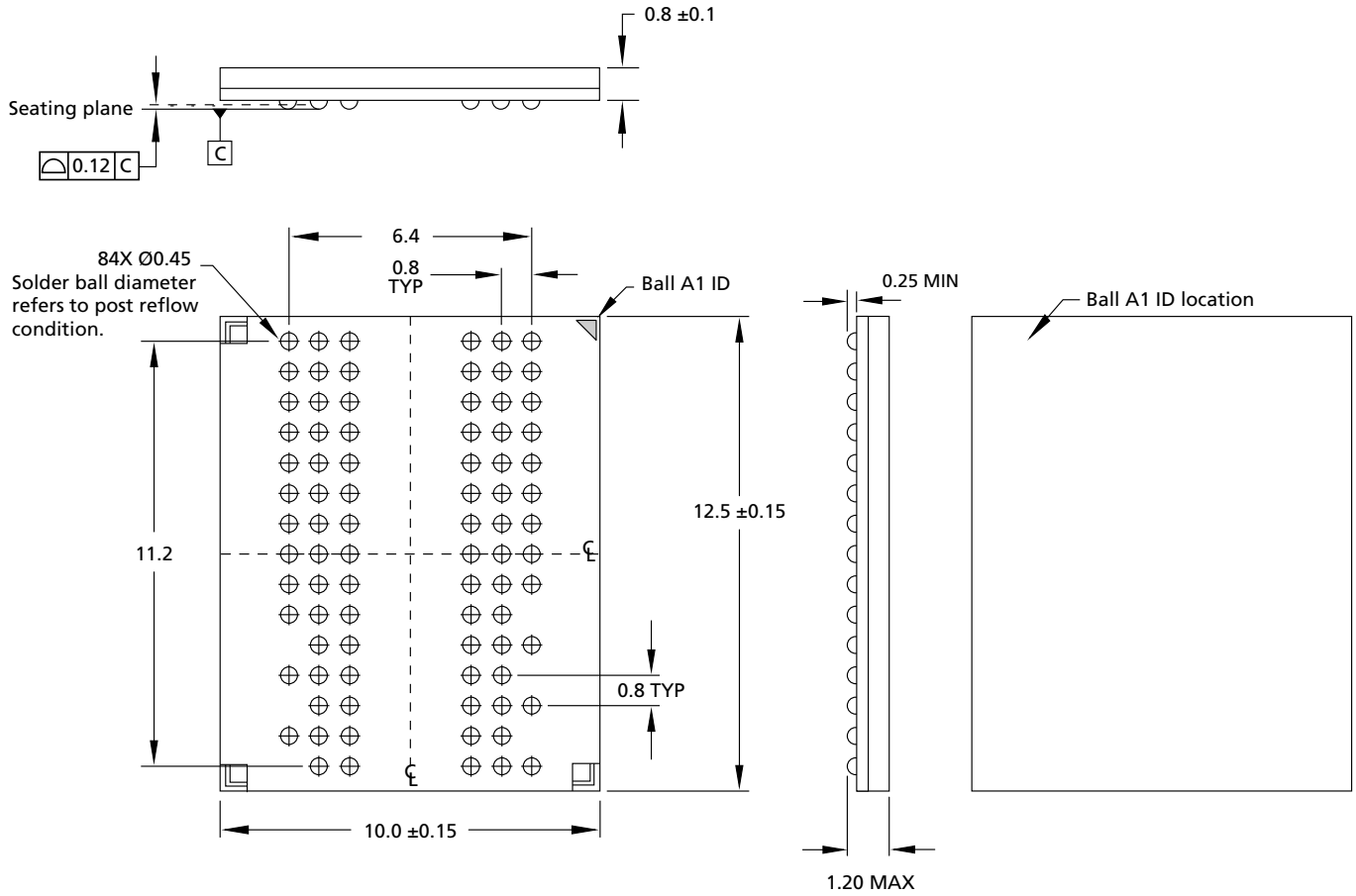
Package Dimensions

Figure 8: 84-Ball FBGA (12mm x 12.5mm) – x16



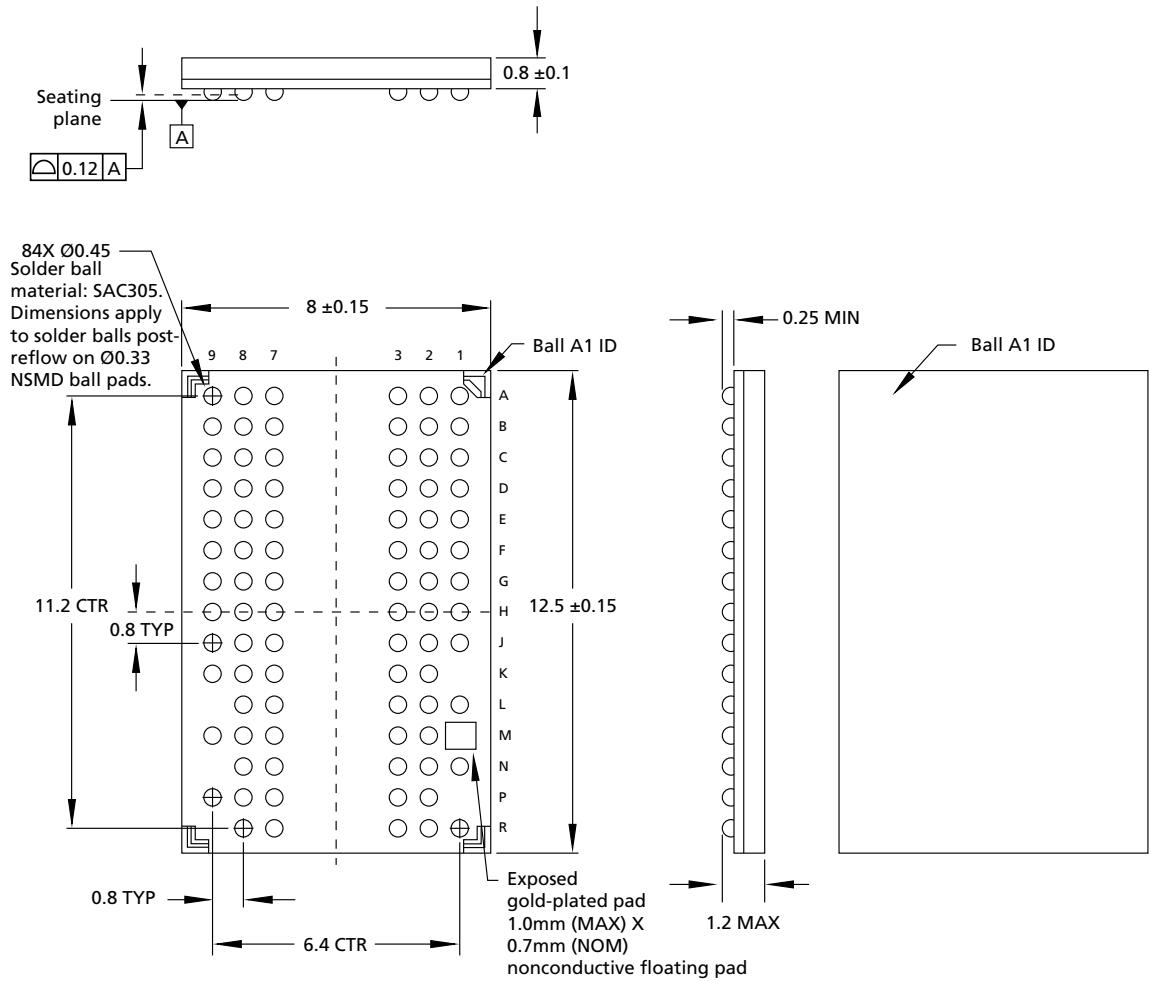
Note: 1. All dimensions are in millimeters.

Figure 9: 84-Ball FBGA (10mm x 12.5mm) – x16



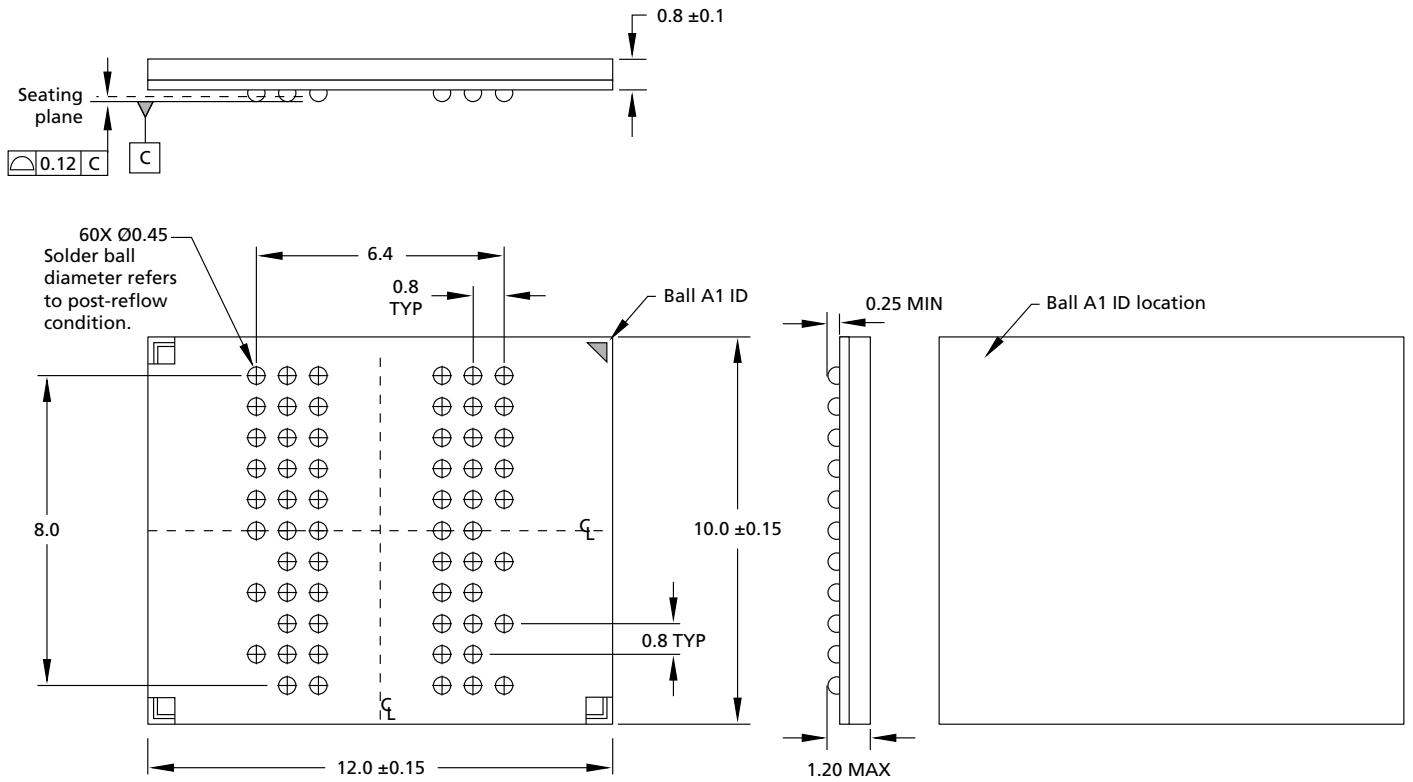
Note: 1. All dimensions are in millimeters.

Figure 10: 84-Ball FBGA (8mm x 12.5mm) – x16



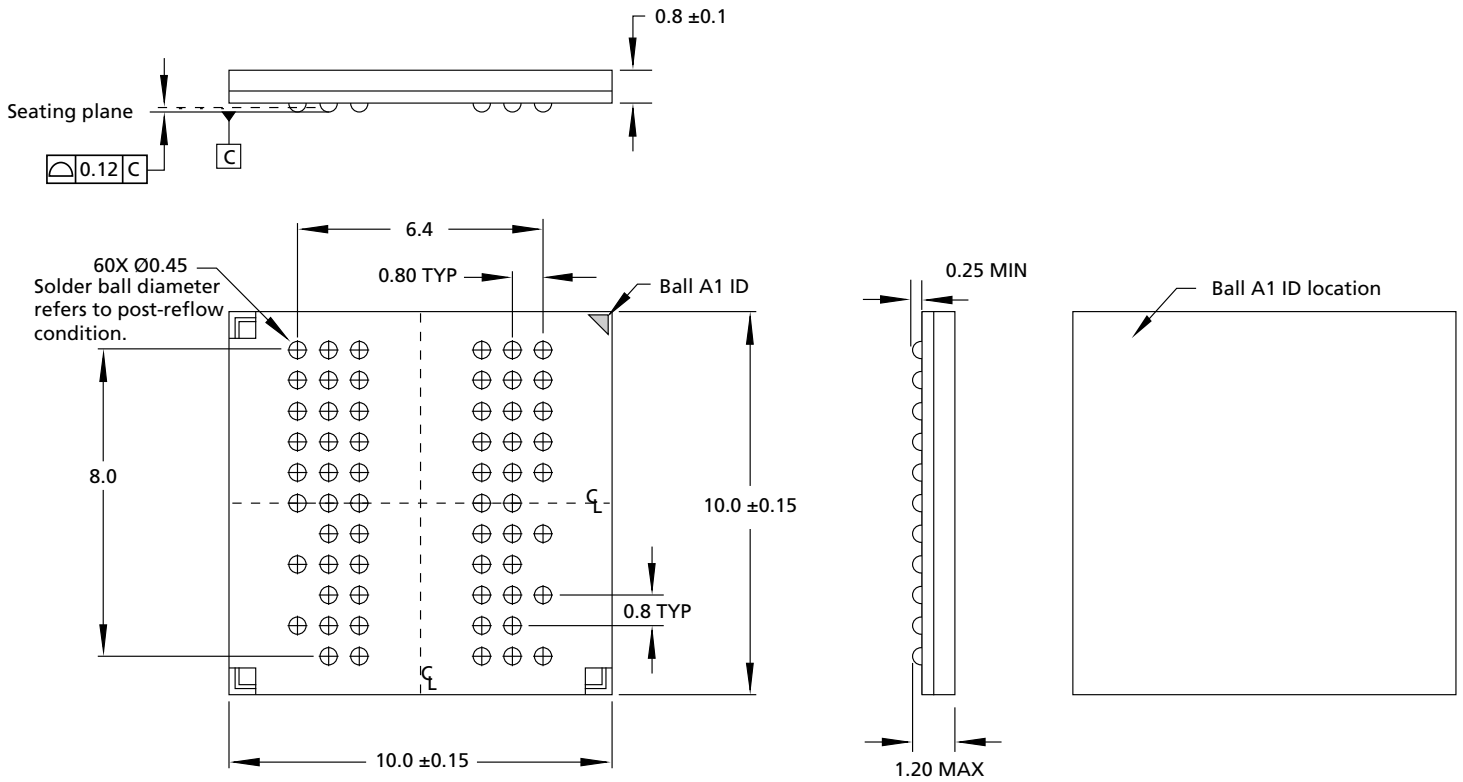
Note: 1. All dimensions are in millimeters.

Figure 11: 60-Ball FBGA (12mm x 10mm) – x4, x8



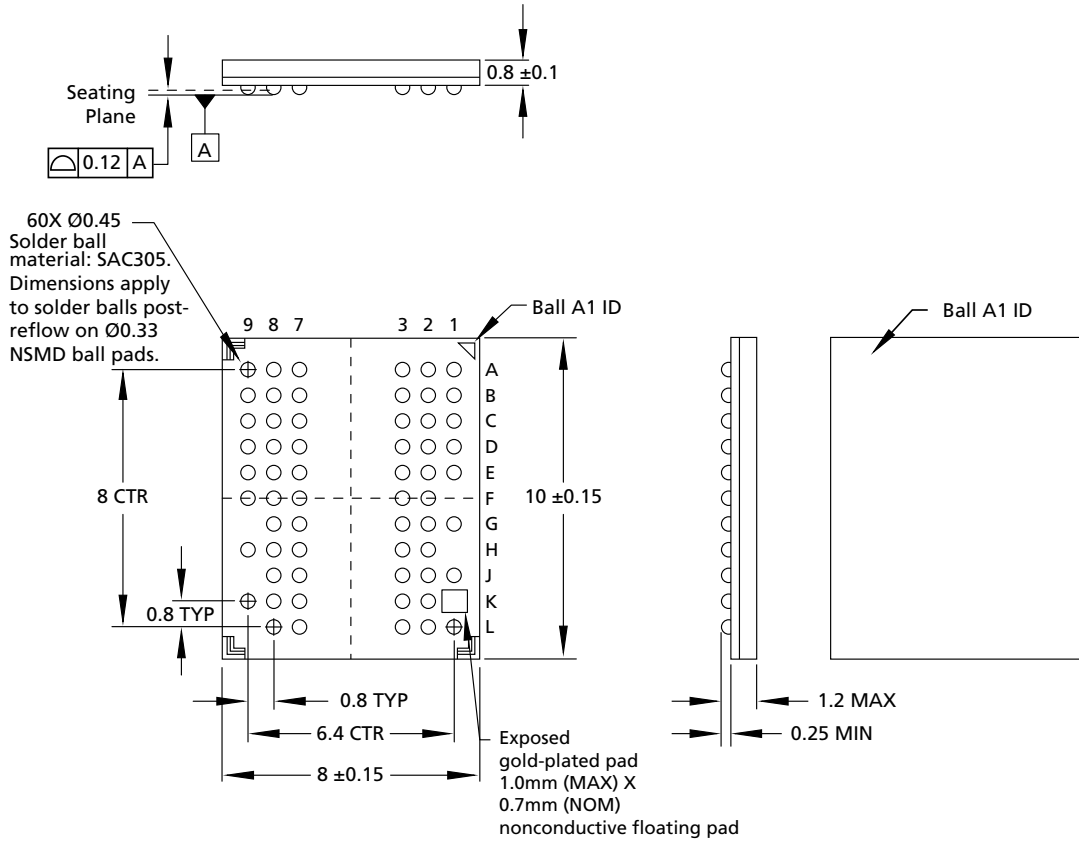
Note: 1. All dimensions are in millimeters.

Figure 12: 60-Ball FBGA (10mm x 10mm) – x4, x8



Note: 1. All dimensions are in millimeters.

Figure 13: 60-Ball FBGA (8mm x 10mm) – x4, x8



Note: 1. All dimensions are in millimeters.