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DDR2 SDRAM

MT47H128M4 – 32 Meg x 4 x 4 banks
MT47H64M8 – 16 Meg x 8 x 4 banks
MT47H32M16 – 8 Meg x 16 x 4 banks

Features

- V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 4 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Selectable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Automotive temperature (AT) option
- RoHS-compliant
- Supports JEDEC clock jitter specification

Options[1]	Marking
• Configuration	
– 128 Meg x 4 (32 Meg x 4 x 4 banks)	128M4
– 64 Meg x 8 (16 Meg x 8 x 4 banks)	64M8
– 32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
• FBGA package (Pb-free) – x16	
– 84-ball FBGA (8mm x 12.5mm) Rev. F, G	HR
• FBGA package (Pb-free) – x4, x8	
– 60-ball FBGA (8mm x 10mm) Rev. F, G	CF
• FBGA package (lead solder) – x16	
– 84-ball FBGA (8mm x 12.5mm) Rev. F, G	HW
• FBGA package (lead solder) – x4, x8	
– 60-ball FBGA (8mm x 10mm) Rev. F, G	JN
• Timing – cycle time	
– 1.875ns @ CL = 7 (DDR2-1066)	-187E
– 2.5ns @ CL = 5 (DDR2-800)	-25E
– 2.5ns @ CL = 6 (DDR2-800)	-25
– 3.0ns @ CL = 4 (DDR2-667)	-3E
– 3.0ns @ CL = 5 (DDR2-667)	-3
– 3.75ns @ CL = 4 (DDR2-533)	-37E
• Self refresh	
– Standard	None
– Low-power	L
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 85°C)	None
– Industrial (–40°C ≤ T_C ≤ 95°C; –40°C ≤ T_A ≤ 85°C)	IT
– Automotive (–40°C ≤ T_C, T_A ≤ 105°C)	AT
• Revision	:F/:G

Note: 1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for product offerings and availability.

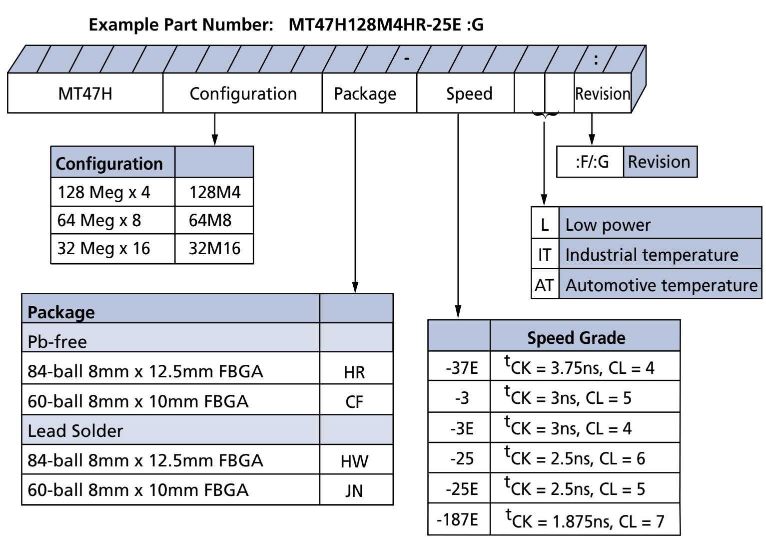
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)				^tRC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	
-187E	400	533	800	1066	54
-25E	400	533	800	800	55
-25	400	533	667	800	55
-3E	400	667	667	n/a	54
-3	400	533	667	n/a	55
-37E	400	533	n/a	n/a	55

Table 2: Addressing

Parameter	128 Meg x 4	64 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	A[13:0] (16K)	A[13:0] (16K)	A[12:0] (8K)
Bank address	BA[1:0] (4)	BA[1:0] (4)	BA[1:0] (4)
Column address	A[11, 9:0] (2K)	A[9:0] (1K)	A[9:0] (1K)

Figure 1: 512Mb DDR2 Part Numbers



Note: 1. Not all speeds and configurations are available in all packages.

FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

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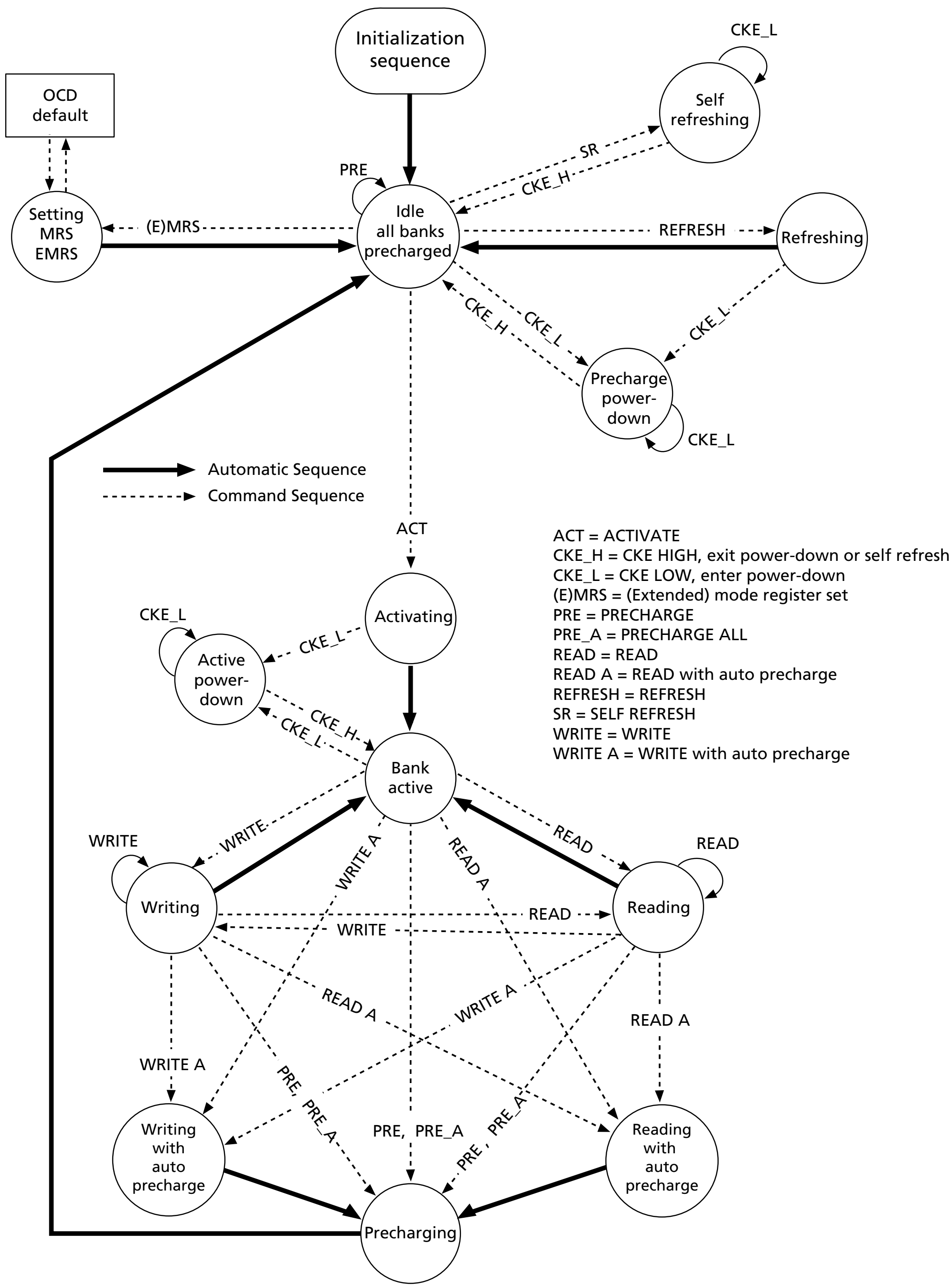
State Diagram

Figure 2: Simplified State Diagram



Note: 1. This diagram provides the basic command flow. It is not comprehensive and does not identify all timing requirements or possible command restrictions such as multibank interaction, power down, entry/exit, etc.

Functional Description

The DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR2 SDRAM enables concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Industrial Temperature

The industrial temperature (IT) option, if offered, has two simultaneous requirements: ambient temperature surrounding the device cannot be less than –40°C or greater than +85°C, and the case temperature cannot be less than –40°C or greater than +95°C. JEDEC specifications require the refresh rate to double when T_C exceeds +85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, input/output impedance and IDD values must be derated when T_C is < 0°C or > +85°C.

Automotive Temperature

The automotive temperature (AT) option, if offered, has two simultaneous requirements: ambient temperature surrounding the device cannot be less than –40°C or greater than +105°C, and the case temperature cannot be less than –40°C or greater than +105°C. JEDEC specifications require the refresh rate to double when T_C exceeds +85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance the input/output impedance and IDD values must be derated when T_C is < 0°C or > +85°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

Functional Block Diagrams

The DDR2 SDRAM is a high-speed CMOS, dynamic random access memory. It is internally configured as a multibank DRAM.

Figure 3: 128 Meg x 4 Functional Block Diagram

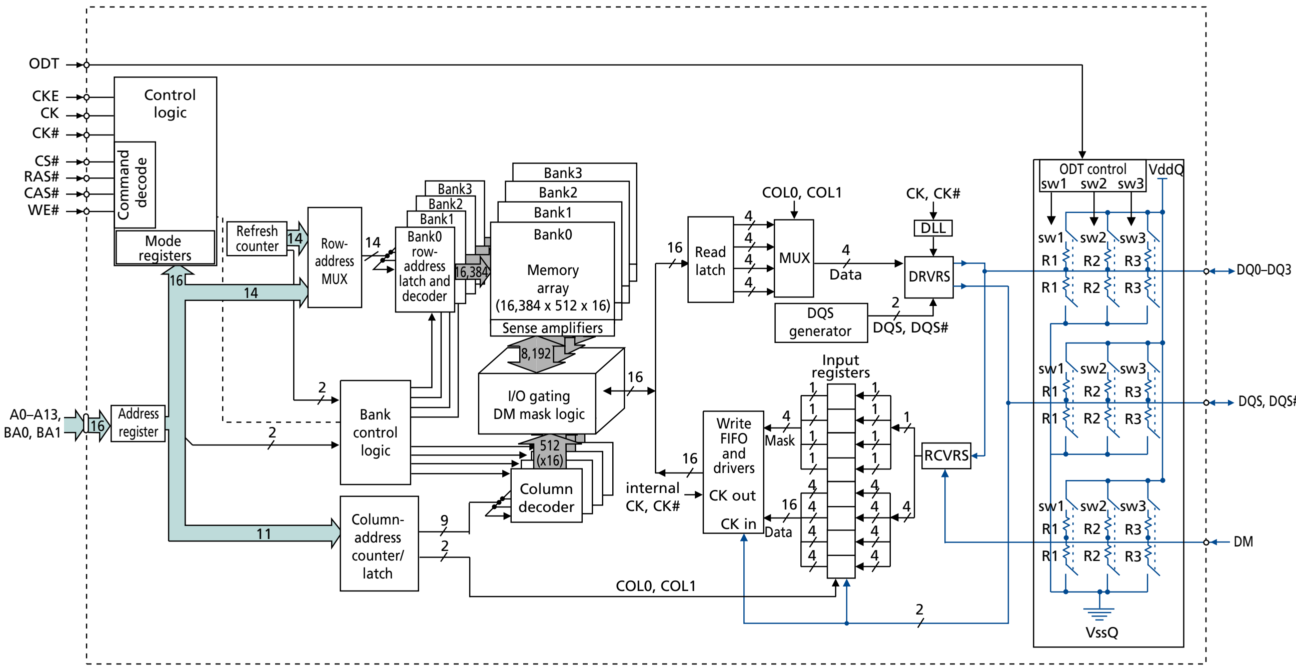


Figure 4: 64 Meg x 8 Functional Block Diagram

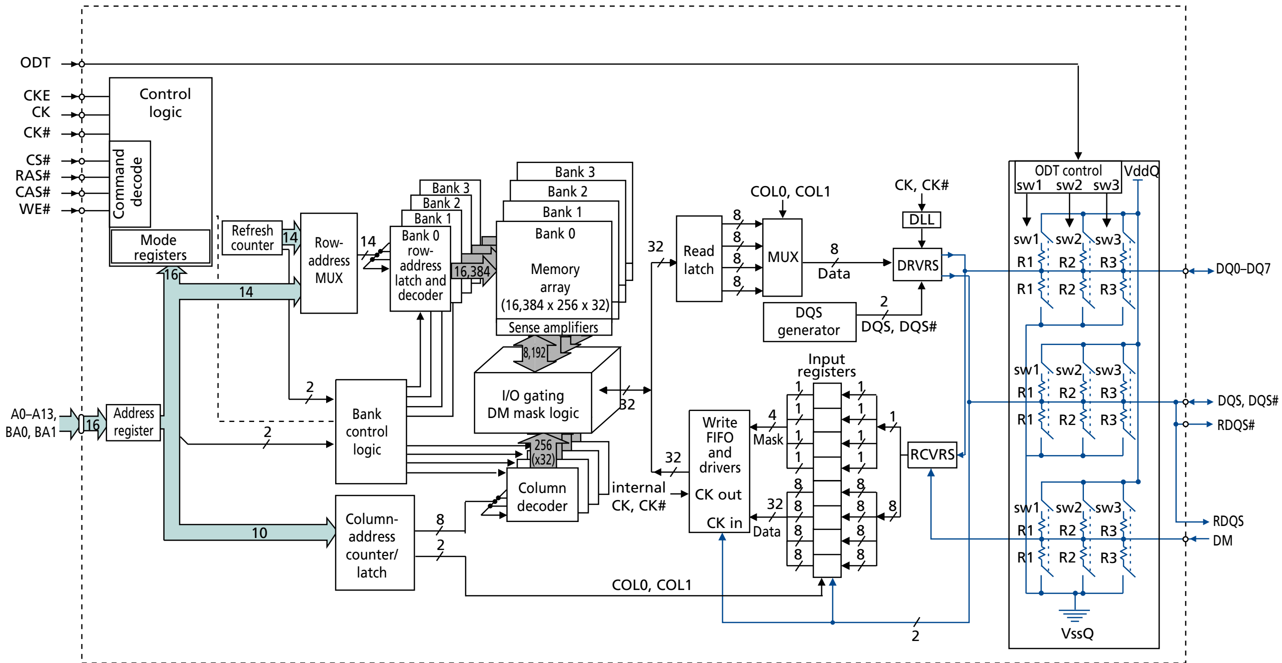
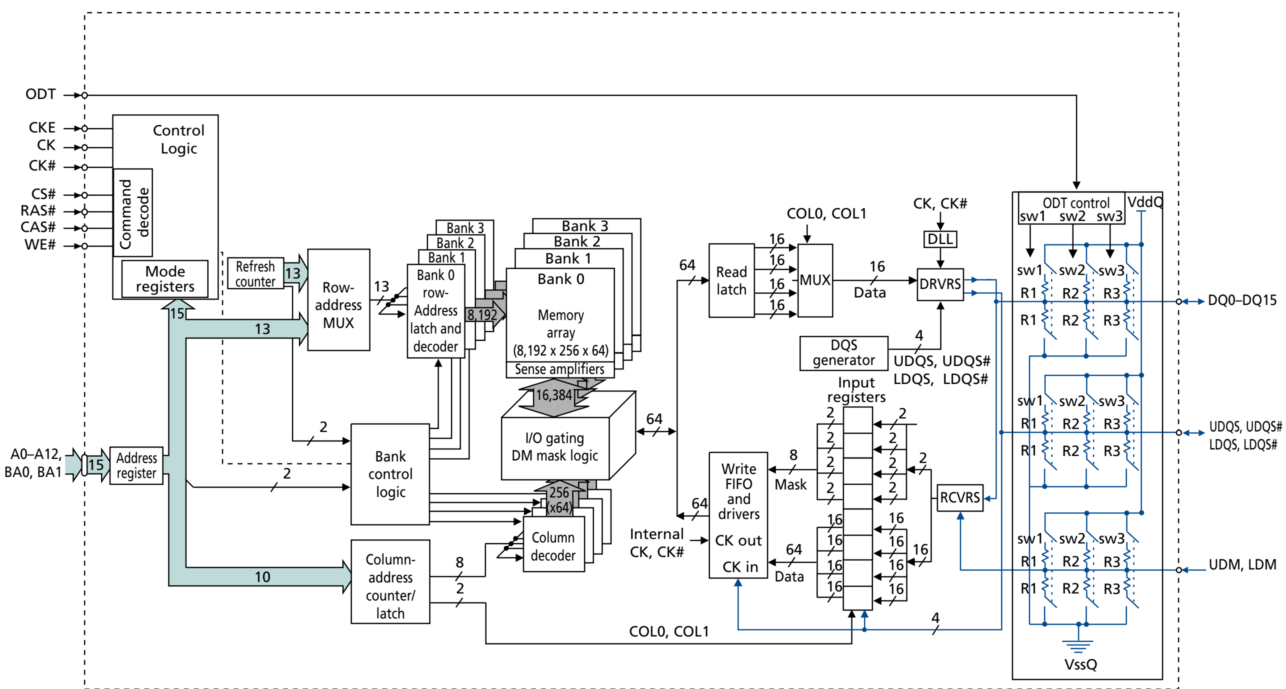


Figure 5: 32 Meg x 16 Functional Block Diagram



Ball Assignments and Descriptions

Figure 6: 60-Ball FBGA – x4, x8 Ball Assignments (Top View)

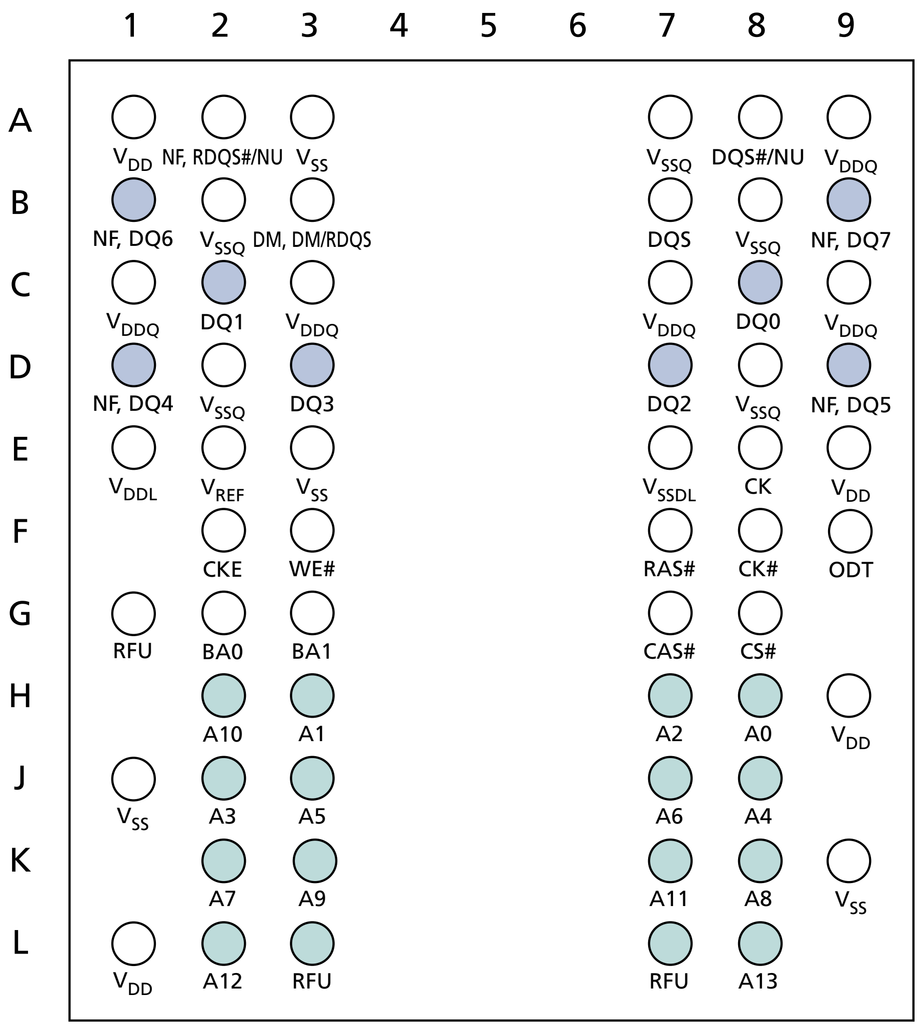


Figure 7: 84-Ball FBGA – x16 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	V_{DD}	NC	V_{SS}				V_{SSQ}	UDQS#/NU	V_{DDQ}
B	DQ14	V_{SSQ}	UDM				UDQS	V_{SSQ}	DQ15
C	V_{DDQ}	DQ9	V_{DDQ}				V_{DDQ}	DQ8	V_{DDQ}
D	DQ12	V_{SSQ}	DQ11				DQ10	V_{SSQ}	DQ13
E	V_{DD}	NC	V_{SS}				V_{SSQ}	LDQS#/NU	V_{DDQ}
F	DQ6	V_{SSQ}	LDM				LDQS	V_{SSQ}	DQ7
G	V_{DDQ}	DQ1	V_{DDQ}				V_{DDQ}	DQ0	V_{DDQ}
H	DQ4	V_{SSQ}	DQ3				DQ2	V_{SSQ}	DQ5
J	V_{DDL}	V_{REF}	V_{SS}				V_{SSDL}	CK	V_{DD}
K		CKE	WE#				RAS#	CK#	ODT
L	RFU	BA0	BA1				CAS#	CS#	
M		A10	A1				A2	A0	V_{DD}
N	V_{SS}	A3	A5				A6	A4	
P		A7	A9				A11	A8	V_{SS}
R	V_{DD}	A12	RFU				RFU	RFU	

Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions

Symbol	Type	Description
A[12:0] (x16) A[13:0] (x4, x8)	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[1:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
BA0, BA1	Input	**Bank address inputs:** BA[1:0] define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[1:0] define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down and SELF REFRESH operations (all banks idle), or ACTIVATE power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, V_{REF} must be maintained.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered high. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
LDM, UDM, DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ[7:0] and UDM is DM for upper byte DQ[15:8].
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ[15:0], LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ[7:0], DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.
DQ[15:0] (x16) DQ[3:0] (x4) DQ[7:0] (x8)	I/O	**Data input/output:** Bidirectional data bus for 32 Meg x 16. Bidirectional data bus for 128 Meg x 4. Bidirectional data bus for 64 Meg x 8.

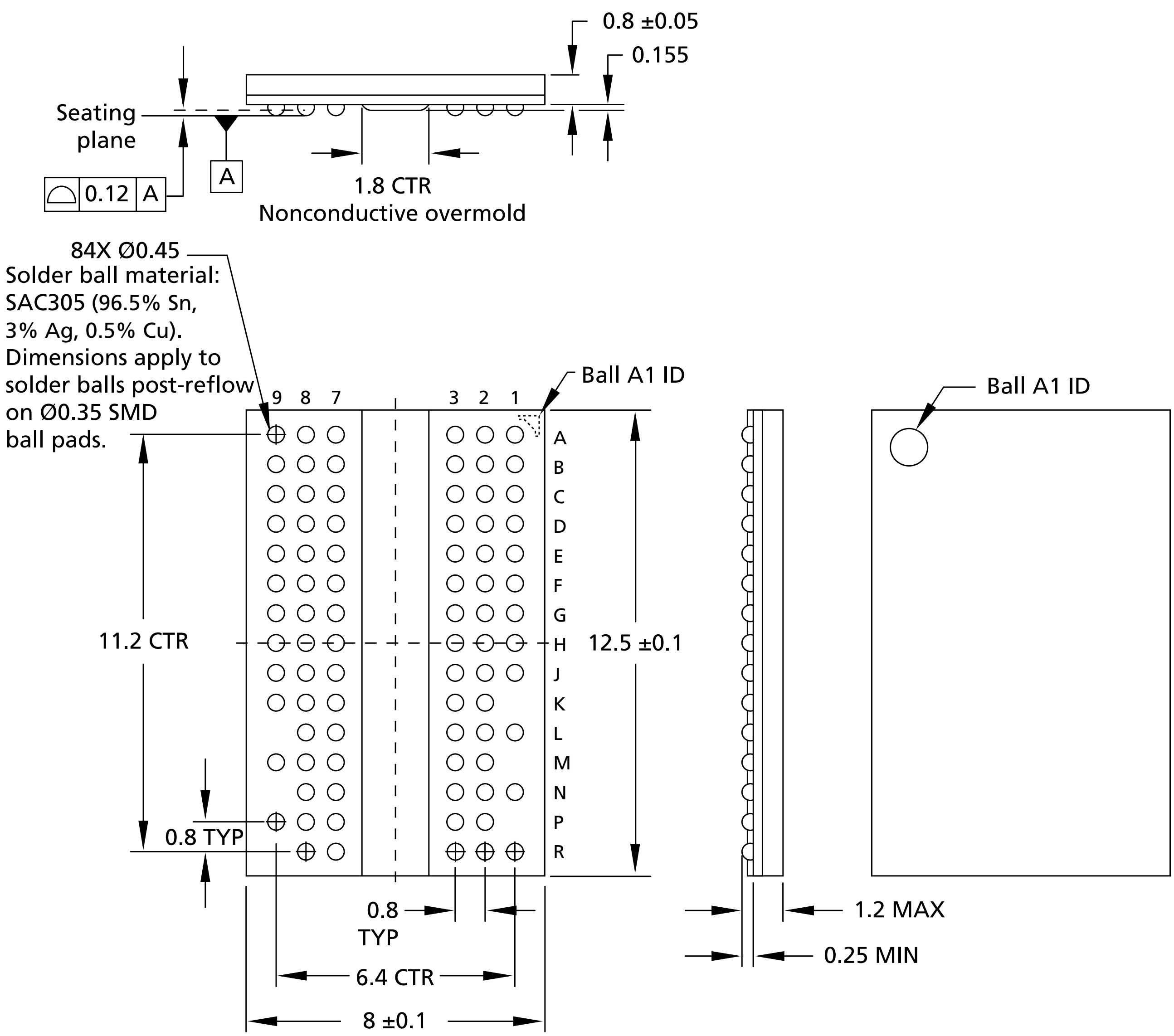
Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions (Continued)

Symbol	Type	Description
DQS, DQS#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
LDQS, LDQS#	I/O	**Data strobe for lower byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
UDQS, UDQS#	I/O	**Data strobe for upper byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
RDQS, RDQS#	Output	**Redundant data strobe:** For 64 Meg x 8 only. RDQS is enabled/disabled via the load mode command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball B3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled *and* differential data strobe mode is enabled.
V_{DD}	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDQ}	Supply	**DQ power supply:** 1.8V ±0.1V. Isolated on the device for improved noise immunity.
V_{DDL}	Supply	**DLL power supply:** 1.8V ±0.1V.
V_{REF}	Supply	SSTL_18 reference voltage (V_{DDQ}/2).
V_{SS}	Supply	Ground.
V_{SSDL}	Supply	**DLL ground:** Isolated on the device from V_{SS} and V_{SSQ}.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NC	–	**No connect:** These balls should be left unconnected.
NF	–	**No function: x8:** these balls are used as DQ[7:4]; x4: they are no function.
NU	–	**Not used:** If EMR(E10) = 0: x16, A8 = UDQS# and E8 = LDQS#; x8, A2 = RDQS# and A8 = DQS#; x4, A2 = NU and A8 = NU. If EMR(E10) = 1: x16, A8 = NU and E8 = NU; x8, A2 = NU and A8 = NU; x4, A2 = NU and A8 = NU.
RFU	–	**Reserved for future use:** Bank address BA2, row address bits A13 (x16 only), A14, and A15.

Packaging

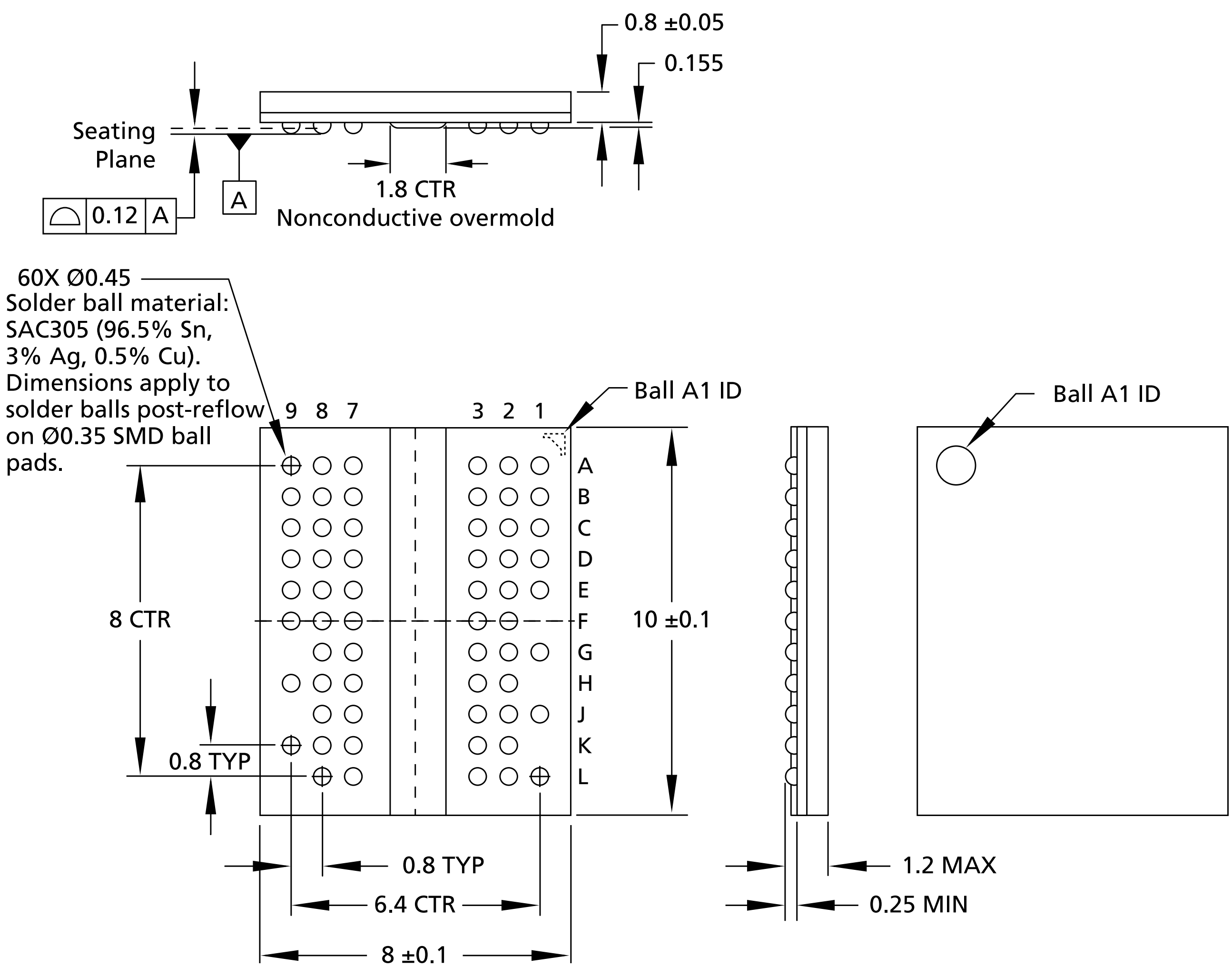
Package Dimensions

Figure 8: 84-Ball FBGA (8mm x 12.5mm) – x16



Notes: 1. All dimensions are in millimeters.
2. Solder ball material for this package is also available as leaded eutectic (62% Sn, 36% Pb, 2% Ag).

Figure 9: 60-Ball FBGA (8mm x 10mm) – x4, x8



Notes:
1. All dimensions are in millimeters.
2. Solder ball material for this package is also available as leaded eutectic (62% Sn, 36% Pb, 2% Ag).

FBGA Package Capacitance

Table 4: Input Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance: CK, CK#	C_{CK}	1.0	2.0	pF	1
Delta input capacitance: CK, CK#	C_{DCK}	–	0.25	pF	2, 3
Input capacitance: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, ODT	C_I	1.0	2.0	pF	1, 4
Delta input capacitance: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, ODT	C_{DI}	–	0.25	pF	2, 3
Input/output capacitance: DQ, DQS, DM, NF	C_{IO}	2.5	4.0	pF	1, 5
Delta input/output capacitance: DQ, DQS, DM, NF	C_{DIO}	–	0.5	pF	2, 3

Notes:
1. This parameter is sampled. V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V, V_{REF} = V_{SS}, f = 100 MHz, T_C = 25°C, $V_{OUT(DC)}$ = V_{DDQ}/2, V_{OUT} (peak-to-peak) = 0.1V. DM input is grouped with I/O balls, reflecting the fact that they are matched in loading.
2. The capacitance per ball group will not differ by more than this maximum amount for any given device.
3. ΔC are not pass/fail parameters; they are targets.
4. Reduce MAX limit by 0.25pF for -25 and -25E speed devices.
5. Reduce MAX limit by 0.5pF for -3, -3E, -5E, -25, -25E, and -37E speed devices.

Electrical Specifications – Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions oustide those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–1.0	2.3	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.5	2.3	V	1, 2
V_{DDL} supply voltage relative to V_{SSL}	V_{DDL}	–0.5	2.3	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	2.3	V	3
Input leakage current; any input 0V ≤ V_{IN} ≤ V_{DD}; all other balls not under test = 0V	I_I	–5	5	µA	
Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT disabled	I_{OZ}	–5	5	µA	
V_{REF} leakage current; V_{REF} = valid V_{REF} level	I_{VREF}	–2	2	µA	

Notes:
1. V_{DD}, V_{DDQ}, and V_{DDL} must be within 300mV of each other at all times; this is not required when power is ramping down.
2. V_{REF} ≤ 0.6 x V_{DDQ}; however, V_{REF} may be ≥ V_{DDQ} provided that V_{REF} ≤ 300mV.
3. Voltage on any I/O may not exceed voltage on V_{DDQ}.

Temperature and Thermal Impedance

It is imperative that the DDR2 SDRAM device's temperature specifications, shown in Table 6 (page 22), be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 7 (page 22) for the applicable and available die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the thermal impedances listed in Table 7. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

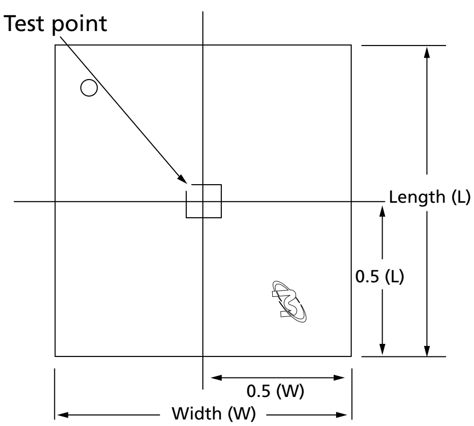
The DDR2 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

Table 6: Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	T_{STG}	–55	150	°C	1
Operating temperature: commercial	T_C	0	85	°C	2, 3
Operating temperature: industrial	T_C	–40	95	°C	2, 3 , 4
	T_A	–40	85	°C	4, 5
Operating temperature: automotive	T_C	–40	105	°C	2, 3, 4
	T_A	–40	105	°C	4, 5

Notes:
1. MAX storage case temperature T_{STG} is measured in the center of the package, as shown in Figure 10. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15, "Recommended Soldering Parameters."
2. MAX operating case temperature T_C is measured in the center of the package, as shown in Figure 10.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. Both temperature specifications must be satisfied.
5. Operating ambient temperature surrounding the package.

Figure 10: Example Temperature Test Point Location



Lmm x Wmm FBGA

Table 7: Thermal Impedance

Die Revision	Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)
F[1]	60-ball	2-layer	71.4	54.1	47.5	33.7	5.5
		4-layer	53.6	44.5	40.5	33.5	
	84-ball	2-layer	65.8	50.4	44.3	30.7	4.1
		4-layer	50.0	41.3	37.7	30.5	

Table 7: Thermal Impedance (Continued)

Die Revision	Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)
G[1]	60-ball	2-layer	94.2	76.5	70.1	57.3	6.1
		4-layer	76.4	66.9	63.1	56.5	
	84-ball	2-layer	88.8	71.3	65.6	52.5	6.0
		4-layer	71.4	62.1	58.7	52.0	

Note: 1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Electrical Specifications – I_{DD} Parameters

I_{DD} Specifications and Conditions

Table 8: General I_{DD} Parameters

I_{DD} Parameters	-187E	-25E	-25	-3E	-3	-37E	-5E	Units
CL (I_{DD})	7	5	6	4	5	4	3	^tCK
^tRCD (I_{DD})	13.125	12.5	15	12	15	15	15	ns
^tRC (I_{DD})	58.125	57.5	60	57	60	60	55	ns
^tRRD (I_{DD}) - x4/x8 (1KB)	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns
^tRRD (I_{DD}) - x16 (2KB)	10	10	10	10	10	10	10	ns
^tCK (I_{DD})	1.875	2.5	2.5	3	3	3.75	5	ns
^tRAS MIN (I_{DD})	45	45	45	45	45	45	40	ns
^tRAS MAX (I_{DD})	70,000	70,000	70,000	70,000	70,000	70,000	70,000	ns
^tRP (I_{DD})	13.125	12.5	15	12	15	15	15	ns
^tRFC (I_{DD} - 256Mb)	75	75	75	75	75	75	75	ns
^tRFC (I_{DD} - 512Mb)	105	105	105	105	105	105	105	ns
^tRFC (I_{DD} - 1Gb)	127.5	127.5	127.5	127.5	127.5	127.5	127.5	ns
^tRFC (I_{DD} - 2Gb)	197.5	197.5	197.5	197.5	197.5	197.5	197.5	ns
^tFAW (I_{DD}) - x4/x8 (1KB)	Defined by pattern in on page							ns
^tFAW (I_{DD}) - x16 (2KB)	Defined by pattern in on page							ns

I_{DD7} Conditions

The detailed timings are shown below for I_{DD7}. Where general I_{DD} parameters in the General Parameters Table conflict with pattern requirements in the I_{DD7} Timing Patterns Table, then the I_{DD7} timing patterns requirements take precedence.

Table 9: I_{DD7} Timing Patterns (4-Bank Interleave READ Operation)

Speed Grade	I_{DD7} Timing Patterns
Timing patterns for 4-bank x4/x8/x16 devices	
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D
-37E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D
-3	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D
-3E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D
-25	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D D
-25E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D
-187E	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D D

Notes:
1. A = active; RA = read auto precharge; D = deselect.
2. All banks are being interleaved at ^tRC (I_{DD}) without violating ^tRRD (I_{DD}) using a BL = 4.
3. Control and address bus inputs are stable during DESELECTs.

Table 10: DDR2 I_{DD} Specifications and Conditions (Die Revision F)

Notes: 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-25E/ -25	-3E/-3	-37E	-5E	Units
Operating one bank active-precharge current: $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; address bus inputs are switching; Data bus inputs are switching	I_{DD0}	x4, x8	100	90	80	80	mA
		x16	135	120	110	110	
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN (I_{DD}), $^tRCD = {}^tRCD (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; address bus inputs are switching; Data pattern is same as I_{DD4W}	I_{DD1}	x4, x8	115	105	95	90	mA
		x16	165	150	135	130	
Precharge power-down current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2P}	x4, x8, x16	7	7	7	7	mA
Precharge quiet standby current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2Q}	x4, x8	50	45	40	35	mA
		x16	65	55	45	40	
Precharge standby current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD2N}	x4, x8	55	50	45	40	mA
		x16	70	60	50	45	
Active power-down current: All banks open; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD3Pf}	Fast PDN exit MR12 = 0	40	35	30	25	mA
	I_{DD3Ps}	Slow PDN exit MR12 = 1	12	12	12	12	
Active standby current: All banks open; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD3N}	x4, x8	70	65	55	45	mA
		x16	75	70	60	50	
Operating burst write current: All banks open, continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; address bus inputs are switching; Data bus inputs are switching	I_{DD4W}	x4, x8	195	170	140	115	mA
		x16	295	250	205	160	