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DDR2 SDRAM

MT47H128M4 – 32 Meg x 4 x 4 Banks
MT47H64M8 – 16 Meg x 8 x 4 Banks
MT47H32M16 – 8 Meg x 16 x 4 Banks

Features

- RoHS compliant
- V_{DD} = +1.8V ±0.1V, $V_{DD}Q$ = +1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 4 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Selectable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Automotive temperature (AT) option
- Supports JEDEC clock jitter specification

Options — Marking

- Configuration
  - 128 Meg x 4 (32 Meg x 4 x 4 banks) — 128M4
  - 64 Meg x 8 (16 Meg x 8 x 4 banks) — 64M8
  - 32 Meg x 16 (8 Meg x 16 x 4 banks) — 32M16
- FBGA package (Pb-free)
  - 84-ball FBGA (12mm x 12.5mm) Rev. B — CC
  - 84-ball FBGA (10mm x 12.5mm) Rev. D — BN
  - 84-ball FBGA (8mm x 12.5mm) Rev. F — HR
  - 60-ball FBGA (12mm x 10mm) Rev. B — CB
  - 60-ball FBGA (10mm x 10mm) Rev. D — B6
  - 60-ball FBGA (8mm x 10mm) Rev. F — CF
- FBGA package (with lead)
  - 84-ball FBGA (12mm x 12.5mm) Rev. B — GC
  - 84-ball FBGA (10mm x 12.5mm) Rev. D — FN
  - 84-ball FBGA (8mm x 12.5mm) Rev. F — HW
  - 60-ball FBGA (12mm x 10mm) Rev. B — GB
  - 60-ball FBGA (10mm x 10mm) Rev. D — F6
  - 60-ball FBGA (8mm x 10mm) Rev. F — JN
- Timing – cycle time
  - 2.5ns @ CL = 5 (DDR2-800) — -25E
  - 2.5ns @ CL = 6 (DDR2-800) — -25
  - 3.0ns @ CL = 4 (DDR2-667) — -3E
  - 3.0ns @ CL = 5 (DDR2-667) — -3
  - 3.75ns @ CL = 4 (DDR2-533) — -37E[1]
  - 5.0ns @ CL = 3 (DDR2-400) — -5E[1]
- Self refresh
  - Standard — None
  - Low-power — L
- Operating temperature
  - Commercial (0°C ≤ T_C ≤ 85°C) — None
  - Industrial (–40°C ≤ T_C ≤ 95°C; –40°C ≤ T_A ≤ 85°C) — IT
  - Automotive, Revision :D only (–40°C ≤ T_C, T_A ≤ 105°C) — AT
- Revision — :B[1]/:D[1]/:F

Notes: 1. Not recommended for new designs

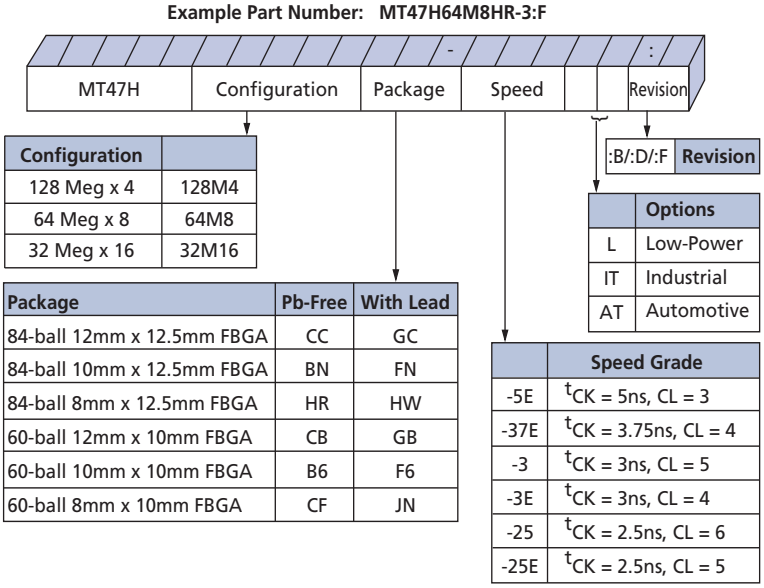
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)					^tRC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	CL = 7	
-25E	400	533	800	800	–	55
-25	400	533	667	800	–	55
-3E	400	667	667	–	–	54
-3	400	533	667	–	–	55
-37E	400	533	–	–	–	55
-5E	400	400	–	–	–	55

Table 2: Addressing

Parameter	128 Meg x 4	64 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	A0–A13 (16K)	A0–A13 (16K)	A0–A12 (8K)
Bank address	BA0–BA1 (4)	BA0–BA1 (4)	BA0–BA1 (4)
Column address	A0–A9, A11 (2K)	A0–A9 (1K)	A0–A9 (1K)

Figure 1: 512Mb DDR2 Part Numbers



Notes: 1. Not all speeds and configurations are available in all packages.

FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: www.micron.com.

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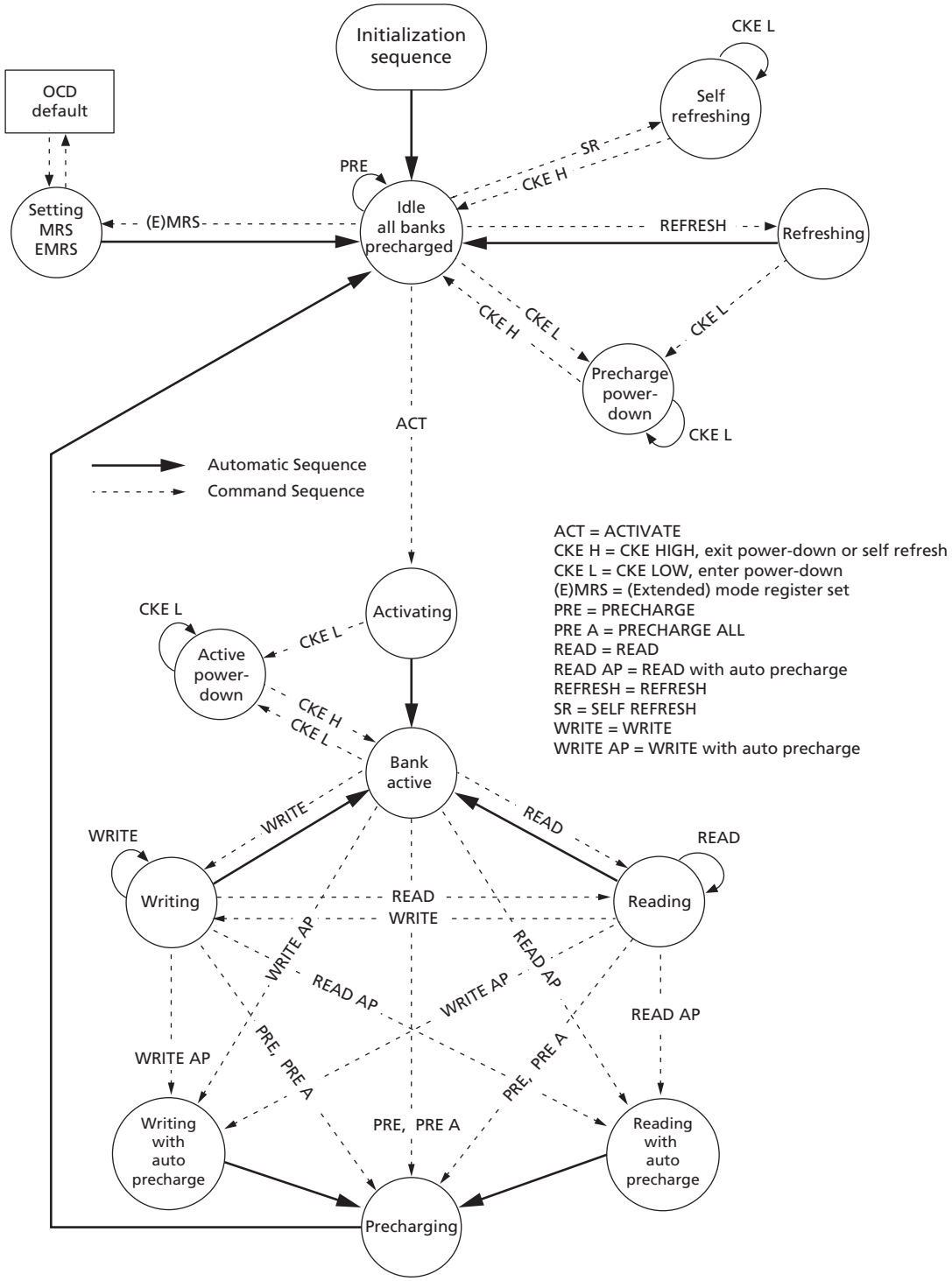
State Diagram

Figure 2: Simplified State Diagram



Notes: 1. This diagram provides the basic command flow. It is not comprehensive and does not identify all timing requirements or possible command restrictions such as multibank interaction, power down, entry/exit, etc.

Functional Description

The DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable READ or WRITE burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst READ of eight with another READ or a burst WRITE of eight with another WRITE. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Industrial Temperature

The industrial temperature (IT) option, if offered, has two simultaneous requirements: ambient temperature surrounding the device cannot be less than –40°C or greater than +85°C, and the case temperature cannot be less than –40°C or greater than +95°C. JEDEC specifications require the refresh rate to double when T_C exceeds +85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is < 0°C or > +85°C.

Automotive Temperature

The automotive temperature (AT) option, if offered, has two simultaneous requirements: ambient temperature surrounding the device cannot be less than –40°C or greater than +105°C, and the case temperature cannot be less than –40°C or greater than +105°C. JEDEC specifications require the refresh rate to double when T_C exceeds +85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is < 0°C or > +85°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

Functional Block Diagrams

The DDR2 SDRAM is a high-speed CMOS, dynamic random access memory. It is internally configured as a multi-bank DRAM.

Figure 3: 128 Meg x 4 Functional Block Diagram

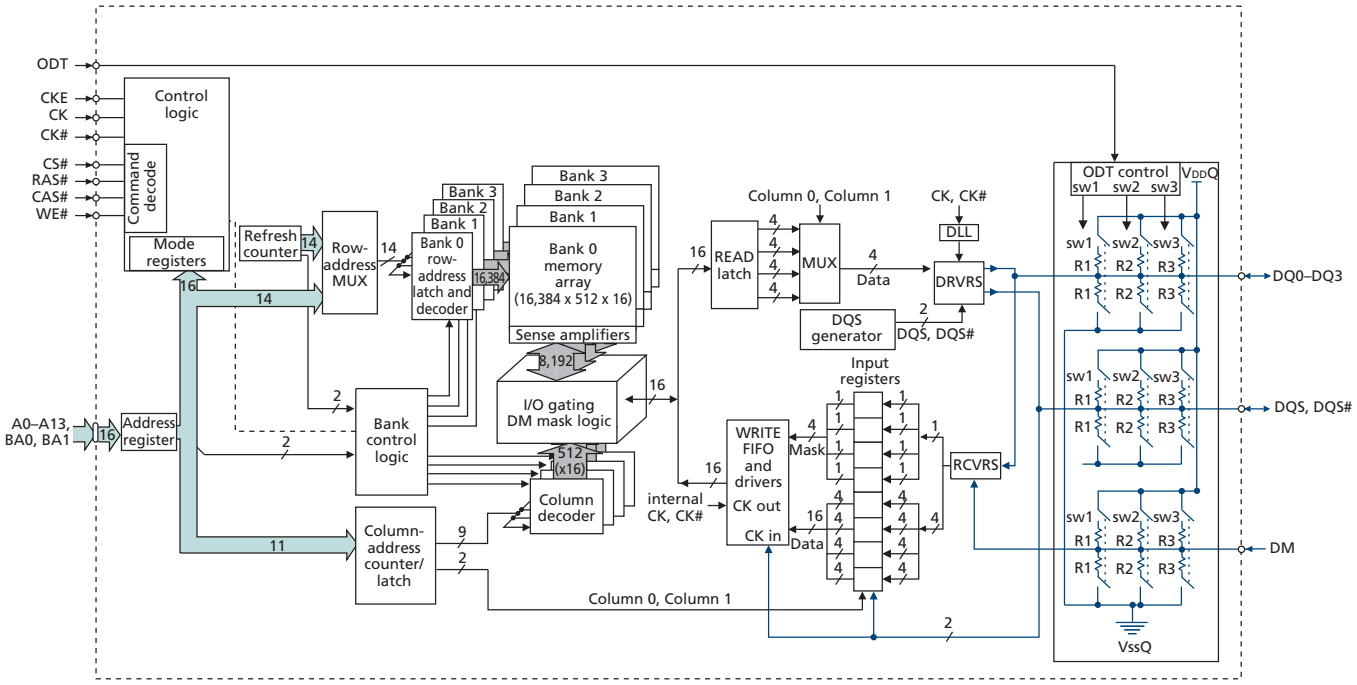


Figure 4: 64 Meg x 8 Functional Block Diagram

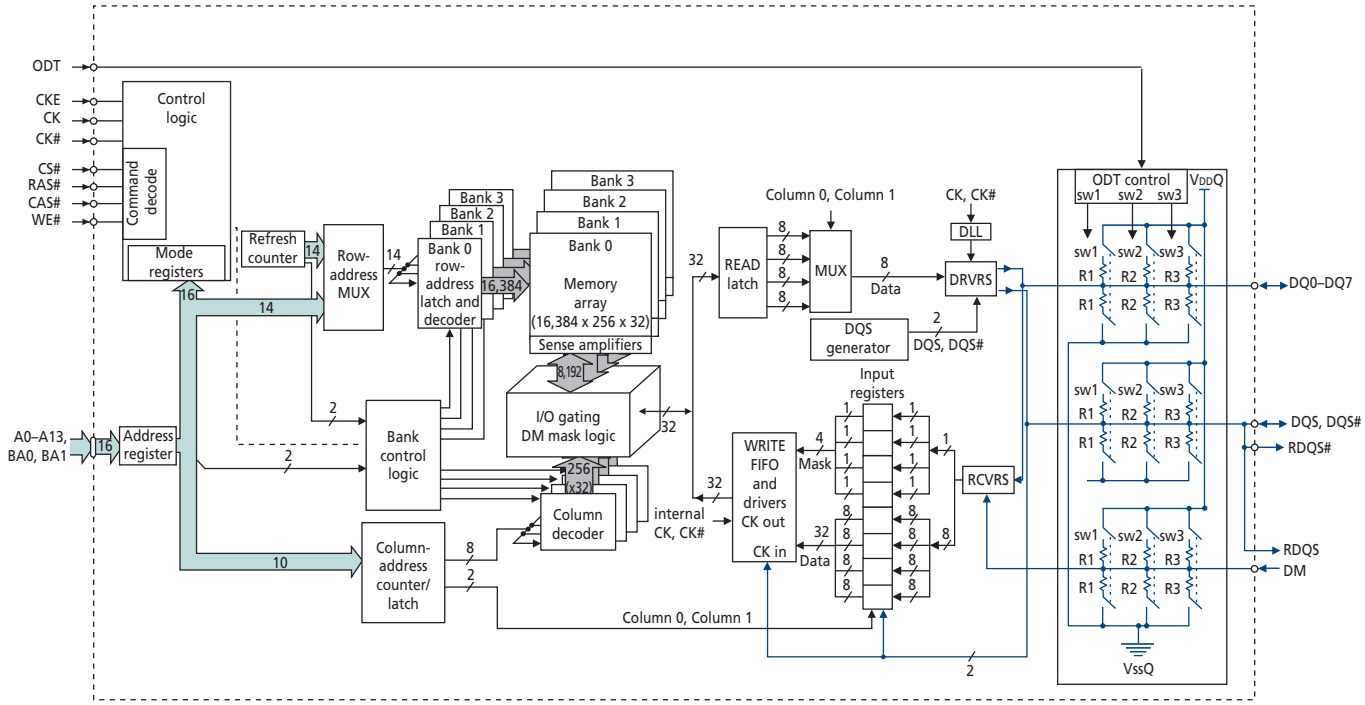
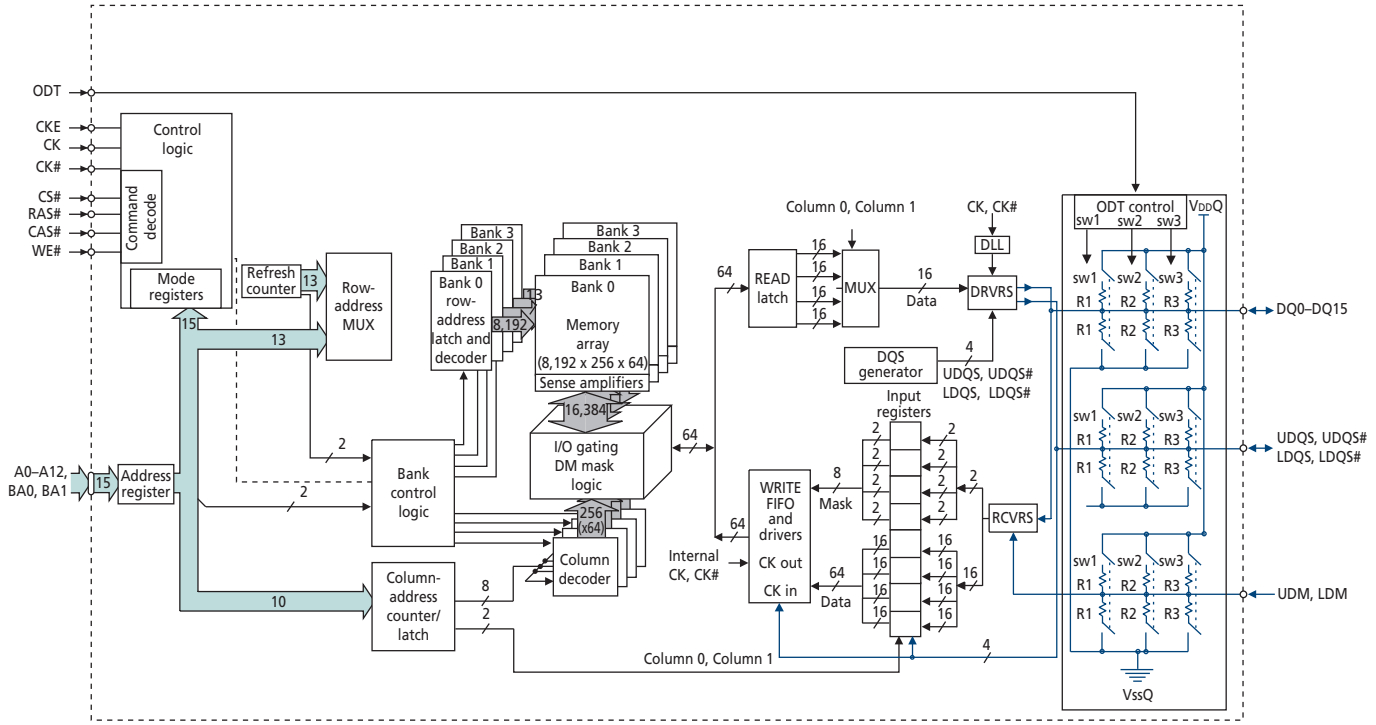


Figure 5: 32 Meg x 16 Functional Block Diagram



Ball Assignments and Descriptions

Figure 6: 60-Ball FBGA – x4, x8 Ball Assignments (Top View)

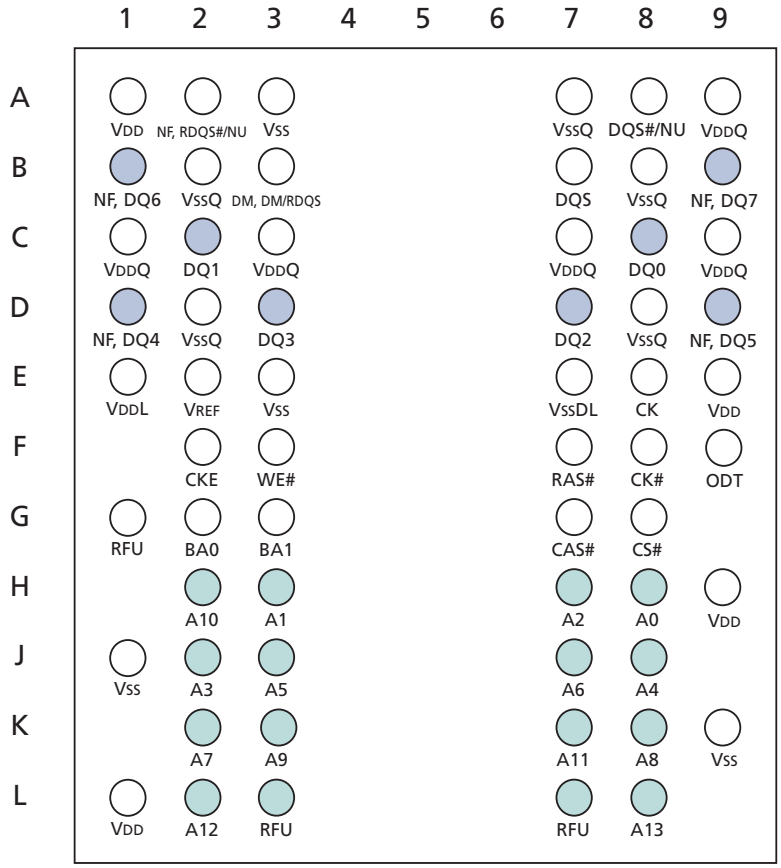


Figure 7: 84-Ball FBGA – x16 Ball Assignments (Top View)

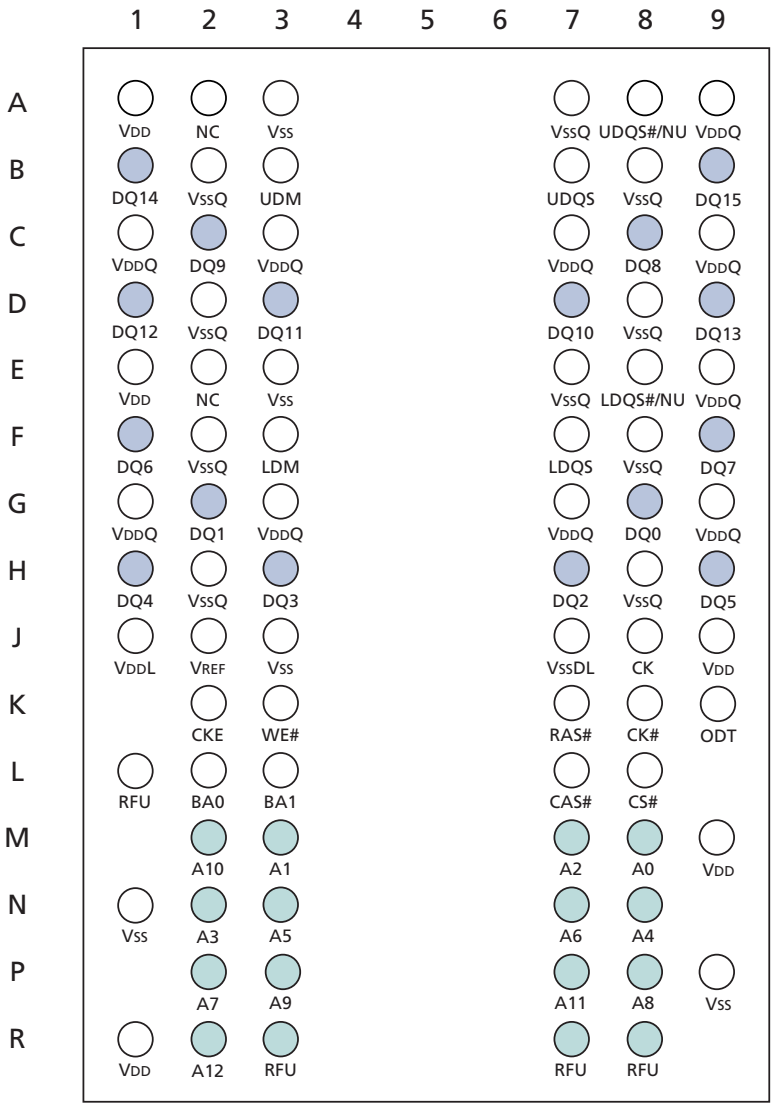


Table 3: FBGA 60-Ball – x4, x8 and 84-Ball – x16 Descriptions

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
M8, M3, M7, N2, N8, N3, N7, P2, P8, P3, M2, P7, R2	–	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0–BA2) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
–	H8, H3, H7, J2, J8, J3, J7, K2, K8, K3, H2, K7, L2, L8	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0–BA2) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
L2, L3	G2, G3,	BA0, BA1	Input	**Bank address inputs:** BA0–BA1 define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
J8, K8	E8, F8	CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
K2	F2	CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, OUTPUT DISABLE, and for self refresh entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, V_{REF} must be maintained.
L8	G8	CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code.

Table 3: FBGA 60-Ball – x4, x8 and 84-Ball – x16 Descriptions (continued)

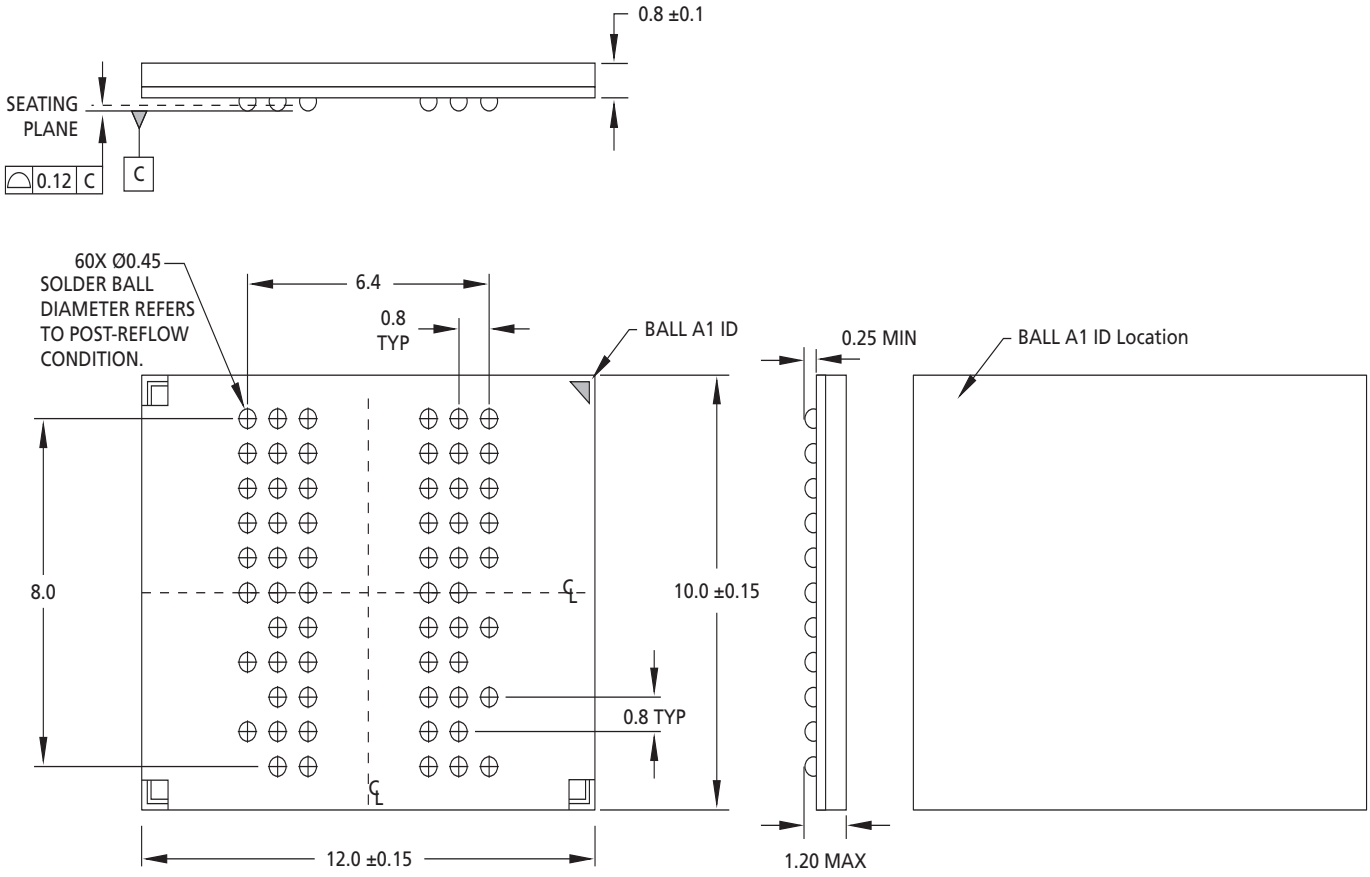
x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
F3, B3	B3	LDM, UDM DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a WRITE access. DM is sampled on both edges of DQS. Although the DM balls are input-only, the DM loading is designed to match that of the DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
K9	F9	ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (resgistered LOW) termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
K7, L7, K3	F7, G7, F3	RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.
G8, G2, H7, H3, H1, H9, F1, F9, C8, C2, D7, D3, D1, D9, B1, B9	–	DQ0–DQ2, DQ3–DQ5, DQ6–DQ8, DQ9–DQ11, DQ12–DQ14, DQ15	I/O	**Data input/output:** Bidirectional data bus for 32 Meg x 16.
–	C8, C2, D7, D3, D1, D9, B1, B9	DQ0–DQ2, DQ3–DQ5, DQ6–DQ7	I/O	**Data input/output:** Bidirectional data bus for 64 Meg x 8.
–	C8, C2, D7, D3	DQ0–DQ2, DQ3	I/O	**Data input/output:** Bidirectional data bus for 128 Meg x 4.
–	B7, A8	DQS, DQS#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
F7, E8	–	LDQS, LDQS#	I/O	**Data strobe for lower byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
B7, A8	–	UDQS, UDQS#	I/O	**Data strobe for upper byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	B3, A2	RDQS, RDQS#	Output	**Redundant data strobe:** For 64 Meg x 8 only. RDQS is enabled/disabled via the load mode command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball B3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled and differential data strobe mode is enabled.

Table 3: FBGA 60-Ball – x4, x8 and 84-Ball – x16 Descriptions (continued)

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
A1, E1, M9, R1, J9	A1, E9, L1, H9	VDD	Supply	**Power supply:** 1.8V ±0.1V.
A9, C1, C3, C7, C9, G3, E9, G1, G7, G9	A9, C1, C3, C7, C9	VDDQ	Supply	**DQ power supply:** 1.8V ±0.1V. Isolated on the device for improved noise immunity.
J1	E1	VDDL	Supply	**DLL power supply:** 1.8V ±0.1V.
J2	E2	VREF	Supply	SSTL_18 reference voltage (VDDQ/2).
A3, E3, J3, N1, P9	A3, E3, J1, K9	VSS	Supply	Ground.
J7	E7	VSSDL	Supply	**DLL ground:** Isolated on the device from VSS and VSSQ.
A7, B2, B8, D2, D8, E7, F2, F8, H2, H8	A7, B2, B8, D2, D8	VSSQ	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
A2, E2	–	NC	–	**No connect:** These balls should be left unconnected.
–	B1, B9, D1, D9	NF	–	**No function:** x8: these balls are used as DQ4–DQ7; x4: they are no function.
A8, E8	A2, A8	NU	–	**Not used:** If EMR(E10) = 0: x16, A8 = UDQS# and E8 = LDQS#; x8, A2 = RDQS# and A8 = DQS#; x4, A2 = NU and A8 = NU. If EMR(E10) = 1: x16, A8 = NU and E8 = NU; x8, A2 = NU and A8 = NU; x4, A2 = NU and A8 = NU.
L1, R8, R3, R7	G1, L3, L7	RFU	–	**Reserved for future use:** Bank address BA2. Row address bits A13 (x16 only), A14, and A15.

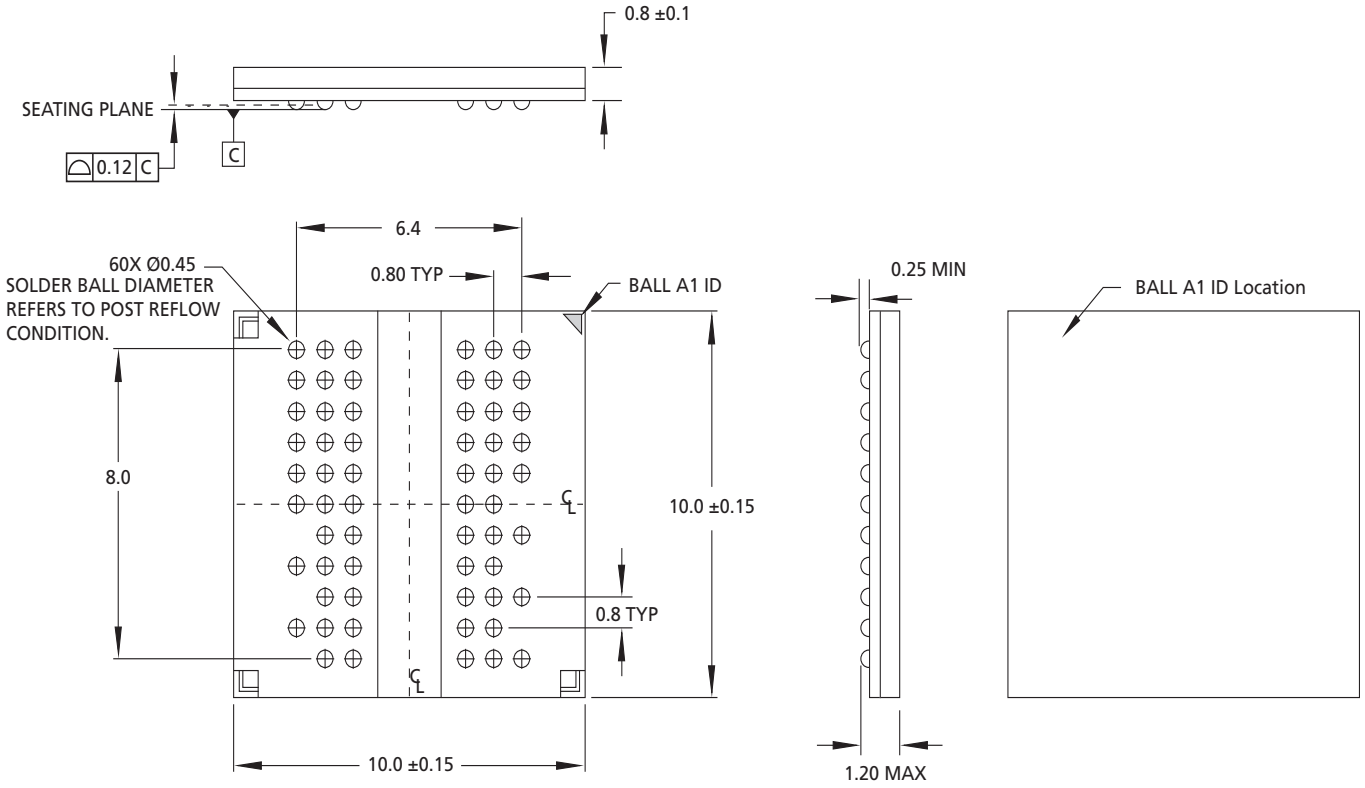
Package Dimensions

Figure 8: 60-Ball FBGA (12mm x 10mm) – x4, x8



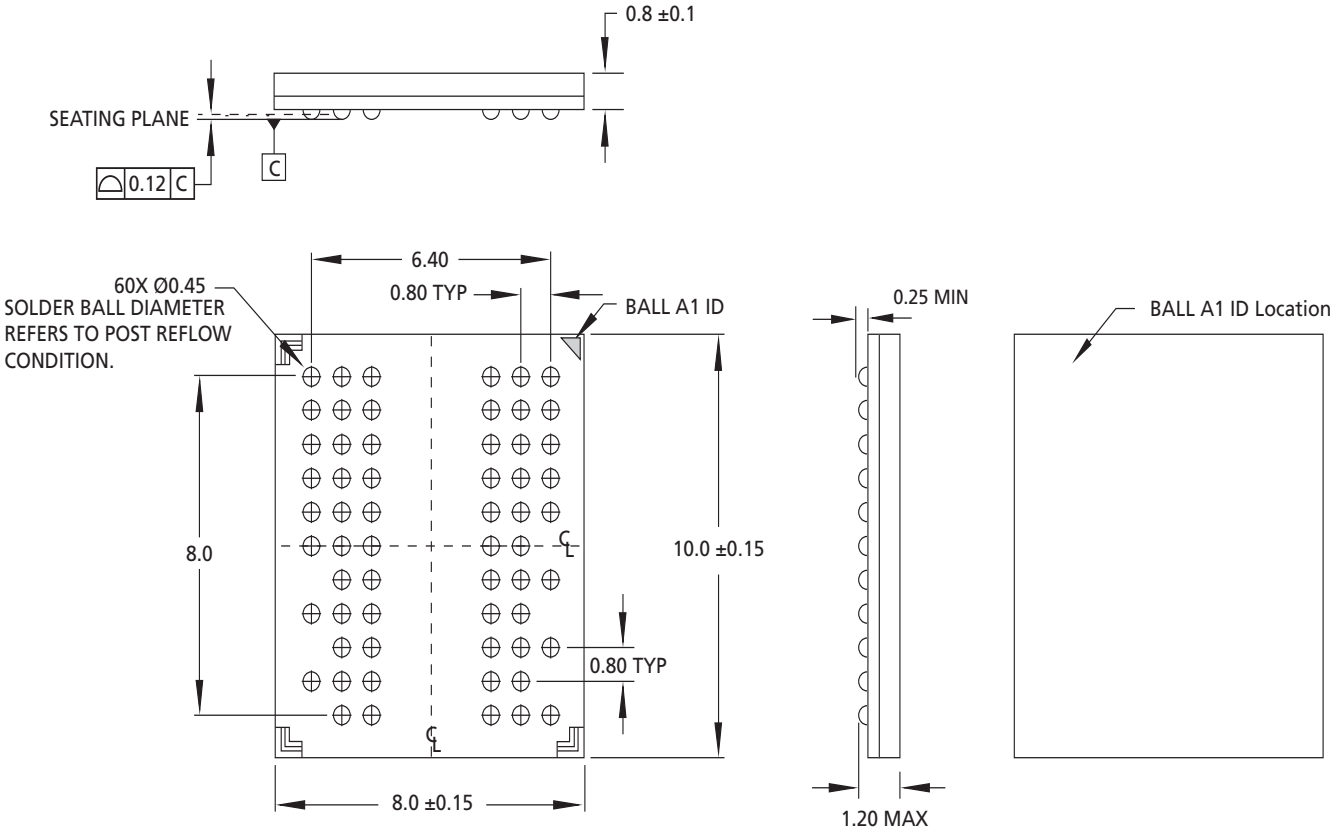
Notes: 1. All dimensions are in millimeters.

Figure 9: 60-Ball FBGA (10mm x 10mm) – x4, x8



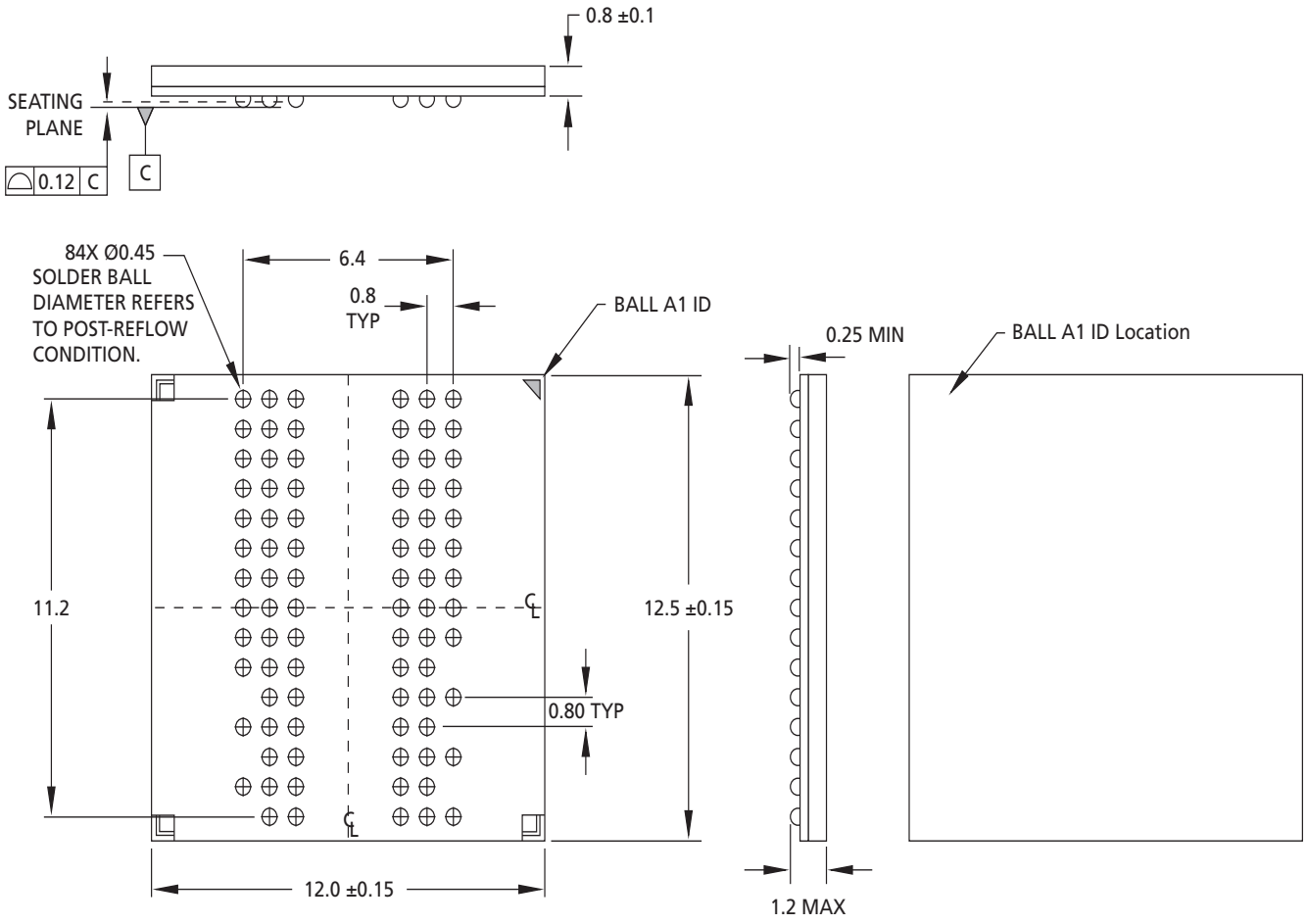
Notes: 1. All dimensions are in millimeters.

Figure 10: 60-Ball FBGA (8mm x 10mm) – x4, x8



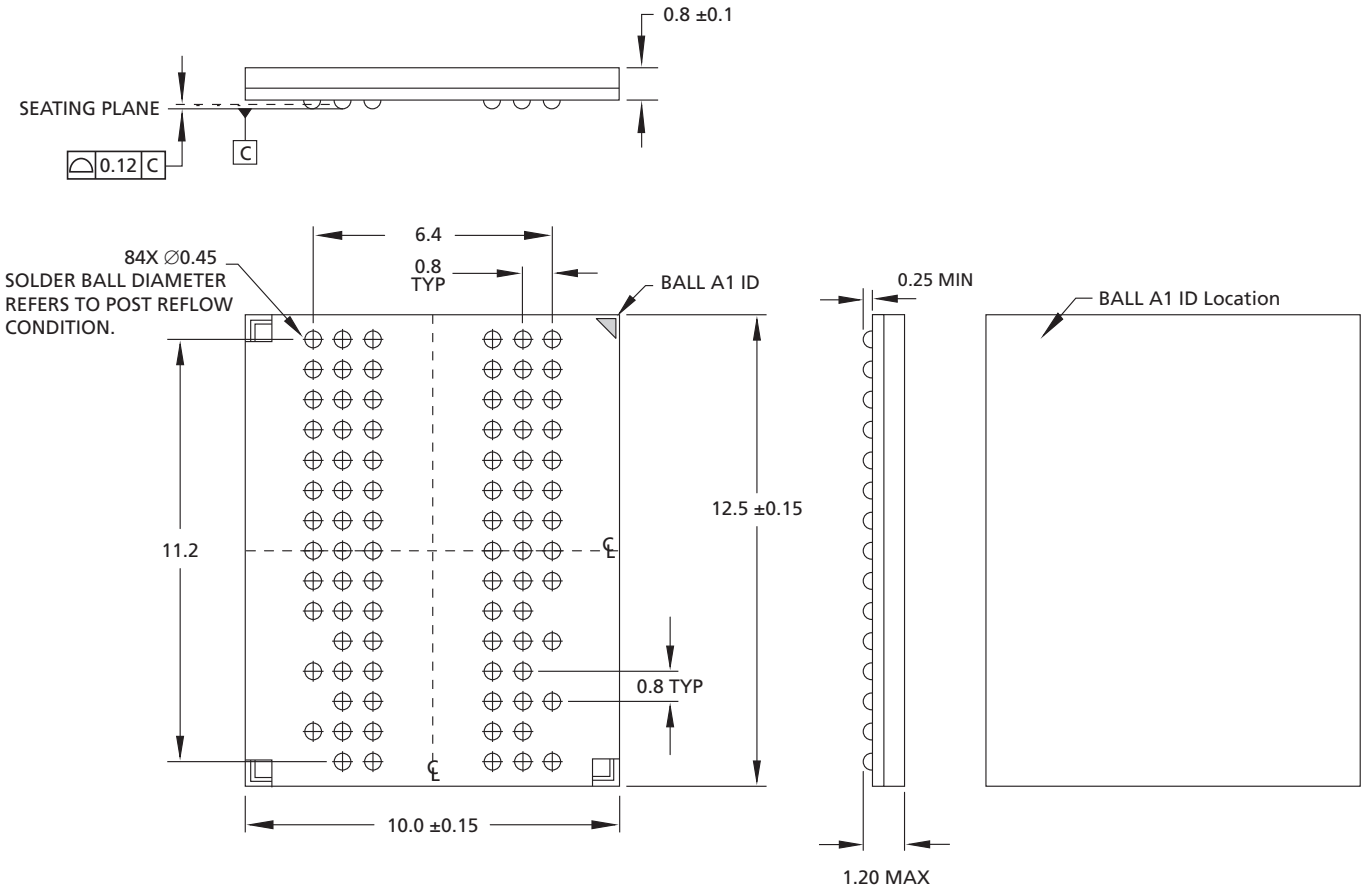
Notes: 1. All dimensions are in millimeters.

Figure 11: 84-Ball FBGA (12mm x 12.5mm) – x16



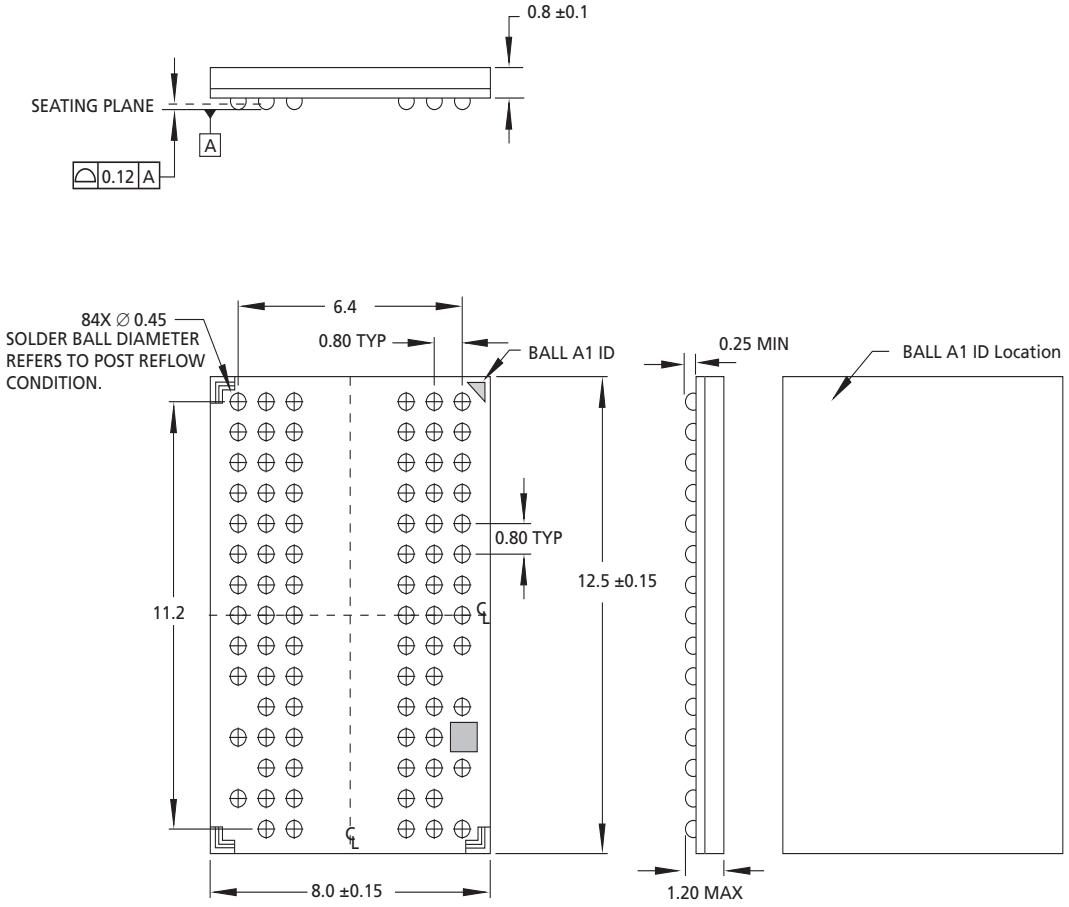
Notes: 1. All dimensions are in millimeters.

Figure 12: 84-Ball FBGA (10mm x 12.5mm) – x16



Notes: 1. All dimensions are in millimeters.

Figure 13: 84-Ball FBGA (8mm x 12.5mm) – x16



Notes: 1. All dimensions are in millimeters.

FBGA Package Capacitance

Table 4: Input Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance: CK, CK#	C_{CK}	1.0	2.0	pF	1
Delta input capacitance: CK, CK#	C_{DCK}	–	0.25	pF	2, 3
Input capacitance: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, ODT	C_I	1.0	2.0	pF	1, 4
Delta input capacitance: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, ODT	C_{DI}	–	0.25	pF	2, 3
Input/output capacitance: DQ, DQS, DM, NF	C_{IO}	2.5	4.0	pF	1, 5
Delta input/output capacitance: DQ, DQS, DM, NF	C_{DIO}	–	0.5	pF	3, 6

Notes:
1. This parameter is sampled. V_{DD} = +1.8V ±0.1V, $V_{DD}Q$ = +1.8V ±0.1V, V_{REF} = V_{SS}, *f* = 100 MHz, T_C = 25°C, $V_{OUT(DC)}$ = $V_{DD}Q/2$, V_{OUT} (peak-to-peak) = 0.1V. DM input is grouped with I/O balls, reflecting the fact that they are matched in loading.
2. The input capacitance per ball group will not differ by more than this maximum amount for any given device.
3. ΔC are not pass/fail parameters but rather targets.
4. Reduce MAX limit by 0.25pF for -25, -25E speed devices.
5. Reduce MAX limit by 0.5pF for -3, -3E, -25, -25E speed devices.
6. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

Electrical Specifications – Absolute Ratings

Stresses greater than those listed in Table 5 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions oustide those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 5: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–1.0	+2.3	V	1
$V_{DD}Q$ supply voltage relative to $V_{SS}Q$	$V_{DD}Q$	–0.5	+2.3	V	1, 2
$V_{DD}L$ supply voltage relative to $V_{SS}L$	$V_{DD}L$	–0.5	+2.3	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	+2.3	V	3
Input leakage current; Any input $0V \le V_{IN} \le V_{DD}$; All other balls not under test = 0V	I_I	–5	+5	µA	
Output leakage current; $0V \le V_{OUT} \le V_{DD}Q$; DQ and ODT disabled	I_{OZ}	–5	+5	µA	
V_{REF} leakage current; V_{REF} = Valid V_{REF} level	I_{VREF}	–2	+2	µA	

Notes:
1. V_{DD}, $V_{DD}Q$, and $V_{DD}L$ must be within 300mV of each other at all times.
2. $V_{REF} \le 0.6 \times V_{DD}Q$; however, V_{REF} may be $\ge V_{DD}Q$ provided that $V_{REF} \le 300mV$.
3. Voltage on any I/O may not exceed voltage on $V_{DD}Q$.

Temperature and Thermal Impedance

It is imperative that the DDR2 SDRAM device's temperature specifications, shown in Table 6 on page 23, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 7 on page 24 for the applicable and available die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the thermal impedances listed in Table 7 on page 24. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

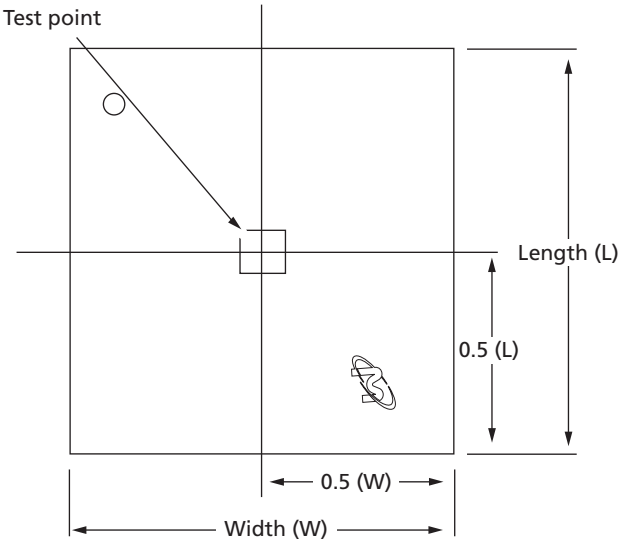
The DDR2 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

Table 6: Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	T_{STG}	–55	+150	°C	1
Operating temperature: commercial	T_C	0	+85	°C	2, 3
Operating temperature: industrial	T_C	–40	+95	°C	2, 3, 4
	T_A	–40	+85	°C	4, 5
Operating temperature: automotive	T_C	–40	+105	°C	2, 3, 4
	T_A	–40	+105	°C	4, 5

Notes:
1. MAX storage case temperature; T_{STG} is measured in the center of the package, as shown in Figure 14. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15, "Recommended Soldering Parameters."
2. MAX operating case temperature; T_C is measured in the center of the package, as shown in Figure 14.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. Both temperature specifications must be satisfied.
5. Operating ambient temperature surrounding the package.

Figure 14: Example Temperature Test Point Location



Lmm x Wmm FGBA

Table 7: Thermal Impedance

Die Revision	Package	Substrate	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)	Notes
B	60-ball	2-layer	53.2	40.0	37.2	27.5	2.9	1
		4-layer	37.4	30.9	27.7	24.2		
	84-ball	2-layer	50.2	36.8	32.1	24.5	3.1	
		4-layer	34.9	28.0	25.5	21.3		
D	60-ball	2-layer	56.9	43.6	38.5	30.6	3.8	1
		4-layer	40.6	34.1	31.3	27.0		
	84-ball	2-layer	56.8	42.8	37.7	24.8	3.9	
		4-layer	40.3	33.2	30.4	23.5		
F	60-ball	2-layer	71.4	54.1	47.5	33.7	5.5	1
		4-layer	53.6	44.5	40.5	33.5		
	84-ball	2-layer	65.8	50.4	44.3	30.7	4.1	
		4-layer	50	41.3	37.7	30.5		
Last shrink target	60-ball	2-layer	72	55	48	34	5.5	2
		4-layer	54	45	41	34		
	84-ball	2-layer	66	52	45	32	4.5	
		4-layer	50	42	39	32		

Notes:
1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. This is an estimate; simulated number and actual results could vary.

Electrical Specifications – IDD Parameters

IDD Specifications and Conditions

Table 8: General IDD Parameters

IDD Parameters	-187E	-25E	-25	-3E	-3	-37E	-5E	Units
CL (IDD)	7	5	6	4	5	4	3	tCK
tRCD (IDD)	13.125	12.5	15	12	15	15	15	ns
tRC (IDD)	58125	57.5	60	57	60	60	55	ns
tRRD (IDD) - x4/x8 (1KB)	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns
tRRD (IDD) - x16 (2KB)	10	10	10	10	10	10	10	ns
tCK (IDD)	1.875	2.5	2.5	3	3	3.75	5	ns
tRAS MIN (IDD)	45	45	45	45	45	45	40	ns
tRAS MAX (IDD)	70,000	70,000	70,000	70,000	70,000	70,000	70,000	ns
tRP (IDD)	13.125	12.5	15	12	15	15	15	ns
tRFC (IDD)	105	105	105	105	105	105	105	ns
tFAW (IDD) - x4/x8	Pattern determined by Table 9 on page 25							ns
tFAW (IDD) - x16	Pattern determined by Table 9 on page 25							ns

IDD7 Conditions

Detailed IDD7 timings are shown below. Where general IDD parameters in Table 8 on page 25 conflict with pattern requirements of Table 9, then Table 9 requirements take precedence.

Table 9: IDD7 Timing Patterns (4-Bank Interleave READ Operation)

Speed Grade	IDD7 Timing Patterns
Timing patterns for 4-bank x4/x8/x16 devices	
-187E	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D
-25E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D
-25	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D
-3E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D
-3	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D
-37E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D

Notes:
1. A = ACTIVATE; RA = READ with auto precharge; D = DESELECT.
2. All banks are being interleaved at tRC (IDD) without violating tRRD (IDD) using a BL = 4.
3. Control and address bus inputs are stable during DESELECTs.