Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Mobile Low-Power SDR SDRAM

MT48H32M16LF – 8 Meg x 16 x 4 banks
MT48H16M32LF/LG – 4 Meg x 32 x 4 banks

Features

- V_{DD}/V_{DDQ} = 1.7–1.95V
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable burst lengths: 1, 2, 4, 8, and continuous
- Auto precharge, includes concurrent auto precharge
- Auto refresh and self refresh modes
- LVTTL-compatible inputs and outputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive strength (DS)
- 64ms refresh period

Options	Marking
• V_{DD}/V_{DDQ}: 1.8V/1.8V	H
• Addressing	
– Standard addressing option	LF
– Reduced page-size option[1]	LG
• Configuration	
– 32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
– 16 Meg x 32 (4 Meg x 32 x 4 banks)	16M32
• Plastic “green” packages	
– 54-ball VFBGA (8mm x 9mm)[2]	BF
– 90-ball VFBGA (10mm x 13mm)[3]	CM
• Timing – cycle time	
– 6ns at CL = 3	-6
– 7.5ns at CL = 3	-75
• Power	
– Standard I_{DD2}/I_{DD7}	None
– Low-power I_{DD2}/I_{DD7}[1]	L
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
• Revision	:B

Notes: 1. Contact factory for availability.
2. Available only for x16 configuration.
3. Available only for x32 configuration.

Table 1: Configuration Addressing

Architecture	32 Meg x 16	16 Meg x 32	16 Meg x 32 Reduced Page-Size Option[1]
Number of banks	4	4	4
Bank address balls	BA0, BA1	BA0, BA1	BA0, BA1
Row address balls	A[12:0]	A[12:0]	A[13:0]
Column address balls	A[9:0]	A[8:0]	A[7:0]

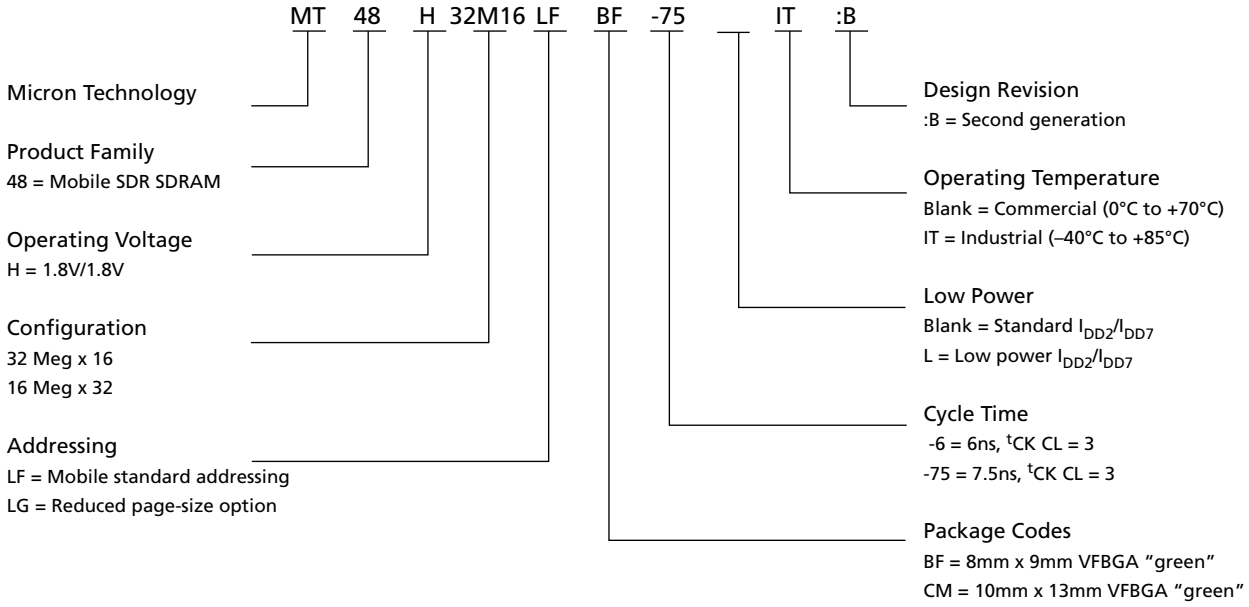
Note: 1. Contact factory for availability

Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz)		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-6	104	166	8ns	5ns
-75	104	133	8ns	5.4ns

Note: 1. CL = CAS (READ) latency

Figure 1: 512Mb Mobile LPSDR Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Contents

List of Tables

List of Figures

General Description

The 512Mb Mobile LPSDR is a high-speed CMOS, dynamic random-access memory containing 536,870,912-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1K columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits. In a reduced page-size option, each of the x32's 134,217,728-bit banks is organized as 16,384 rows by 256 columns x32 bits.

Mobile LPSDR offers substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Note:

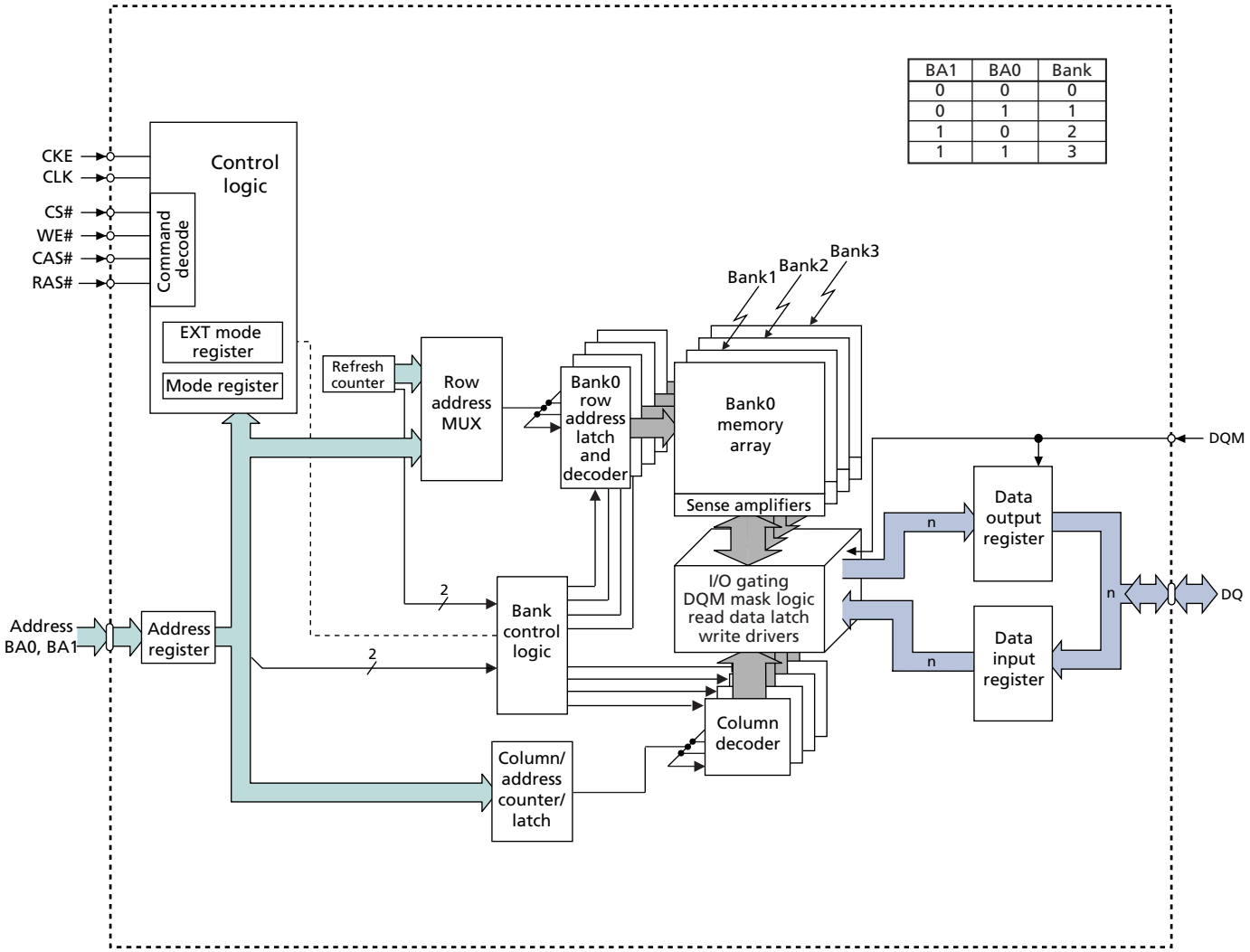
1. Throughout the data sheet, various figures and text refer to DQs as DQ. DQ should be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DQM refers to LDQM. For the upper byte (DQ[15:8]), DQM refers to UDQM. The x32 is divided into four bytes. For DQ[7:0], DQM refers to DQM0. For DQ[15:8], DQM refers to DQM1. For DQ[23:16], DQM refers to DQM2, and for DQ[31:24], DQM refers to DQM3.

2. Complete functionality is described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

3. Any specific requirement takes precedence over a general statement.

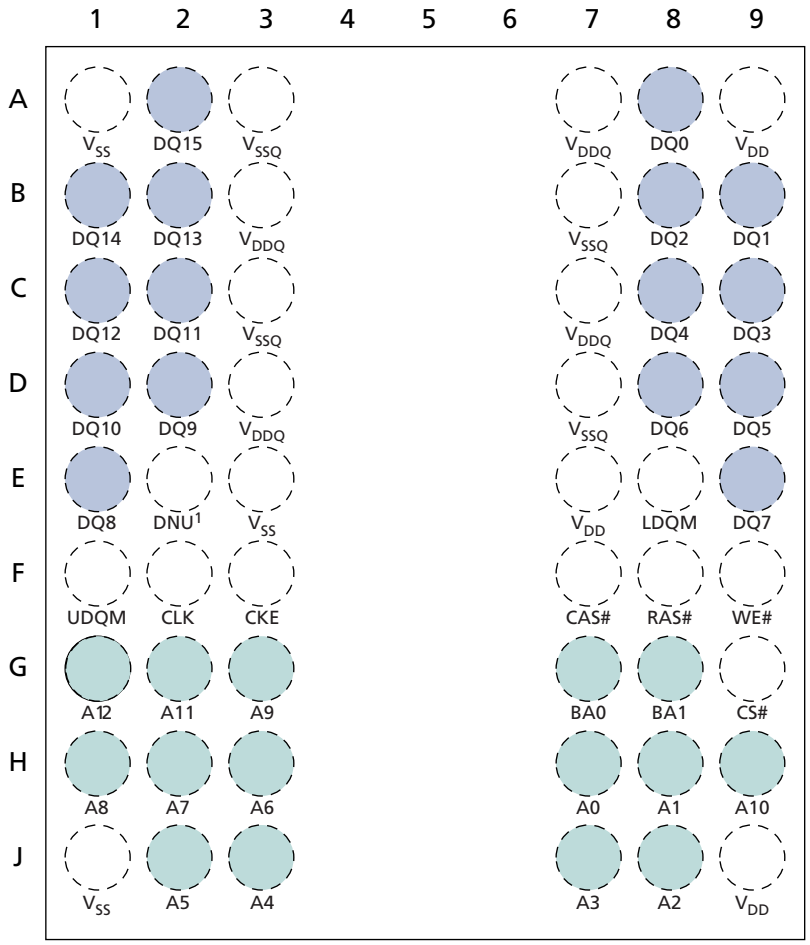
Functional Block Diagram

Figure 2: Functional Block Diagram



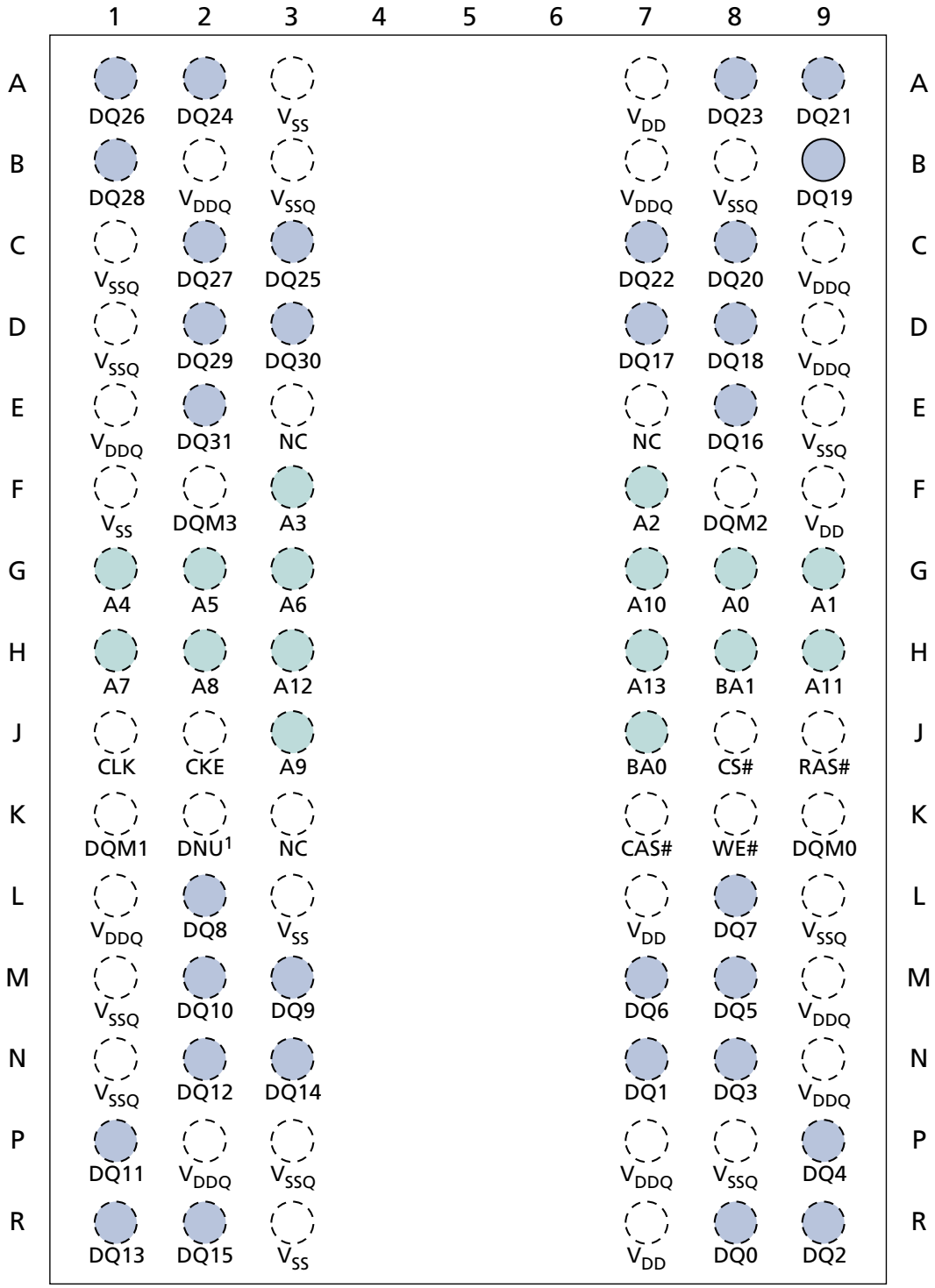
Ball Assignments and Descriptions

Figure 3: 54-Ball VFBGA (Top View)



Note: 1. The E2 pin must be connected to V_{SS}, V_{SSQ}, or left floating.

Figure 4: 90-Ball VFBGA (Top View)



Note: 1. The K2 pin must be connected to V_{SS}, V_{SSQ}, or left floating.

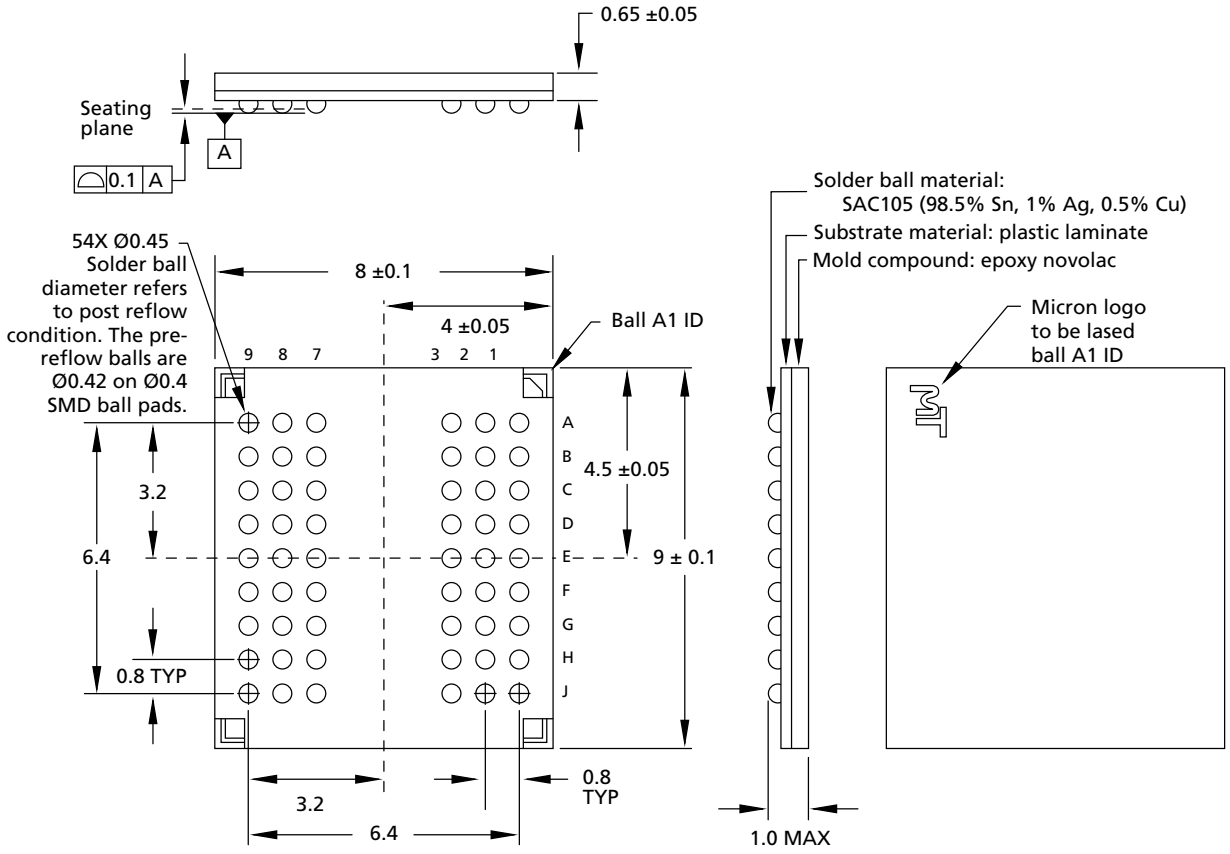
Table 3: VFBGA Ball Descriptions

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
LDQM,UDQM(54-ball) DQM[3:0] (90-ball)	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are High-Z (two-clock latency) during a READ cycle. For the x16, LDQM corresponds to DQ[7:0] and UDQM corresponds to DQ[16:8]. For the x32, DQM0 corresponds to DQ[7:0], DQM1 corresponds to DQ[15:8], DQM2 corresponds to DQ[23:16], and DQM3 corresponds to DQ[31:24]. DQM[3:0] (or LDQM and UDQM if x16) are considered same state when referenced as DQM.
BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 become "Don't Care" when registering an ALL BANK PRECHARGE (A10 HIGH).
A[13:0]	Input	Address inputs: Addresses are sampled during the ACTIVE command (row) and READ/WRITE command [column); column address A[9:0] (x16); with A10 defining auto precharge] to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command. The maximum address range is dependent upon configuration. Unused address pins become RFU.[1]
DQ[31:0]	I/O	Data input/output: Data bus.
V_{DDQ}	Supply	DQ power: Provide isolated power to DQ for improved noise immunity.
V_{SSQ}	Supply	DQ ground: Provide isolated ground to DQ for improved noise immunity.
V_{DD}	Supply	Core power supply.
V_{SS}	Supply	Ground.
DNU	–	Do not use: Must be grounded or left floating.
NC	–	Internally not connected. These balls can be left unconnected but it is recommended that they be connected to V_{SS}.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact the factory for details.

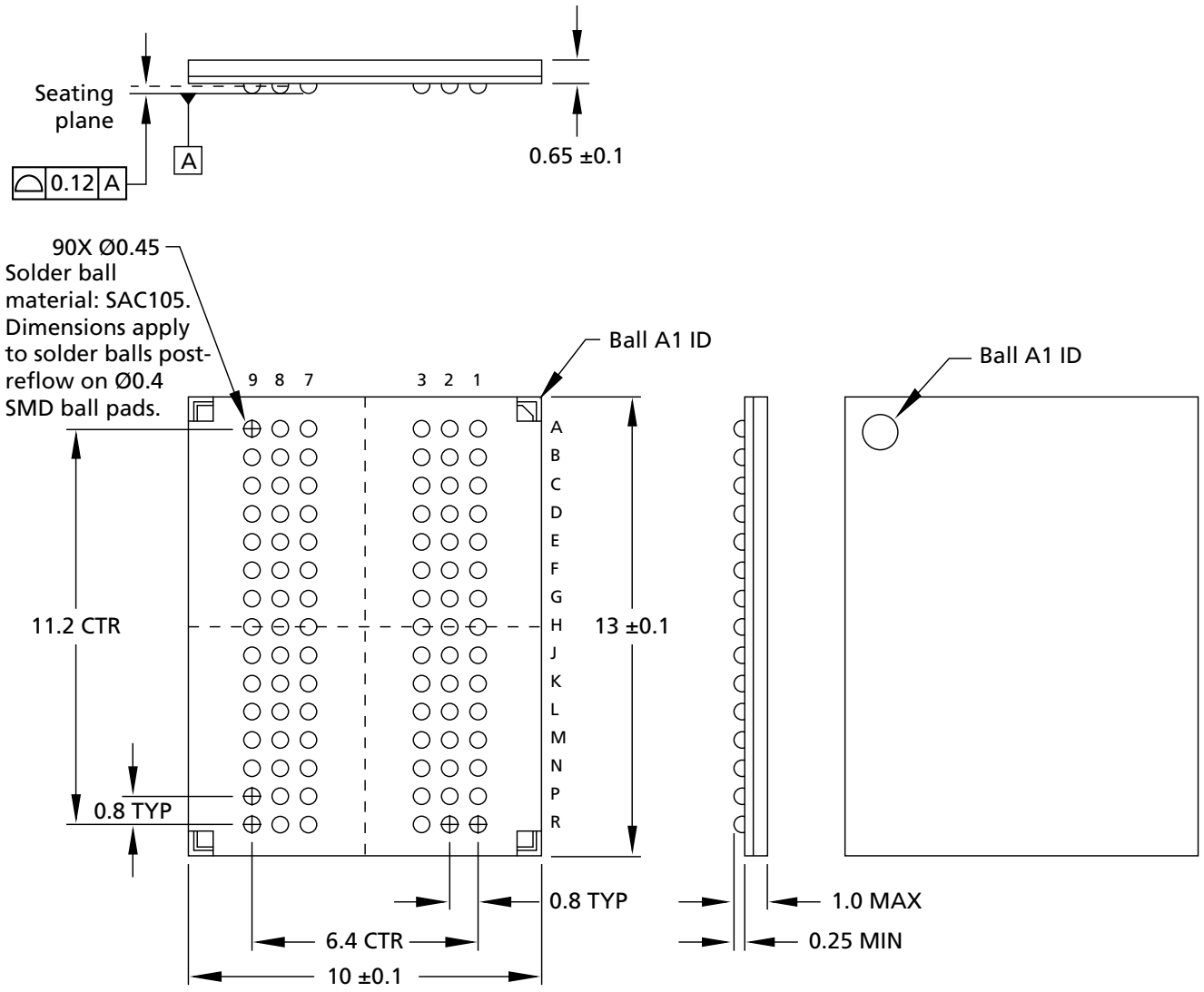
Package Dimensions

Figure 5: 54-Ball VFBGA (8mm x 9mm)



Note: 1. 1. All dimensions are in millimeters.

Figure 6: 90-Ball VFBGA (10mm x 13mm)



Note: 1. 1. All dimensions are in millimeters.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Voltage/Temperature	Symbol	Min	Max	Units
Voltage on V_{DD}/V_{DDQ} supply relative to V_{SS}	V_{DD}/V_{DDQ}1	–0.5	+2.4	V
Voltage on inputs, NC or I/O balls relative to V_{SS}	V_{IN}	–0.5	+2.4	
Storage temperature (plastic)	T_{STG}	–55	+150	°C

Note: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Table 5: DC Electrical Characteristics and Operating Conditions

Notes 1 and 2 apply to all parameters and conditions; V_{DD}/V_{DDQ} = 1.7–1.95V

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		V_{DD}	1.7	1.95	V	
I/O supply voltage		V_{DDQ}	1.7	1.95	V	
Input high voltage: Logic 1; All inputs		V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	3
Input low voltage: Logic 0; All inputs		V_{IL}	–0.3	+0.3	V	3
Output high voltage		V_{OH}	0.9 × V_{DDQ}	–	V	4
Output low voltage		V_{OL}	–	0.2	V	4
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)		I_I	–1.0	1.0	µA	
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}		I_{OZ}	–1.5	1.5	µA	
Operating temperature:	Industrial	T_A	–40	+85	°C	
	Commercial	T_A	0	+70	°C	

Notes:
1. All voltages referenced to V_{SS}.
2. A full initialization sequence is required before proper device operation is ensured.
3. $V_{IH,max}$ overshoot: $V_{IH,max}$ = V_{DDQ} + 2V for a pulse width ≤3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{IL,min}$ = –2V for a pulse width ≤3ns.
4. I_{OUT} = 4mA for full drive strength. Other drive strengths require appropriate scale.

Table 6: Capacitance

Note 1 applies to all parameters and conditions

Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	C_{L1}	2.0	5.0	pF
Input capacitance: All other input-only balls	C_{L2}	2.0	5.0	pF
Input/output capacitance: DQ	C_{L0}	2.5	6.0	pF

Note: 1. This parameter is sampled. V_{DD}, V_{DDQ} = +1.8V; TA = 25°C; ball under test biased at 0.9V, f = 1 MHz.

Electrical Specifications – I_{DD} Parameters

Table 7: I_{DD} Specifications and Conditions (x16)

Note 1 applies to all parameters and conditions; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max		Units	Notes
			-6	-75		
Operating current: Active mode; Burst = 1; READ or WRITE; $^{t}RC = {}^{t}RC$ (MIN)		I_{DD1}	90	80	mA	2, 3, 4
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2P}	300	300	µA	5
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		I_{DD2N}	10	8	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		I_{DD3P}	5	5	mA	3, 4, 6
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3N}	20	18	mA	3, 4, 6
Operating current: Burst mode; READ or WRITE; All banks active, half of DQ toggling every cycle		I_{DD4}	100	90	mA	2, 3, 4
Auto refresh current: CKE = HIGH; CS# = HIGH	^{t}RFC = 110ns	I_{DD5}	100	100	mA	2, 3, 4, 6
	^{t}RFC = 7.8125µs	I_{DD6}	3	3	mA	2, 3, 4, 7
Deep power-down		I_{ZZ}	10	10	µA	5, 8

Table 8: I_{DD} Specifications and Conditions (x32)

Note 1 applies to all parameters and conditions; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max		Units	Notes
			-6	-75		
Operating current: Active mode; Burst = 1; READ or WRITE; $^{t}RC = {}^{t}RC$ (MIN)		I_{DD1}	90	80	mA	2, 3, 4
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2P}	300	300	µA	5
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		I_{DD2N}	10	8	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		I_{DD3P}	5	5	mA	3, 4, 6
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3N}	20	18	mA	3, 4, 6
Operating current: Burst mode; READ or WRITE; All banks active, half DQ toggling every cycle		I_{DD4}	105	95	mA	2, 3, 4
Auto refresh current: CKE = HIGH; CS# = HIGH	^{t}RFC = 110ns	I_{DD5}	100	100	mA	2, 3, 4, 6
	^{t}RFC = 7.8125µs	I_{DD6}	3	3	mA	2, 3, 4, 7
Deep power-down		I_{ZZ}	10	10	µA	5, 8

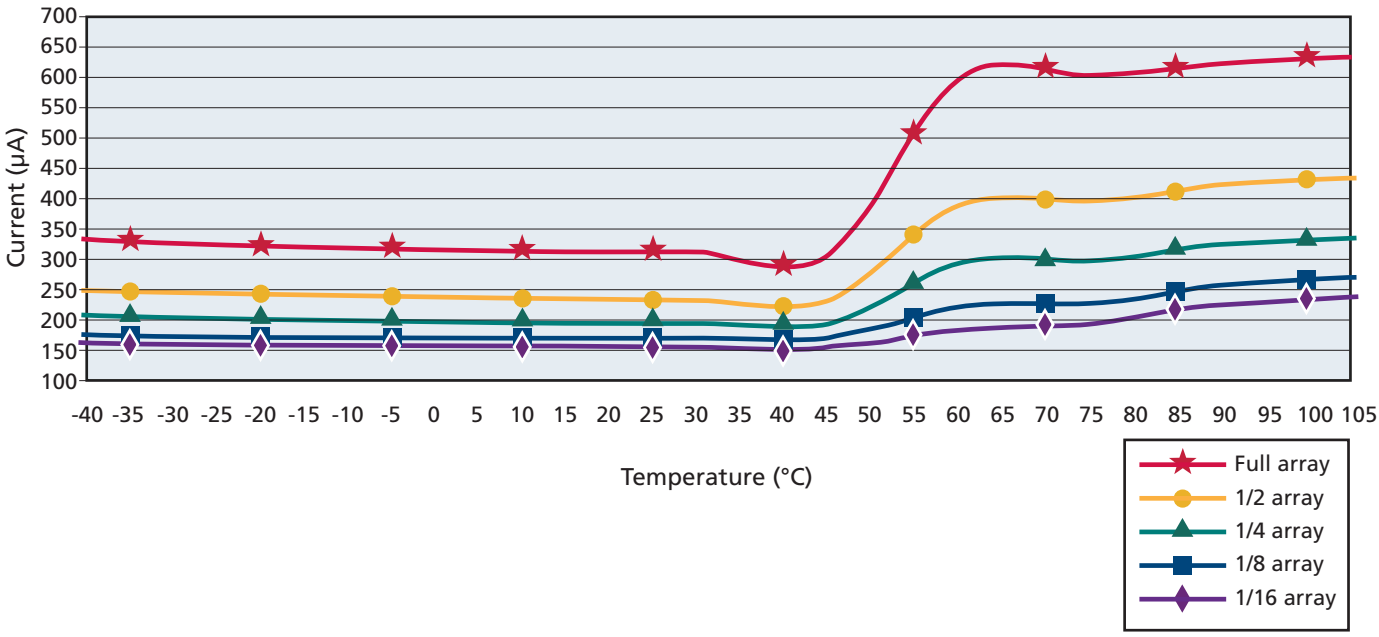
Table 9: I_{DD7} Specifications and Conditions (x16 and x32)

Notes 1, 5, 9, and 10 apply to all parameters and conditions; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Low Power	Standard	Units
Self refresh CKE = LOW; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are stable; Data bus inputs are stable	Full array, 85°C	I_{DD7}	500	700	µA
	Full array, 45°C		250	390	µA
	Half array, 85°C		400	520	µA
	Half array, 45°C		220	310	µA
	1/4 array, 85°C		350	430	µA
	1/4 array, 45°C		205	275	µA
	1/8 array, 85°C		350	430	µA
	1/8 array, 45°C		205	275	µA
	1/16 array, 85°C		325	375	µA
	1/16 array, 45°C		200	250	µA

Notes:
1. A full initialization sequence is required before proper device operation is ensured.
2. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
3. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. Measurement is taken 500ms after entering into this operating mode to allow tester measuring unit settling time.
6. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL}levels.
7. CKE is HIGH during REFRESH command period ^{t}RFC (MIN) else CKE is LOW.
8. Typical values at 25°C (not a maximum value).
9. Enables on-die refresh and address counters.
10. Values for I_{DD7} 85°C full array and partial array are guaranteed for the entire temperature range. All other I_{DD7} values are estimated.

Figure 7: Typical Self Refresh Current vs. Temperature



Electrical Specifications – AC Operating Conditions

Table 10: Electrical Characteristics and Recommended AC Operating Conditions

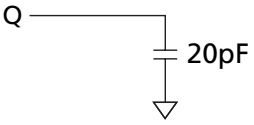
Notes 1–5 apply to all parameters and conditions

AC Characteristics			-6		-75			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from CLK (positive edge)	CL = 3	tAC	–	5	–	5.4	ns	
	CL = 2		–	8	–	8		
Address hold time		tAH	1	–	1	–	ns	
Address setup time		tAS	1.5	–	1.5	–	ns	
CLK high-level width		tCH	2.5	–	2.5	–	ns	
CLK low-level width		tCL	2.5	–	2.5	–	ns	
Clock cycle time	CL = 3	tCK	6	–	7.5	–	ns	6
	CL = 2		9.6	–	9.6	–		
CKE hold time		tCKH	1	–	1	–	ns	
CKE setup time		tCKS	1.5	–	1.5	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		tCMH	1	–	1	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		tCMS	1.5	–	1.5	–	ns	
Data-in hold time		tDH	1	–	1	–	ns	
Data-in setup time		tDS	1.5	–	1.5	–	ns	
Data-out High-Z time	CL = 3	tHZ	–	5	–	5.4	ns	7
	CL = 2		–	8	–	8	ns	
Data-out Low-Z time		tLZ	1	–	1	–	ns	
Data-out hold time (load)		tOH	2.5	–	2.5	–	ns	
Data-out hold time (no load)		tOHn	1.8	–	1.8	–	ns	
ACTIVE-to-PRECHARGE command		tRAS	42	120,000	45	120,000	ns	
ACTIVE-to-ACTIVE command period		tRC	60	–	67.5	–	ns	
ACTIVE-to-READ or WRITE delay		tRCD	18	–	19.2	–	ns	
Refresh period (8192 rows)		tREF	–	64	–	64	ms	8
AUTO REFRESH period		tRFC	72	–	72	–	ns	
PRECHARGE command period		tRP	18	–	19.2	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		tRRD	2	–	2	–	tCK	
Transition time		tT	0.3	1.2	0.3	1.2	ns	9
WRITE recovery time		tWR	15	–	15	–	ns	10
Exit SELF REFRESH-to-ACTIVE command		tXSR	120	–	120	–	ns	11

Table 11: AC Functional Characteristics

Notes 1–5 apply to all parameters and conditions

Parameter		Symbol	-6	-75	Units	Notes
Last data-in to burst STOP command		tBDL	1	1	tCK	12
READ/WRITE command to READ/WRITE command		tCCD	1	1	tCK	12
Last data-in to new READ/WRITE command		tCDL	1	1	tCK	13
CKE to clock disable or power-down entry mode		tCKED	1	1	tCK	13
Data-in to ACTIVE command		tDAL	5	5	tCK	14, 16
Data-in to PRECHARGE command		tDPL	2	2	tCK	15, 16
DQM to input data delay		tDQD	0	0	tCK	12
DQM to data mask during WRITEs		tDQM	0	0	tCK	12
DQM to data High-Z during READs		tDQZ	2	2	tCK	12
WRITE command to input data delay		tDWD	0	0	tCK	12
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	tCK	
CKE to clock enable or power-down exit mode		tPED	1	1	tCK	13
Last data-in to PRECHARGE command		tRDL	2	2	tCK	15, 16
Data-out High-Z from PRECHARGE command	CL = 3	tROH	3	3	tCK	12
	CL = 2		2	2	tCK	

Notes:
1. A full initialization sequence is required before proper device operation is ensured.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C standard temperature and –40°C ≤ T_A ≤ +85°C industrial temperature) is ensured.
3. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. 

Outputs measured for 1.8V at 0.9V with equivalent load:

   Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.
5. AC timing tests have V_{IL} and V_{IH} with timing referenced to $V_{IH/2}$ = crossover point. If the input transition time is longer than tTmax, then the timing is referenced at $V_{IL,max}$ and $V_{IH,min}$ and no longer at the $V_{IH/2}$ crossover point.
6. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) during access or precharge states (READ, WRITE, including tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
7. tHZ defines the time at which the output achieves the open circuit condition, it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet tOH before going High-Z.
8. This device requires 8192 AUTO REFRESH cycles every 64ms (tREF). Providing a distributed AUTO REFRESH command every 7.8125µs meets the refresh requirement and ensures that each row is refreshed. Alternatively, 8192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRFC), once every 64ms.
9. AC characteristics assume tT = 1ns. For command and address input slew rates <0.5V/ns, timing must be derated. Input setup times require an additional 50ps for each 100 mV/

ns reduction in slew rate. Input hold times remain unchanged. If the slew rate exceeds 4.5V/ns, functionality is uncertain.

10. For auto precharge mode, the precharge timing budget (^{t}RP) begins at ^{t}RP – (1 × ^{t}CKns), after the first clock delay and after the last WRITE is executed.
11. CLK must be toggled a minimum of two times during this period.
12. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
13. Timing is specified by ^{t}CKS. Clock(s) specified as a reference only at minimum cycle rate.
14. Timing is specified by ^{t}WR plus ^{t}RP. Clock(s) specified as a reference only at minimum cycle rate.
15. Timing is specified by ^{t}WR.
16. Based on ^{t}CK (MIN), CL = 3.

Output Drive Characteristics

Table 12: Target Output Drive Characteristics (Full Strength)

Notes 1–2 apply to all parameters and conditions; characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	–2.80	–18.53
0.20	5.60	26.80	–5.60	–26.80
0.30	8.40	32.80	–8.40	–32.80
0.40	11.20	37.05	–11.20	–37.05
0.50	14.00	40.00	–14.00	–40.00
0.60	16.80	42.50	–16.80	–42.50
0.70	19.60	44.57	–19.60	–44.57
0.80	22.40	46.50	–22.40	–46.50
0.85	23.80	47.48	–23.80	–47.48
0.90	23.80	48.50	–23.80	–48.50
0.95	23.80	49.40	–23.80	–49.40
1.00	23.80	50.05	–23.80	–50.05
1.10	23.80	51.35	–23.80	–51.35
1.20	23.80	52.65	–23.80	–52.65
1.30	23.80	53.95	–23.80	–53.95
1.40	23.80	55.25	–23.80	–55.25
1.50	23.80	56.55	–23.80	–56.55
1.60	23.80	57.85	–23.80	–57.85
1.70	23.80	59.15	–23.80	–59.15
1.80	–	60.45	–	–60.45
1.90	–	61.75	–	–61.75

Notes:
1. Table values based on nominal impedance of 25Ω (full drive strength) at $V_{DDQ/2}$.
2. The full variation in drive current, from minimum to maximum (due to process, voltage, and temperature) will lie within the outer bounding lines of the I-V curves.

Table 13: Target Output Drive Characteristics (Three-Quarter Strength)

Notes 1 and 2 apply to all parameters and conditions; characteristics are specified under best and worst process variations/ conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.96	12.97	–1.96	–12.97
0.20	3.92	18.76	–3.92	–18.76
0.30	5.88	22.96	–5.88	–22.96
0.40	7.84	25.94	–7.84	–25.94
0.50	9.80	28.00	–9.80	–28.00
0.60	11.76	29.75	–11.76	–29.75
0.70	13.72	31.20	–13.72	–31.20
0.80	15.68	32.55	–15.68	–32.55
0.85	16.66	33.24	–16.66	–33.24
0.90	16.66	33.95	–16.66	–33.95
0.95	16.66	34.58	–16.66	–34.58
1.00	16.66	35.04	–16.66	–35.04
1.10	16.66	35.95	–16.66	–35.95
1.20	16.66	36.86	–16.66	–36.86
1.30	16.66	37.77	–16.66	–37.77
1.40	16.66	38.68	–16.66	–38.68
1.50	16.66	39.59	–16.66	–39.59
1.60	16.66	40.50	–16.66	–40.50
1.70	16.66	41.41	–16.66	–41.41
1.80	–	42.32	–	–42.32
1.90	–	43.23	–	–43.23

Notes:
1. Table values based on nominal impedance of 37Ω (three-quarter drive strength) at $V_{DDQ/2}$.
2. The full variation in drive current, from minimum to maximum (due to process, voltage, and temperature) will lie within the outer bounding lines of the I-V curves.

Table 14: Target Output Drive Characteristics (One-Half Strength)

Notes 1–3 apply to all parameters and conditions; characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	–1.27	–8.42
0.20	2.55	12.30	–2.55	–12.30
0.30	3.82	14.95	–3.82	–14.95
0.40	5.09	16.84	–5.09	–16.84
0.50	6.36	18.20	–6.36	–18.20
0.60	7.64	19.30	–7.64	–19.30
0.70	8.91	20.30	–8.91	–20.30
0.80	10.16	21.20	–10.16	–21.20
0.85	10.80	21.60	–10.80	–21.60
0.90	10.80	22.00	–10.80	–22.00
0.95	10.80	22.45	–10.80	–22.45
1.00	10.80	22.73	–10.80	–22.73
1.10	10.80	23.21	–10.80	–23.21
1.20	10.80	23.67	–10.80	–23.67
1.30	10.80	24.14	–10.80	–24.14
1.40	10.80	24.61	–10.80	–24.61
1.50	10.80	25.08	–10.80	–25.08
1.60	10.80	25.54	–10.80	–25.54
1.70	10.80	26.01	–10.80	–26.01
1.80	–	26.48	–	–26.48
1.90	–	26.95	–	–26.95

Notes:
1. Table values based on nominal impedance of 55Ω (one-half drive strength) at $V_{DDQ/2}$.
2. The full variation in drive current, from minimum to maximum (due to process, voltage, and temperature) will lie within the outer bounding lines of the I-V curves.
3. The I-V curve for one-quarter drive strength is approximately 50% of one-half drive strength.