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SYNCHRONOUS DRAM

MT48H4M16LF - 1 MEG x 16 x 4 BANKS

Features

- Temperature compensated self refresh (TCSR)
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes concurrent auto precharge, and auto refresh modes
- Self refresh mode; standard and low power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Low voltage power supply
- Partial array self refresh power-saving mode
- Deep power-down mode
- Programmable output drive strength
- Operating temperature ranges:
  Extended (-25°C to +85°C)
  Industrial (-40°C to +85°C)

OPTIONS	MARKING
• VDD/VDDQ	
1.8V/1.8V	H
• Configurations	
4 Meg x 16 (1 Meg x 16 x 4 banks)	4M16
• Package/Ball out	
54-ball FBGA, 8mm x 8mm (standard)	F4
54-ball FBGA, 8mm x 8mm (lead-free)	B4
• Timing (Cycle Time)	
8ns @ CL = 3 (125 MHz)	-8
9.6ns @ CL = 3 (104 MHz)	-10
• Operating Temperature	
Extended (-25°C to +85°C)	none
Industrial (-40°C to +85°C)	IT

FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on the Micron web site, www.micron.com/decoder.

Figure 1: 54-Ball FBGA Pin Assignment (Top View)

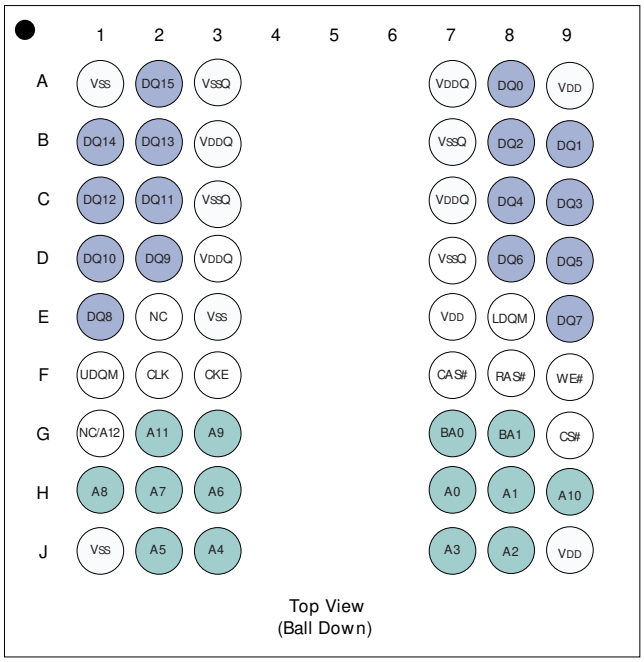

Table 1: Address Table

	4 MEG x 16
Configuration	1 Meg x 16 x 4 banks
Refresh Count	4K
Row Addressing	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	256 (A0–A7)

Table 2: Key Timing Parameters

CL = CAS (READ) latency

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2	CL = 3		
-8	125 MHz		6ns	2.5ns	1ns
-10	104 MHz	–	7ns	2.5ns	1ns
-8	104 MHz	8ns	–	2.5ns	1ns
-10	83 MHz	8ns	-	2.5ns	1ns

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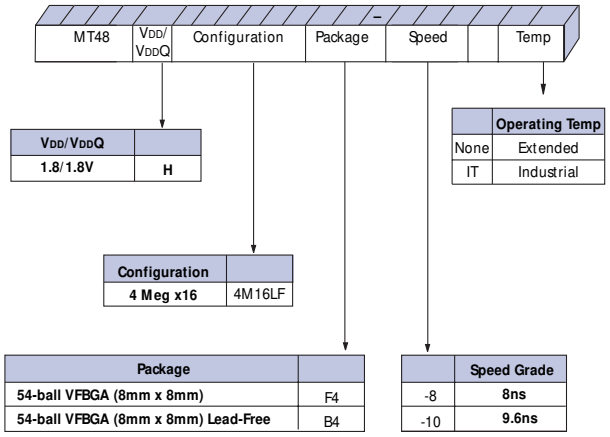
Figure 2: Part Numbering Diagram

Example Part Number: MT48H4M16LF-8 IT



General Description

The Micron® 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 16,777,216-bit banks is organized as 4,096 rows by 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 64Mb SDRAM is designed to operate in 1.8V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, Deep Power-Down Mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

Figure 3: Functional Block Diagram 4 Meg x 16 SDRAM

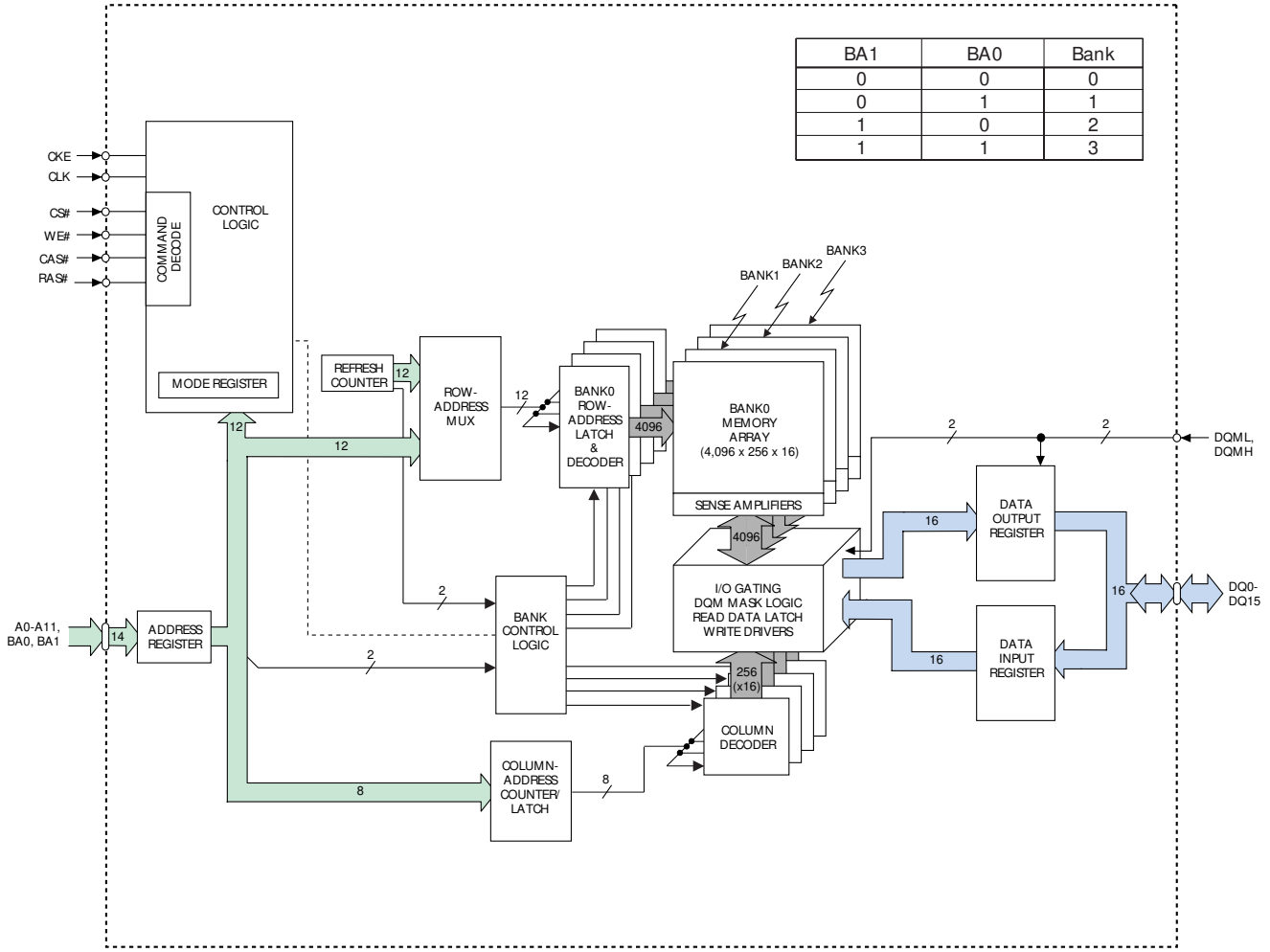


Table 3: Ball Descriptions

54-BALL FBGA	SYMBOL	TYPE	DESCRIPTION
F2	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank), DEEP POWER DOWN (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
G9	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F7, F8, F9	CAS#, RAS#, WE#	Input	Command Inputs: CAS#, RAS#, and WE# (along with CS#) define the command being entered.
E8, F1	LDQM, UDQM	Input	Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. LDQM corresponds to DQ0–DQ7, UDQM corresponds to DQ8–DQ15. LDQM and UDQM are considered same state when referenced as DQM.
G7, G8	BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. These pins also select between the mode register and the extended mode register.
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2	A0–A11	Input	Address Inputs: A0–A11 are sampled during the ACTIVE command (row-address A0–A11) and READ/WRITE command (column-address A0–A7; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	DQ0–DQ15	I/O	Data Input/Output: Data bus.
E2, G1	NC	–	These could be left unconnected, but it is recommended they be connected to V_{SS}. G1 is a no connect for this part but may be used as A12 in future designs.
A7, B3, C7, D3	V_{DDQ}	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
A3, B7, C3, D7	V_{SSQ}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
A9, E7, J9	V_{DD}	Supply	Core Power Supply.
A1, E3, J1	V_{SS}	Supply	Ground.

Functional Description

In general, the 64Mb SDRAMs (1 Meg x 16 x 4 banks) are quad-bank DRAMs that operate at 1.8V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 16,777,216-bit banks is organized as 4,096 rows by 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A11 select the row). The address bits (A0–A7) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power should be applied to V_{DD} and V_{DDQ} simultaneously. Once the power is applied to V_{DD} and V_{DDQ} and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, command inhibit or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one command inhibit or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO refresh cycles must be performed. After the AUTO refresh cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

In order to achieve low power consumption, there are two mode registers in the mobile component, mode register and extended mode register. The mode register is illustrated in Figure 4, Mode Register Definition, on page 9 (the extended mode register is illustrated in Figure 6, Extended Mode Register Table, on page 11).

The mode register defines the specific mode of operation of the SDRAM, including burst length, burst type, CAS latency, operating mode and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10, and M11 should be set to zero. M12 and M13 should be set to zero to prevent extended mode register.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4, Mode Register Definition, on page 9. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A0–A7 when the burst length is set to two; by A2–A7 when the burst length is set to four; and by A3–A7 when the burst length is set to eight.

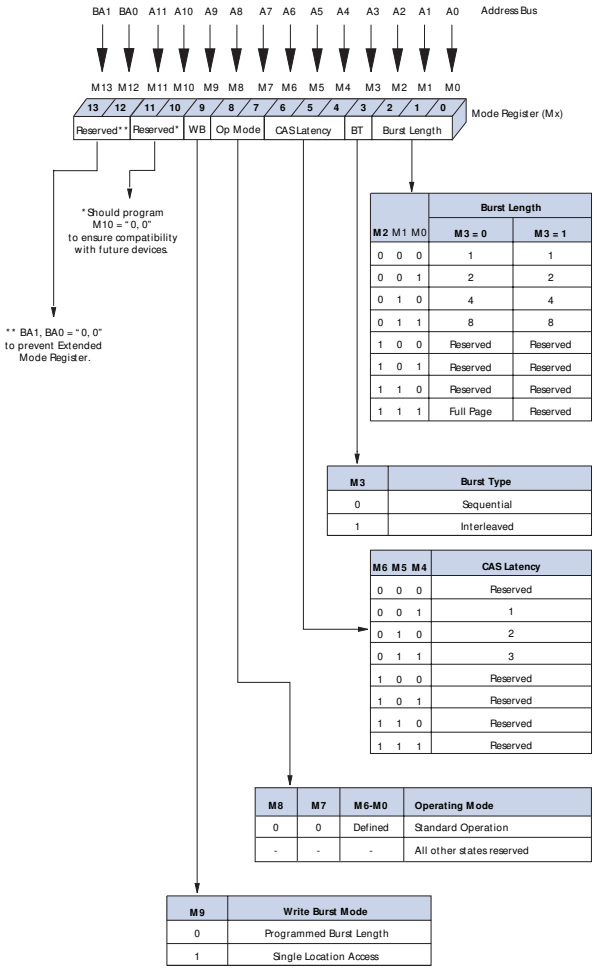
Table 4: Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0–A7 (location 0-y)	Cn, Cn+1, Cn+2, Cn+3, Cn+4..., ...Cn-1, Cn...	Not Supported

NOTE:

1. For full-page accesses: y = 256.
2. For a burst length of two, A1–A7 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2–A7 select the block-of-four burst; A0–A1 select the starting column within the block.
4. For a burst length of eight, A3–A7 select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A7 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0–A7 select the unique column to be accessed, and mode register bit M3 is ignored.

Figure 4: Mode Register Definition



The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 4.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to one, two, or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge $n + m$. The DQs will start driving as a result of the clock edge one cycle earlier ($n + m - 1$), and provided that the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming that the clock cycle time is such that all relevant access times are met, if a read command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 5, CAS Latency. Table 5, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 5: CAS Latency

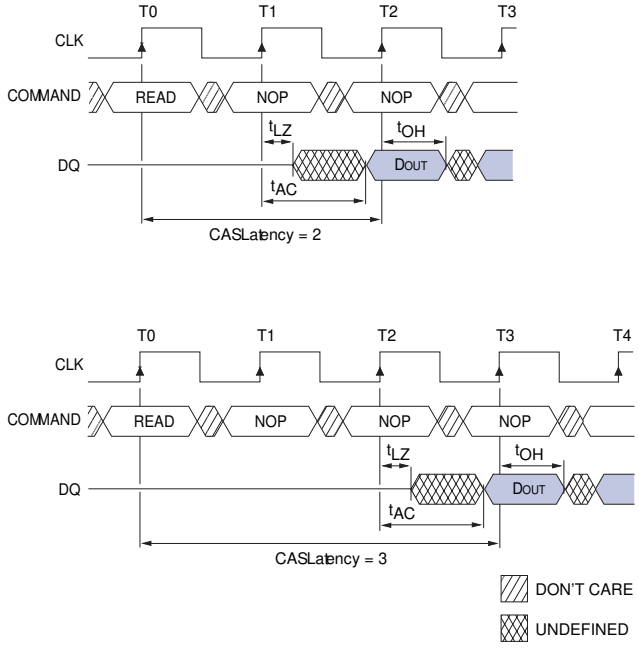


Table 5: CAS Latency

SPEED	ALLOWABLE OPERATING FREQUENCY (MHZ)	
	CAS LATENCY = 2	CAS LATENCY = 3
-8	≤ 104	≤ 125
-10	≤ 83.3	≤ 104

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both read and write bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (non-burst) accesses.

Extended Mode Register

The extended mode register controls the functions beyond those controlled by the mode register. These additional functions are special features of the mobile device. They include temperature compensated self refresh (TCSR) control, partial array self refresh (PASR), and output drive strength. Not programming the extended mode register upon initialization, will result in default settings for the low power features. The extended mode will default to the +85°C setting for TCSR, full drive strength, and full array refresh.

The extended mode register is programmed via the MODE REGISTER SET command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

The extended mode register must be programmed with E6 through E11 set to "0." It must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

Once the values are entered the extended mode register settings will be retained even after exiting deep power-down.

Temperature Compensated Self Refresh

Temperature compensated self refresh (TCSR) allows the controller to program the refresh interval during self refresh mode, according to the case temperature of the mobile device. This allows great power savings during SELF REFRESH during most operating temperature ranges. Only during extreme temperatures would the controller have to select the maximum TCSR level. This would guarantee data during SELF REFRESH.

Every cell in the SDRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. Historically, during self refresh, the refresh rate has been set to accommodate the worst case, or highest temperature range expected.

Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high, because the refresh rate was set to accommodate the higher temperatures. Adjusting the refresh rate by setting E4 and E3 allows the SDRAM to accommodate more specific temperature regions during SELF REFRESH. There are four temperature settings, which will vary the SELF REFRESH current according to the selected temperature. This selectable refresh rate will save power when the SDRAM is operating at normal temperatures.

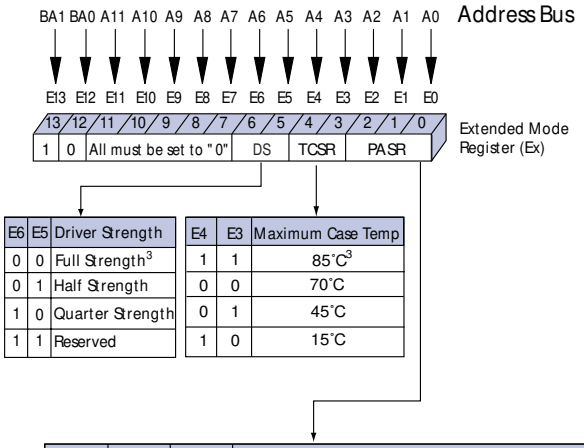
Partial Array Self Refresh

For further power savings during SELF REFRESH, the partial array self refresh (PASR) feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The refresh options are all banks (banks 0, 1, 2, and 3); two banks (banks 0 and 1); and one bank (bank 0). Also included in the refresh options are the 1/2 bank and 1/4 bank partial array self refresh (bank 0). WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during SELF REFRESH. It's important to note that data in unused banks, or portions of banks, will be lost when PASR is used. Data will be lost in banks 1, 2, and 3 when the one bank option is used.

Driver Strength

Bits E5 and E6 of the extended mode register can be used to select the driver strength of the DQ outputs. This value should be set according to the application's requirements. Full drive strength was carried over from standard SDRAM and is suitable to drive higher load systems. Full drive strength is not recommended for loads under 30pF. Half drive strength is intended for multi-drop systems with various loads. This drive option is not recommended for loads under 15pF. Quarter drive strength is intended for lighter loads or point-to-point systems.

Figure 6: Extended Mode Register Table



E6	E5	Driver Strength
0	0	Full Strength[3]
0	1	Half Strength
1	0	Quarter Strength
1	1	Reserved

E4	E3	Maximum Case Temp
1	1	85°C[3]
0	0	70°C
0	1	45°C
1	0	15°C

E2	E1	E0	Self Refresh Coverage
0	0	0	Four Banks[3]
0	0	1	Two Banks (Bank 0,1)
0	1	0	One Bank (Bank 0)
0	1	1	RFU
1	0	0	RFU
1	0	1	1/2 Bank (Bank 0)[4]
1	1	0	1/4 Bank (Bank 0)[5]
1	1	1	RFU

NOTE:

1. E13 and E12 (BA1 and BA0) must be "1, 0" to select the extended mode register (vs. the base mode register).
2. RFU: Reserved for future use
3. Default EMR values are full array for PASR, full drive strength, and 85° for TCSR.
4. E11 = 0
5. E10, E11 = 0

Commands

Figure 6, Truth Table 1 – Commands and DQM Operation[1] provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

Table 6: Truth Table 1 – Commands and DQM Operation[1]

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQS	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/Col	Valid	4
BURST TERMINATE or DEEP POWER DOWN (Enter deep power down mode)	L	H	H	L	X	X	X	9, 10
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Bank, A10	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER/LOAD EXTENDED MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	X	X	X	X	L	X	Active	8
Write Inhibit/Output High-Z	X	X	X	X	H	X	High-Z	8

NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER DOWN
2. A0-A11 define op-code written to mode register.
3. A0–A11 provide row address, and BA0, BA1 determine which bank is made active.
4. A0–A7 provide column address; A10 HIGH enables the auto precharge feature (non persistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay). DQML controls DQ0-7, DQMH controls DQ8-15.
9. This command is BURST TERMINATE when CKE is high and DEEP POWER DOWN when CKE is low.
10. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However the DQs column reads a don't care state to illustrate that the BURST TERMINATE command can occur when there is no data present.

Command Inhibit

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode register is loaded via inputs A0–A11, BA0, BA1. See mode register heading in the Register Definition section. The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

The values of the mode register and extended mode register will be retained even when exiting deep power-down.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A7 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A7 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where auto precharge does not apply. Auto precharge is non persistent in that it is either enabled or disabled for each individual Read or Write command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAMs. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP has been met after the PRECHARGE command as shown in the operation section.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 64Mb SDRAM requires 4,096 AUTO REFRESH cycles every 64ms (^{t}REF). Providing a distributed AUTO REFRESH command every 15.625µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RFC), once every 64ms.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down, as long as power is not completely removed from the SDRAM. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands should be issued at once and then every 15.625µs or less, as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Deep Power-Down

The operating mode deep power-down achieves maximum power reduction by eliminating the power of the whole memory array of the device. Array data will not be retained once the device enters deep power-down mode.

This mode is entered by having all banks idle then CS# and WE# held low with RAS# and CAS# held high at the rising edge of the clock, while CKE is low. This mode is exited by asserting CKE high.

Operation

Bank/row Activation

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 7, Activating a Specific Row in a Specific Bank Register).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 8, which covers any case where 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 7: Activating a Specific Row in a Specific Bank Register

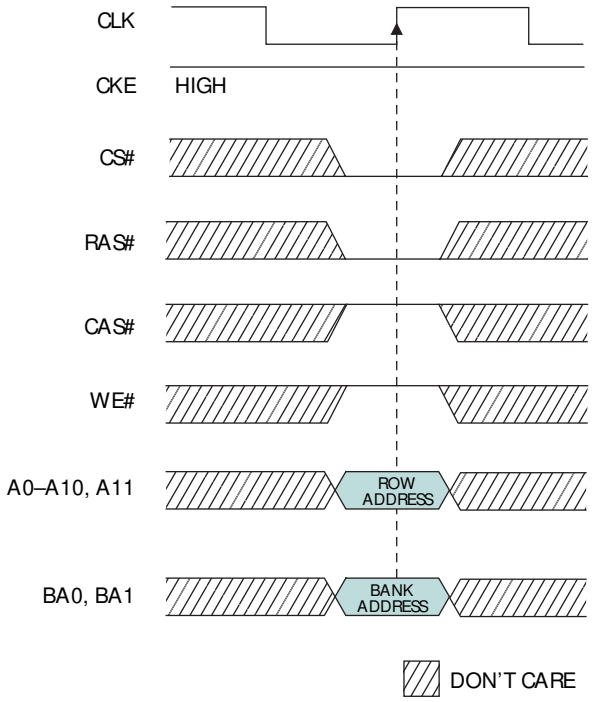
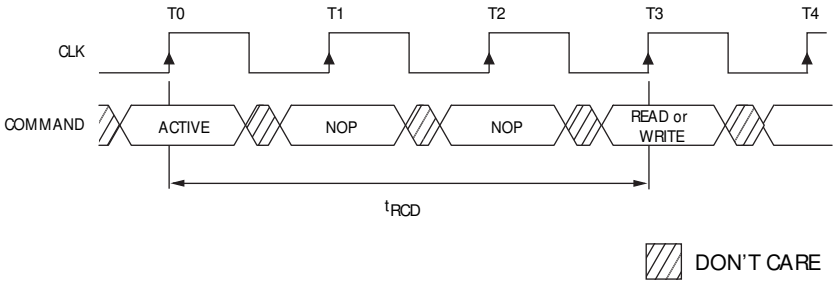


Figure 8: Meeting ^{t}RCD (MIN) when 2 < ^{t}RCD (MIN)/^{t}CK≤ 3



READs

READ bursts are initiated with a READ command, as shown in Figure 8.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 5, CAS Latency, on page 10, shows general timing for each possible CAS latency setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one.

This is shown in Figure 10, Consecutive READ Bursts, on page 17 for CAS latencies of two and three; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. The 64Mb SDRAM uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 11, Random READ Accesses, on page 17, or each subsequent READ may be performed to a different bank.

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQ go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

Figure 9: READ Command

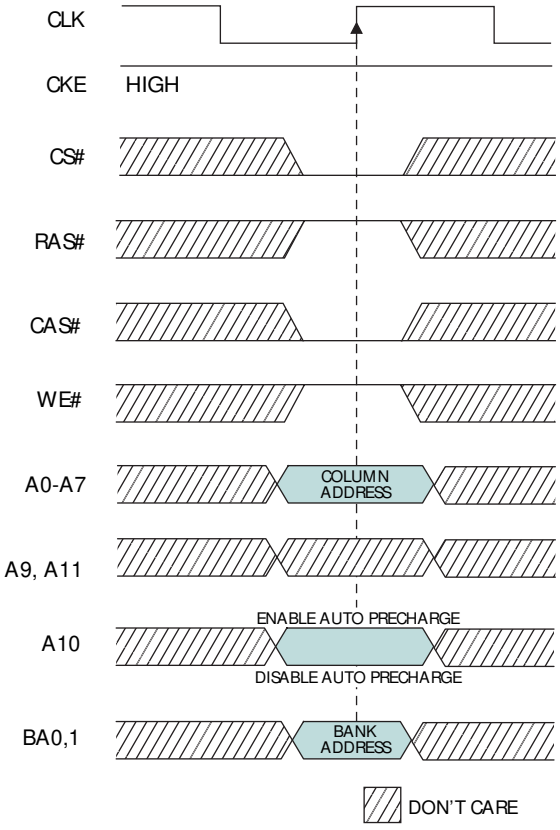
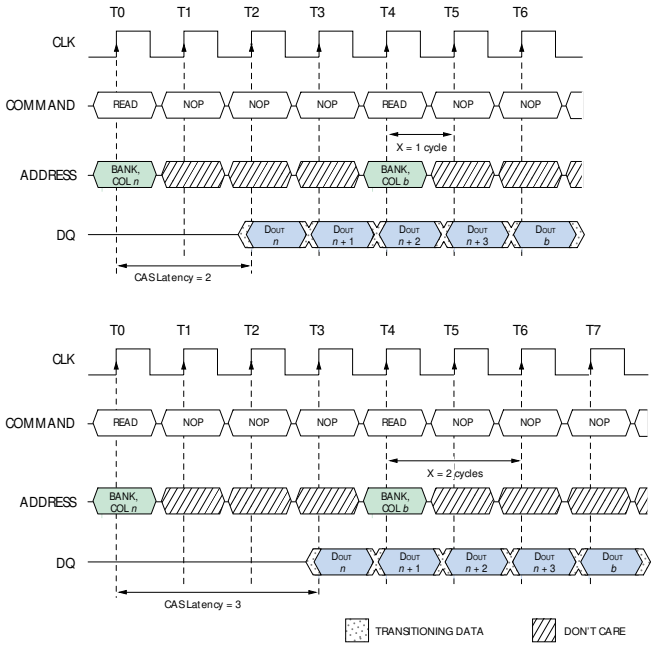
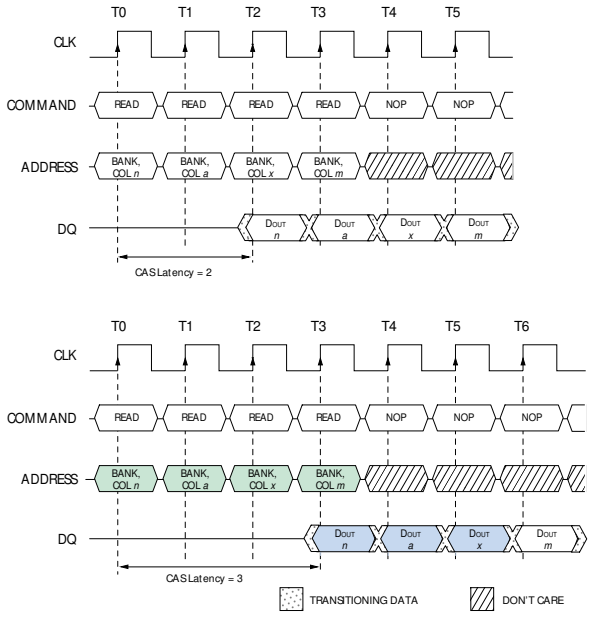


Figure 10: Consecutive READ Bursts



NOTE: Each READ command may be to any bank. DQM is LOW.

Figure 11: Random READ Accesses



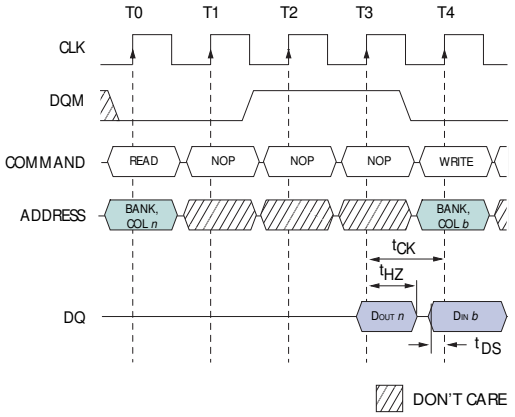
NOTE: Each READ command may be to any bank. DQM is LOW.

The DQM input is used to avoid I/O contention, as shown in Figure 12, READ to WRITE, and Figure 13, READ to WRITE with Extra Clock Cycle, on page 18. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQ will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 in Figure 14, READ to PRECHARGE, on page 18, then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 13, READ to WRITE with Extra Clock Cycle, shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 13 shows the case where the additional NOP is needed. A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 14 for each possible CAS latency; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

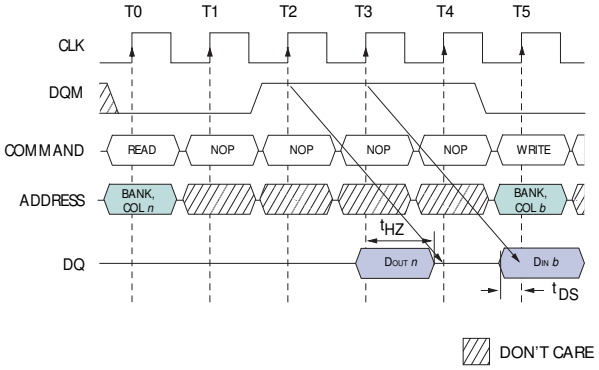
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

Figure 12: READ to WRITE



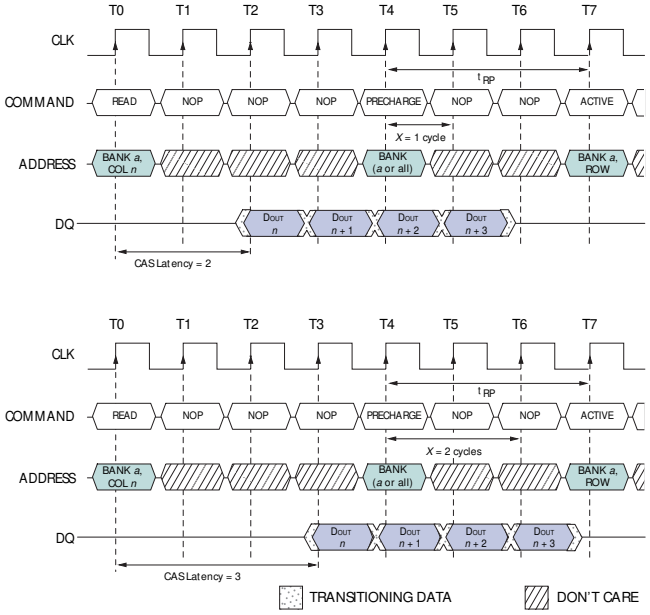
NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a burst of one is used, then DQM is not required.

Figure 13: READ to WRITE with Extra Clock Cycle



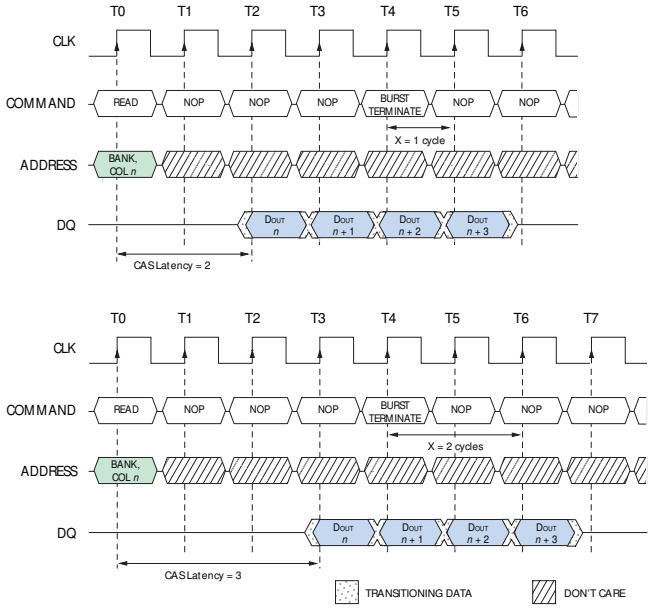
NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank.

Figure 14: READ to PRECHARGE



NOTE: DQM is LOW.

Figure 15: Terminating a READ Burst



NOTE: DQM is LOW.

Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 15, Terminating a READ Burst, for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

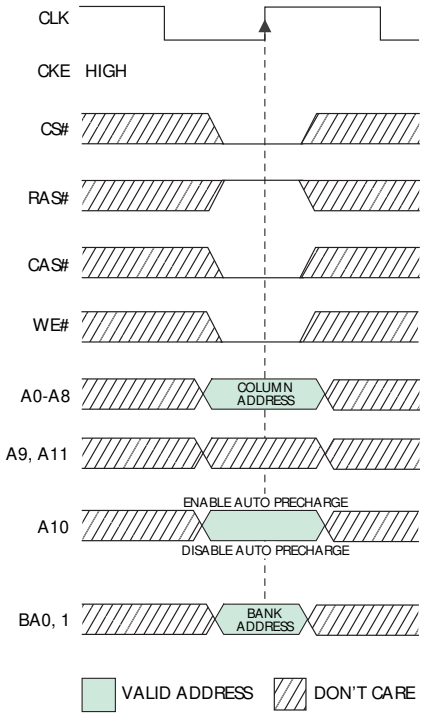
WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 16, WRITE Command.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

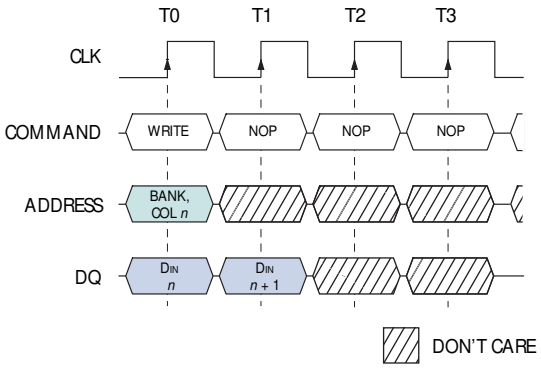
During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored (see Figure 18, WRITE to WRITE). A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Figure 16: WRITE Command



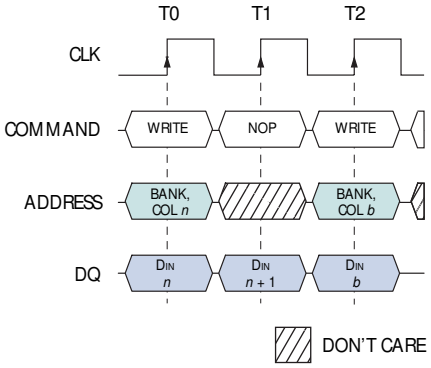
Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 19, Random WRITE Cycles. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. The 64Mb SDRAM uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 19, or each subsequent WRITE may be performed to a different bank.

Figure 17: WRITE Burst



NOTE: Burst length = 2. DQM is LOW.

Figure 18: WRITE to WRITE



NOTE: DQM is LOW. Each WRITE command may be to any bank.

Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is registered, the data inputs will be ignored, and writes will not be executed. An example is shown in Figure 20, WRITE to READ. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

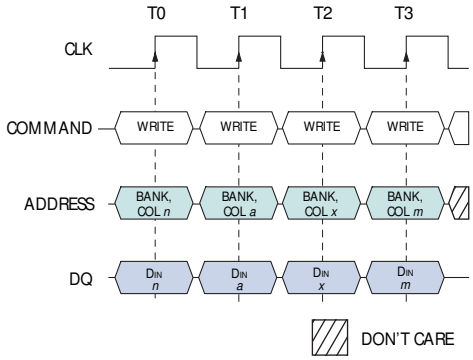
Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock plus time, regardless of frequency.

In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 21, WRITE to PRECHARGE. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

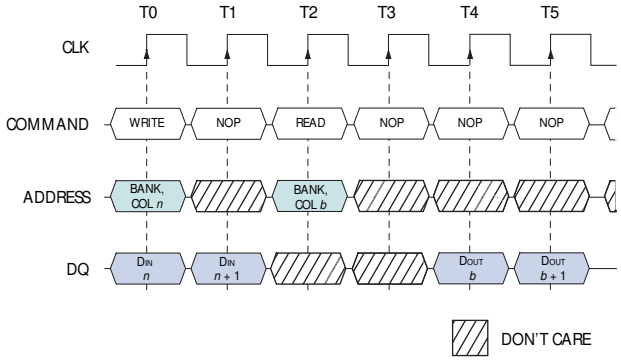
Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 23, Terminating a WRITE Burst, where data n is the last desired data element of a longer burst.

Figure 19: Random WRITE Cycles



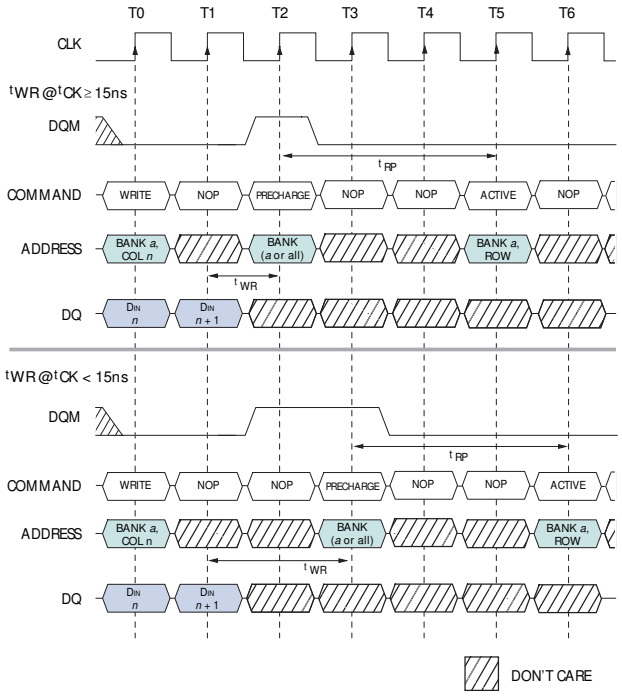
NOTE: Each WRITE command may be to any bank. DQM is LOW.

Figure 20: WRITE to READ



NOTE: The WRITE command may be to any bank, and the READ command may be to any bank. DQM is LOW. CAS latency = 2 for illustration.

Figure 21: WRITE to PRECHARGE



NOTE: DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

PRECHARGE

The PRECHARGE command (see Figure 24, PRECHARGE Command, on page 22) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

Power-down occurs if CKE is registered low coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting ^{t}CKS). See Figure 22, Power-Down.

Figure 22: Power-Down

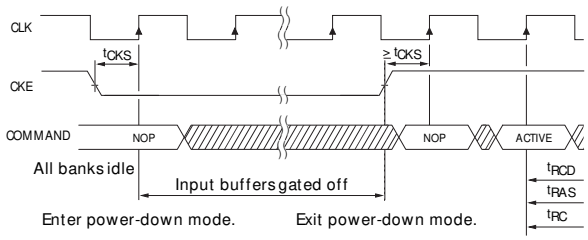
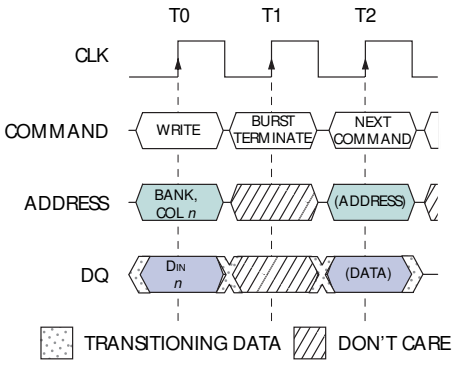
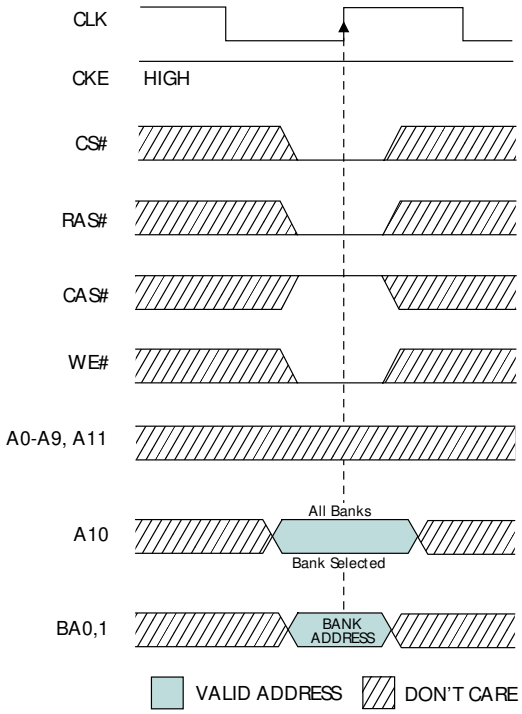


Figure 23: Terminating a WRITE Burst



NOTE: DQMs are LOW.

Figure 24: PRECHARGE Command



DEEP POWER-DOWN

Deep power down mode is a maximum power savings feature achieved by shutting off the power to the entire memory array of the device. Data on the memory array will not be retained once deep power down mode is executed. Deep power down mode is entered by having all banks idle then CS# and WE# held low with RAS# and CAS# high at the rising edge of the clock, while CKE is low. CKE must be held low during deep power-down.

In order to exit deep power down mode, CKE must be asserted high. After exiting, the following sequence is needed in order to enter a new command. Maintain NOP input conditions for a minimum of 100us. Issue PRECHARGE commands for all banks. Issue eight or more AUTOREFRESH commands. The values of the mode register and extended mode register will be retained upon exiting deep power-down.

CLOCK SUSPEND

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered low. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input

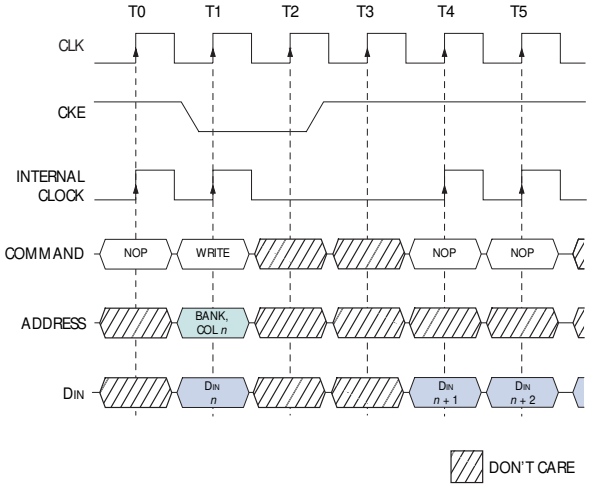
pins at the time of a suspended internal clock edge is ignored; any data present on the DQ pins remains driven; and burst counters are not incremented, as long as the clock is suspended. (See examples in Figure 25, Clock Suspend During WRITE Burst, and Figure 26, Clock Suspend During READ Burst.)

Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

BURST READ/SINGLE WRITE

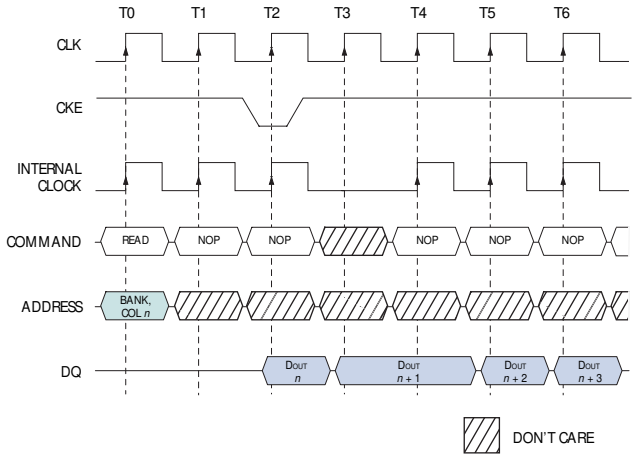
The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

Figure 25: Clock Suspend During WRITE Burst



NOTE: For this example, burst length = 4 or greater, and DM is LOW.

Figure 26: Clock Suspend During READ Burst



NOTE: For this example, CAS latency = 2, burst length = 4 or greater, and DQM is LOW.

Concurrent Auto Precharge

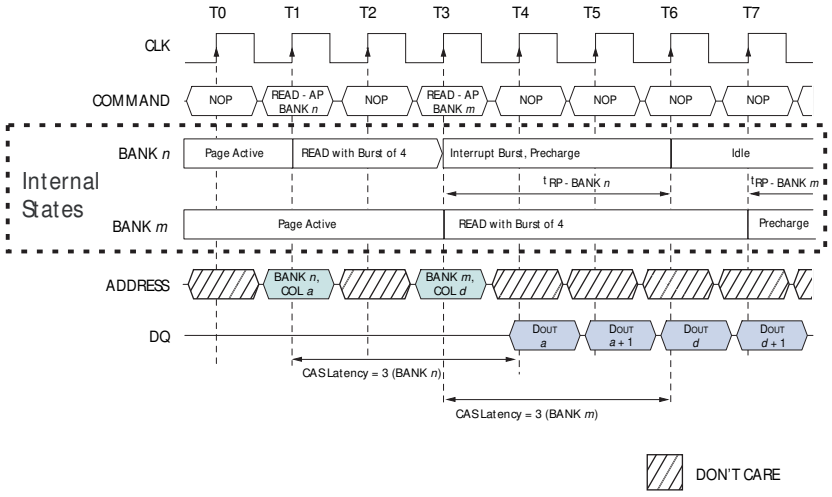
Micron SDRAM devices support Concurrent Auto precharge, which allows an access command (READ or WRITE) to another bank while an access command with auto precharge enabled is executing. Four cases where concurrent auto precharge occurs are defined below.

READ with Auto Precharge

1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ on bank *n*, two or three clocks later, depending on CAS latency. The precharge to bank *n* will begin when the READ to bank *m* is registered (Figure 27, READ With Auto Precharge Interrupted by a READ).

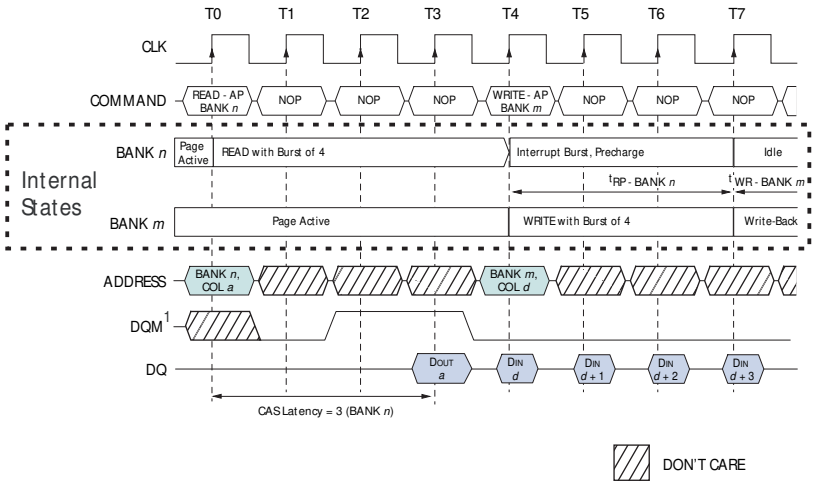
2. Interrupted by a WRITE (with or without auto precharge): When a WRITE to bank *m* registers, a READ on bank *n* will be interrupted. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank *n* will begin when the WRITE to bank *m* is registered (Figure 28, READ With Auto Precharge Interrupted by a WRITE).

Figure 27: READ With Auto Precharge Interrupted by a READ



NOTE: DQM is LOW.

Figure 28: READ With Auto Precharge Interrupted by a WRITE



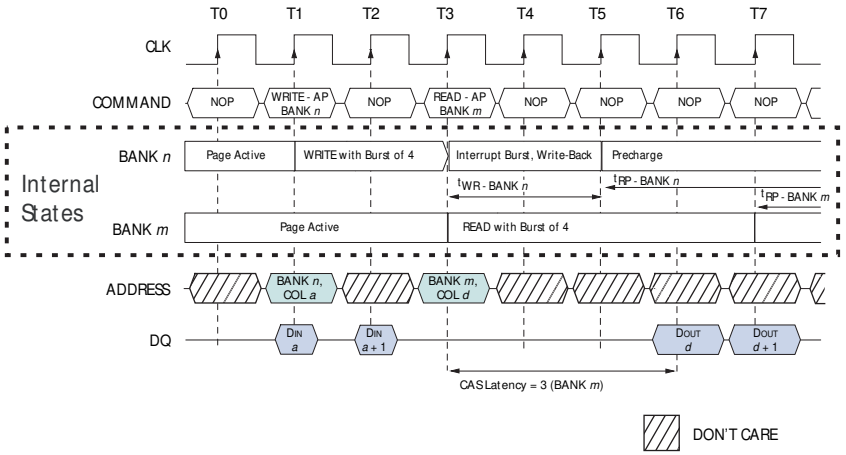
NOTE: DQM is HIGH at T2 to prevent DOUT-*a*+1 from contending with DIN-*d* at T4.

WRITE with Auto Precharge

3. Interrupted by a READ (with or without auto precharge): When a READ to bank *m* registers, it will interrupt a WRITE on bank *n*, with the data-out appearing 2 or 3 clocks later, (depending on CAS latency). The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 29, WRITE With Auto Precharge Interrupted by a READ).

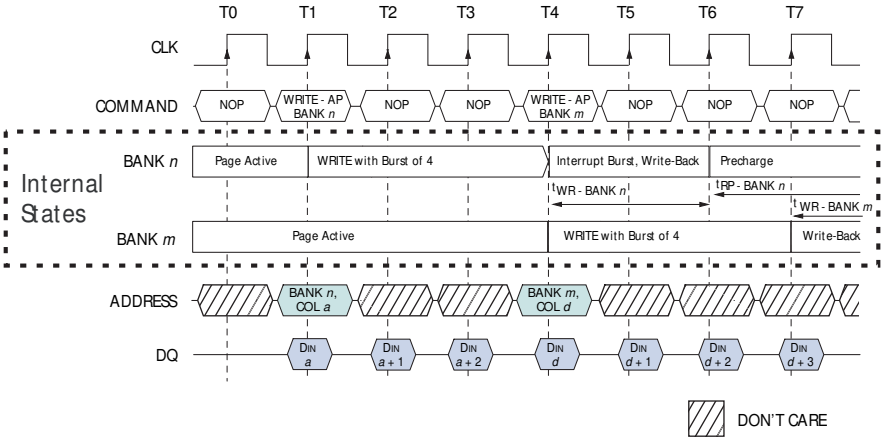
4. Interrupted by a WRITE (with or without auto precharge): When a WRITE to bank *m* registers, it will interrupt a WRITE on bank *n*. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (Figure 30, WRITE With Auto Precharge Interrupted by a WRITE).

Figure 29: WRITE With Auto Precharge Interrupted by a READ



NOTE: DQM is LOW.

Figure 30: WRITE With Auto Precharge Interrupted by a WRITE



NOTE: DQM is LOW.