Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Mobile SDRAM

MT48H16M16LF – 4 Meg x 16 x 4 banks
MT48H8M32LF – 2 Meg x 32 x 4 banks

Features

- Fully synchronous; all signals registered on positive edge of system clock
- V_{DD}/V_{DDQ} = 1.70–1.95V
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable burst lengths: 1, 2, 4, 8, or continuous page
- Auto precharge, includes concurrent auto precharge
- Auto refresh and self refresh modes
- LVTTL-compatible inputs and outputs
- On-chip temperature sensor to control refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive (DS)
- 64ms refresh period (8192 rows)

Options

Options	Marking
• V_{DD}/V_{DDQ}	
– 1.8V/1.8V	H
• Configuration	
– 16 Meg x 16 (4 Meg x 16 x 4 banks)	16M16
– 8 Meg x 32 (2 Meg x 32 x 4 banks)	8M32
• Plastic "green" package	
– 54-ball VFBGA (8mm x 9mm)	BF
– 90-ball VFBGA (8mm x 13mm)	B5
• Timing – cycle time	
– 7.5ns at CL = 3	-75
– 8ns at CL = 3	-8
• Power	
– Standard I_{DD2P}/I_{DD7}	None
– Low I_{DD2P}/I_{DD7}	L
• Operating temperature range	
– Commercial (0° to +70°C)	None
– Industrial (–40°C to +85°C)	IT
• Design revision	:G

Table 1: Addressing

	16 Meg x 16	8 Meg x 32
Configuration	4 Meg x 16 x 4 banks	2 Meg x 32 x 4 banks
Refresh count	8K	8K
Row addressing	8K (A[12:0])	4K (A[11:0])
Bank addressing	4 (BA[1:0])	4 (BA[1:0])
Column addressing	512 (A[8:0])	512 (A[8:0])

Table 2: Key Timing Parameters
CL = CAS (READ) latency

Speed Grade	Clock Rate (MHz)		Access Time		Data Setup Time	Data Hold Time
	CL = 2	CL = 3	CL = 2	CL = 3		
-75	104	133	8ns	6ns	1.5ns	1ns
-8	100	125	9ns	7ns	2.5ns	1ns

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Products and specifications discussed herein are subject to change by Micron without notice.

Table of Contents

Features 1
Options 1
General Description 5
Functional Block Diagrams. 6
Ball Assignments 8
Ball Descriptions 10
Functional Description 12
Initialization 12
Register Definition 13
Mode Register 13
Extended Mode Register (EMR) 16
Commands 19
Operations 23
Bank/Row Activation 23
READs 24
WRITEs 30
Truth Tables 40
Electrical Specifications 45
Absolute Maximum Ratings 45
Notes 52
Timing Diagrams 54
Package Dimensions 73
Revision History. 75

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

List of Figures

Figure 1: 256Mb Mobile SDRAM Part Numbering 5
Figure 2: 16 Meg x 16 SDRAM 6
Figure 3: 8 Meg x 32 SDRAM 7
Figure 4: 54-Ball FBGA (Top View) – 8mm x 9mm 8
Figure 5: 90-Ball VFBGA (Top View) – 8mm x 13mm 9
Figure 6: Mode Register Definition 14
Figure 7: CAS Latency 16
Figure 8: EMR Definition 17
Figure 9: Activating a Specific Row in a Specific Bank 23
Figure 10: Example: Meeting tRCD (MIN) When 2 < tRCD (MIN)/tCK < 3 24
Figure 11: READ Command 24
Figure 12: Consecutive READ Bursts 25
Figure 13: Random READ Accesses 26
Figure 14: READ-to-WRITE 27
Figure 15: READ-to-WRITE with Extra Clock Cycle 28
Figure 16: READ-to-PRECHARGE 28
Figure 17: Terminating a READ Burst 29
Figure 18: WRITE Command 30
Figure 19: WRITE Burst 31
Figure 20: WRITE-to-WRITE 31
Figure 21: Random WRITE Cycles 32
Figure 22: WRITE-to-READ 32
Figure 23: WRITE-to-PRECHARGE 33
Figure 24: Terminating a WRITE Burst 33
Figure 25: PRECHARGE Command 34
Figure 26: Power-Down 35
Figure 27: Clock Suspend During WRITE Burst 36
Figure 28: Clock Suspend During READ Burst 37
Figure 29: READ with Auto Precharge Interrupted by a READ 37
Figure 30: READ with Auto Precharge Interrupted by a WRITE 38
Figure 31: WRITE with Auto Precharge Interrupted by a READ 39
Figure 32: WRITE with Auto Precharge Interrupted by a WRITE 39
Figure 33: Typical Self Refresh Current vs. Temperature 50
Figure 34: Initialize and Load Mode Register 54
Figure 35: Power-Down Mode 55
Figure 36: Clock Suspend Mode 56
Figure 37: Auto Refresh Mode 57
Figure 38: Self Refresh Mode 58
Figure 39: READ – without Auto Precharge 59
Figure 40: READ – with Auto Precharge 60
Figure 41: Single READ – without Auto Precharge 61
Figure 42: Single READ – with Auto Precharge 62
Figure 43: Alternating Bank Read Accesses 63
Figure 44: READ – Continuous Page Burst 64
Figure 45: READ – DQM Operation 65
Figure 46: WRITE – Without Auto Precharge 66
Figure 47: WRITE – with Auto Precharge 67
Figure 48: Single WRITE – Without Auto Precharge 68
Figure 49: Single WRITE – with Auto Precharge 69
Figure 50: Alternating Bank Write Accesses 70
Figure 51: WRITE – Continuous Page Burst 71
Figure 52: WRITE – DQM Operation 72
Figure 53: 54-Ball VFBGA (8mm x 9mm) 73
Figure 54: 90-Ball VFBGA (8mm x 13mm) 74

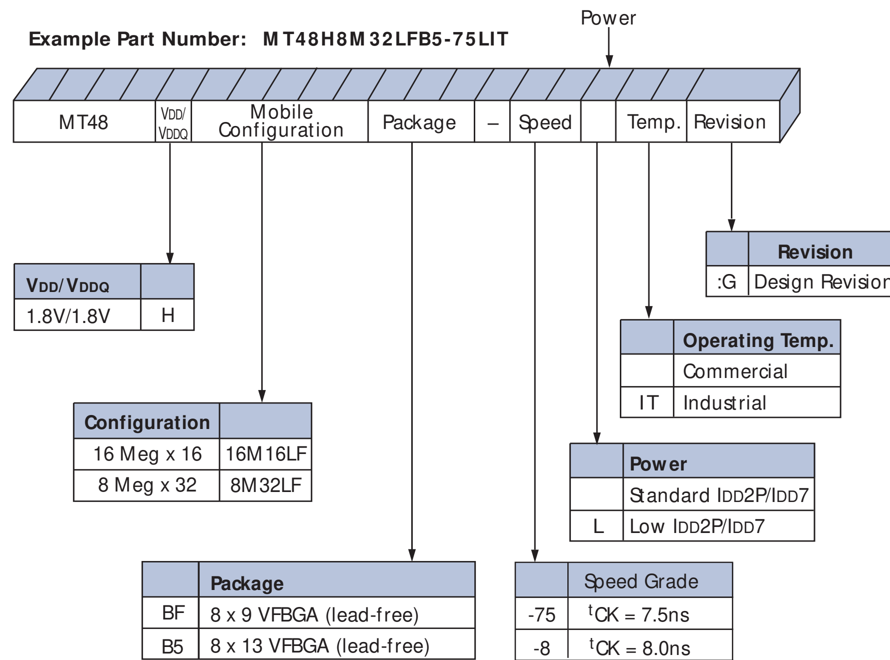
Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

List of Tables

Table 1: Addressing 1
Table 2: Key Timing Parameters 1
Table 3: VFBGA Ball Descriptions. 10
Table 4: Burst Definition Table 15
Table 5: Truth Table – Commands and DQM Operation 19
Table 6: Truth Table – CKE. 40
Table 7: Truth Table – Current State Bank *n*, Command to Bank *n* *41*
Table 8: Truth Table – Current State Bank *n*, Command to Bank *m* *43*
Table 9: Absolute Maximum Ratings 45
Table 10: DC Electrical Characteristics and Operating Conditions. 45
Table 11: Electrical Characteristics and Recommended AC Operating Conditions 46
Table 12: AC Functional Characteristics 47
Table 13: I_{DD} Specifications and Conditions (x16) 48
Table 14: I_{DD} Specifications and Conditions (x32) 49
Table 15: I_{DD7} – Self Refresh Current Options 50
Table 16: Capacitance 51

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Figure 1: 256Mb Mobile SDRAM Part Numbering



General Description

The Micron® 256Mb Mobile SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 67,108,864-bit banks is organized as 8192 rows by 512 columns by 16 bits. Each of the x32's 67,108,864-bit banks is organized as 4096 rows by 512 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BLs) of 1, 2, 4, or 8 locations, or continuous page burst, with a read burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 256Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. It also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

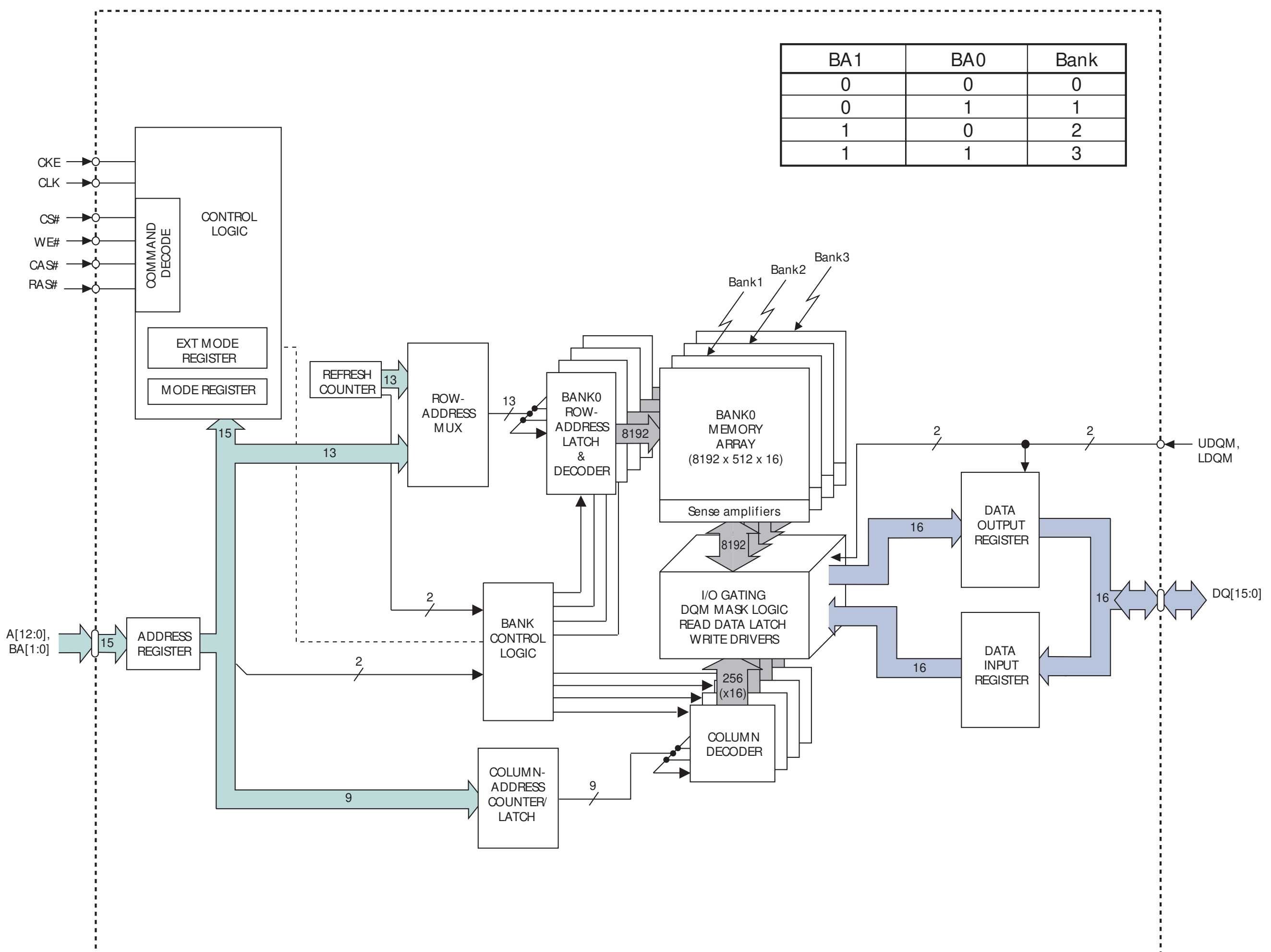
Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

The 256Mb SDRAM is designed to operate in 1.8V low-power memory systems. An auto refresh mode is provided, along with a power-saving deep power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM offers substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Functional Block Diagrams

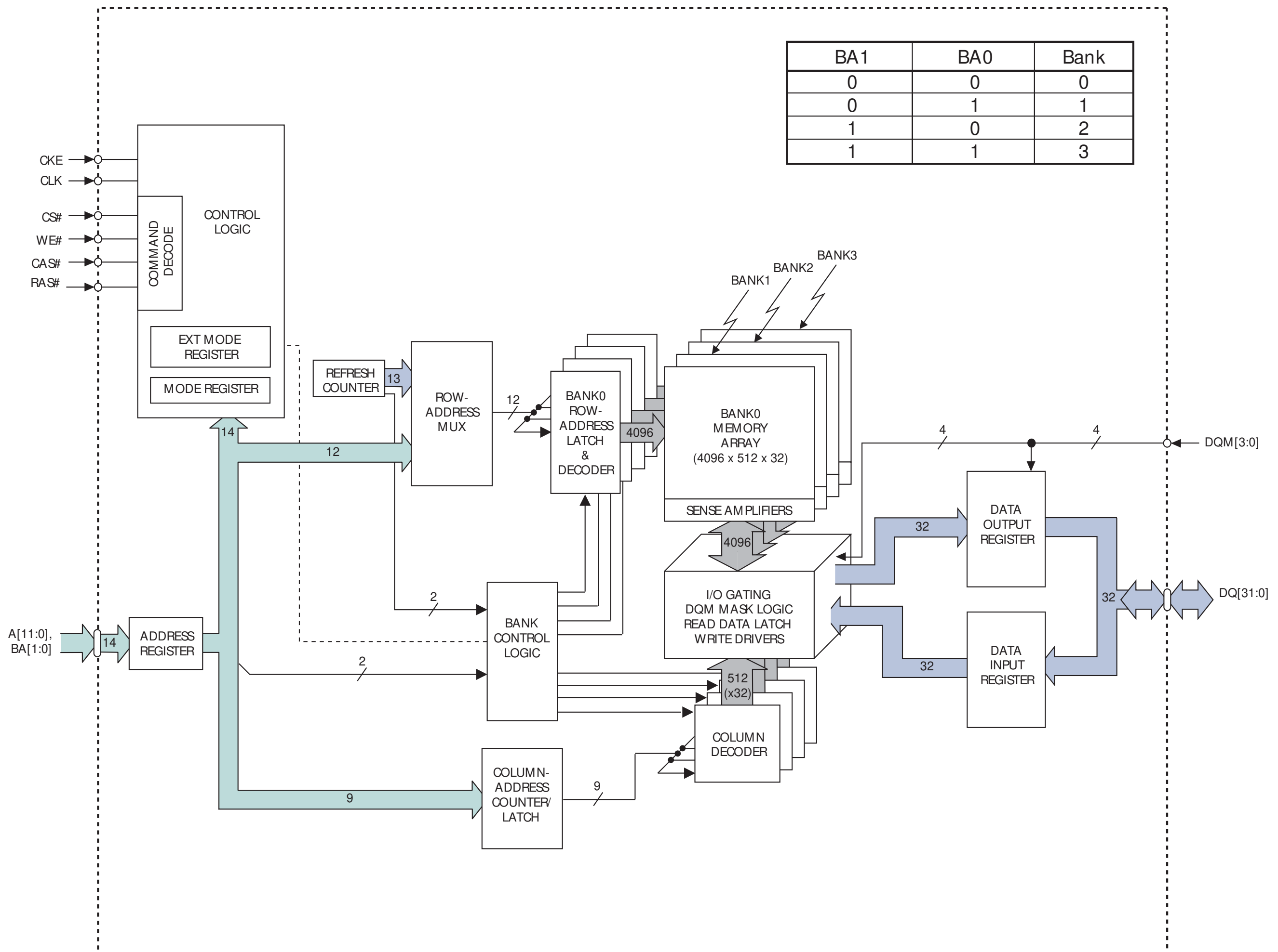
Figure 2: 16 Meg x 16 SDRAM



BA1	BA0	Bank
0	0	0
0	1	1
1	0	2
1	1	3

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

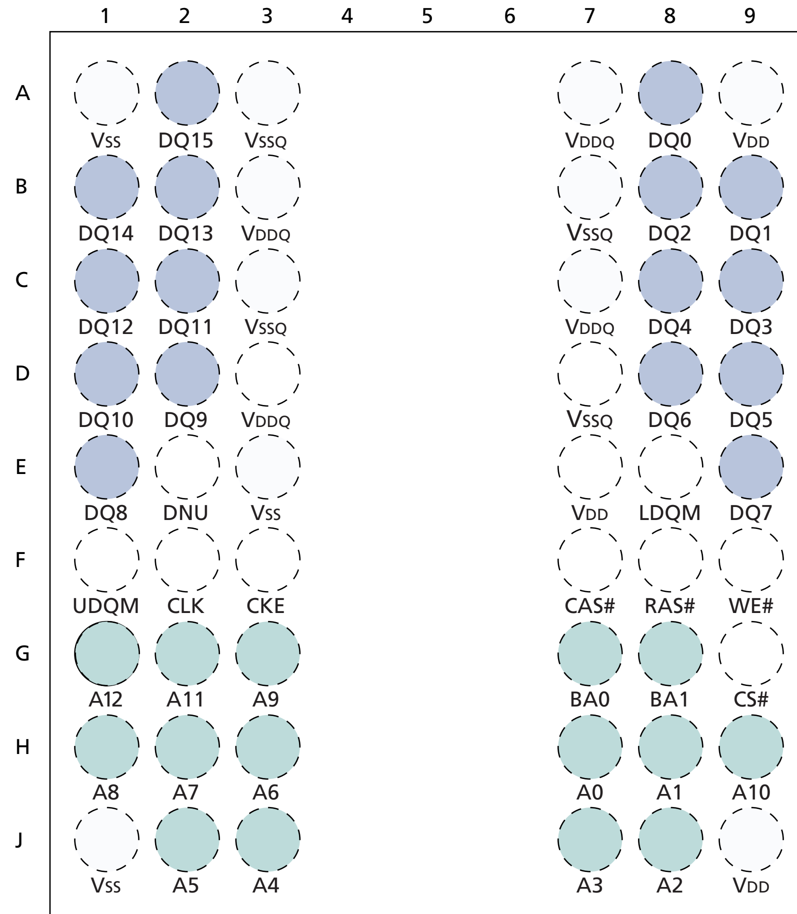
Figure 3: 8 Meg x 32 SDRAM



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

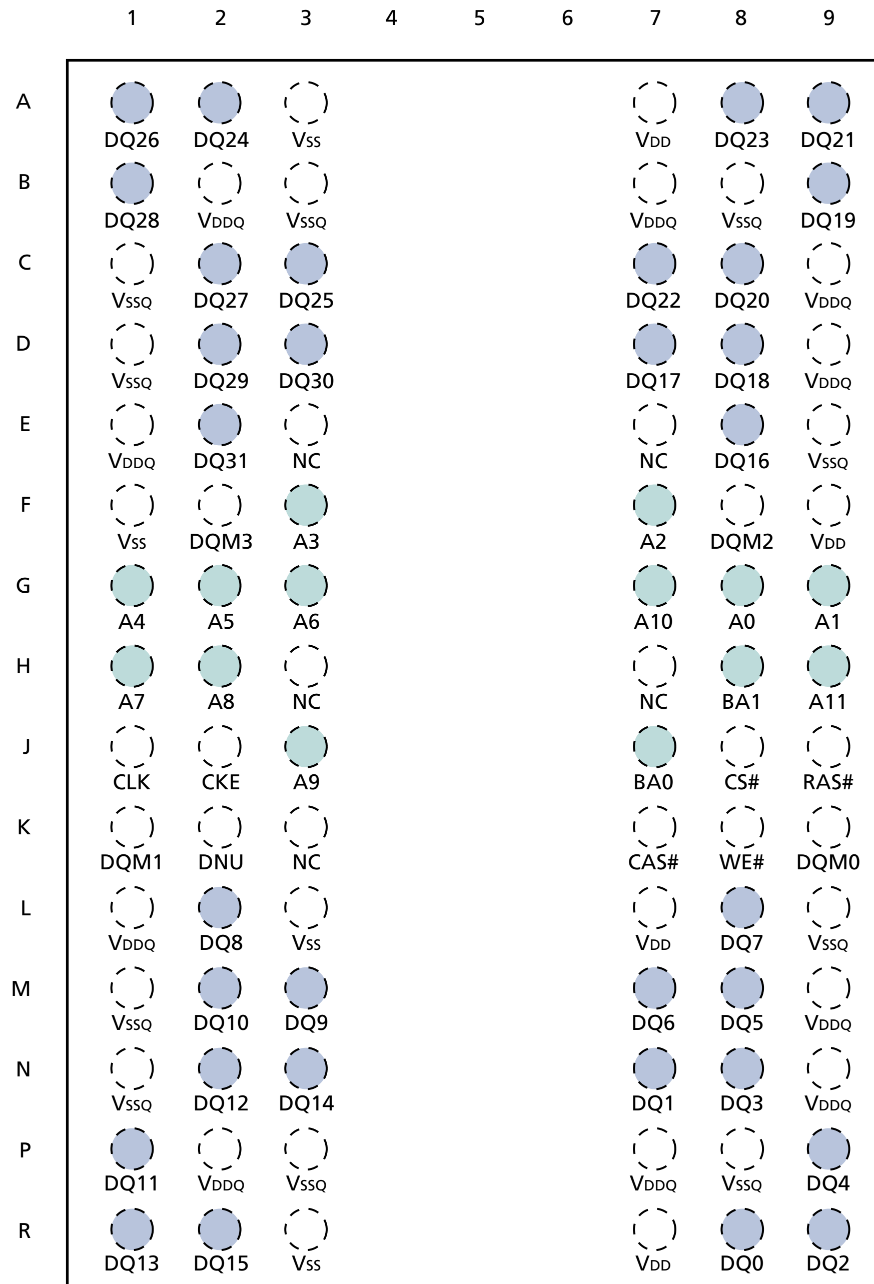
Ball Assignments

Figure 4: 54-Ball FBGA (Top View) – 8mm x 9mm



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Figure 5: 90-Ball VFBGA (Top View) – 8mm x 13mm



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Ball Descriptions

Table 3: VFBGA Ball Descriptions

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
F2	J1	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	J2	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), ACTIVE power-down (row active in any bank), Deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
G9	J8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F7, F8, F9	K7, J9, K8	CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F1, E8	K9, K1, F8, F2	UDQM LDQM, DQM[33:0]	Input	Input/output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. For the x16, LDQM corresponds to DQ[7:0] and UDQM corresponds to DQ[16:8]. For the x32, DQM0 corresponds to DQ[7:0], DQM1 corresponds to DQ[15:8], DQM2 corresponds to DQ[23:16], and DQM3 corresponds to DQ[31:24]. DQM[3:0] (or LDQM and UDQM if x16) are considered same state when referenced as DQM. DQM loading is designed to match that of DQ balls.
G7, G8	J7, H8	BA[1:0]	Input	Bank address input(s): BA[1:0] define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. These balls also provide the op-code during a LOAD MODE REGISTER (LMR) command. BA[1:0] become "Don't Care" when registering an ALL BANK PRECHARGE (A10 HIGH).
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2, G1	G8, G9, F7, F3, G1, G2, G3, H1, H2, J3, G7, H9	A[12:0]	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row-address A[12:0] and READ/WRITE command (column-address A[8:0] (x32); column-address A[8:0] (x16); with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA[1:0]. The address inputs also provide the op-code during a LMR command.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Table 3: VFBGA Ball Descriptions (Continued)

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	R8, N7, R9, N8, P9, M8, M7, L8, L2, M3, M2, P1, N2, R1, N3, R2, E8, D7, D8, B9, C8, A9, C7, A8, A2, C3, A1, C2, B1, D2, D3, E2	DQ[31:0]	I/O	Data input/output: Data bus.
A7, B3, C7, D3	B2, B7, C9, D9, E1, L1, M9, N9, P2, P7	V_{DDQ}	Supply	DQ power: Provide isolated power to DQ for improved noise immunity.
A3, B7, C3, D7	B8, B3, C1, D1, E9, L9, M1, N1, P3, P8	V_{SSQ}	Supply	DQ ground: Provide isolated ground to DQ for improved noise immunity.
A9, E7, J9	A7, F9, L7, R7	V_{DD}	Supply	Core power supply.
A1, E3, J1	A3, F1, L3, R3	V_{SS}	Supply	Ground.
–	E3, E7, H3, H7, K3	NC	–	Internally not connected: These could be left unconnected, but it is recommended they be connected to V_{SS}.
E2	K2	DNU	Input	E2 is a TEST pin that must be tied to V_{SS} or V_{SSQ} in normal operation.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Functional Description

In general, a 256Mb SDRAM is quad-bank DRAM that operates at 1.8V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK).

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank, A[12:0] select the row for x16, and A[11:0] select the row for x32). The address bits (A[8:0] for x16 and A[8:0] for x32) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The initialization for mobile SDRAM is as follows.

1. Simultaneously apply power to V_{DD} and V_{DDQ}.
2. After power supplies have settled, apply a stable clock signal. Stable clock is defined as a signal cycling within timing constraints specified for the clock pin.
3. Wait at least 100µs. During this period NOP or COMMAND INHIBIT commands should be applied. No other command other than NOP or COMMAND INHIBIT is allowed during this period.
4. Preform a PRECHARGE ALL command to place the SDRAM into an all banks idle state.
5. Wait at least ^{t}RP time. During this time NOP or COMMAND INHIBIT commands must be applied.
6. Issue an AUTO REFRESH command.
7. Wait at least ^{t}RFC time, during which only NOP or COMMAND INHIBIT commands are allowed.
8. Issue an Auto Refresh command.
9. Wait at least ^{t}RFC time, during which only NOP or COMMAND INHIBIT commands are allowed.
10. Issue a LOAD MODE REGISTER command with BA1=0, and BA0=0, to program the mode register with desired values.
11. Wait ^{t}MRD time. Only NOP or COMMAND INHIBIT commands may be applied during this time.
12. Issue a LOAD MODE REGISTER command with BA1 = 1, and BA0 = 0, to program the extended mode register with desired values.
13. Wait ^{t}MRD time. Only NOP or COMMAND INHIBIT commands may be applied during this time.

The Mobile SDRAM is now initialized and can accept any valid command.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Register Definition

Mode Register

There are two mode registers in the component: mode register and extended mode register (EMR). The mode register is illustrated in Figure 6 on page 14. The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length (BL), a burst type, a CAS latency (CL), an operating mode and a write burst mode, as shown in Figure 6 on page 14. The mode register is programmed via the LMR command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M[2:0] specify the BL, M3 specifies the type of burst, M[6:4] specify the CL, M[8:7] specify the operating mode, M9 specifies the write burst mode, and M[11:10] should be set to zero.

The mode register must be loaded when all banks are idle, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented, with the BL being programmable, as shown in Figure 6 on page 14. The BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. BL = 1, 2, 4, 8 locations are available for both the sequential and the interleaved burst types, and a continuous page burst is available for the sequential type. The continuous page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[8:1] when BL = 2, A[8:2] when BL = 4, and A[8:3] when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Continuous page bursts wrap within the page if the boundary is reached.

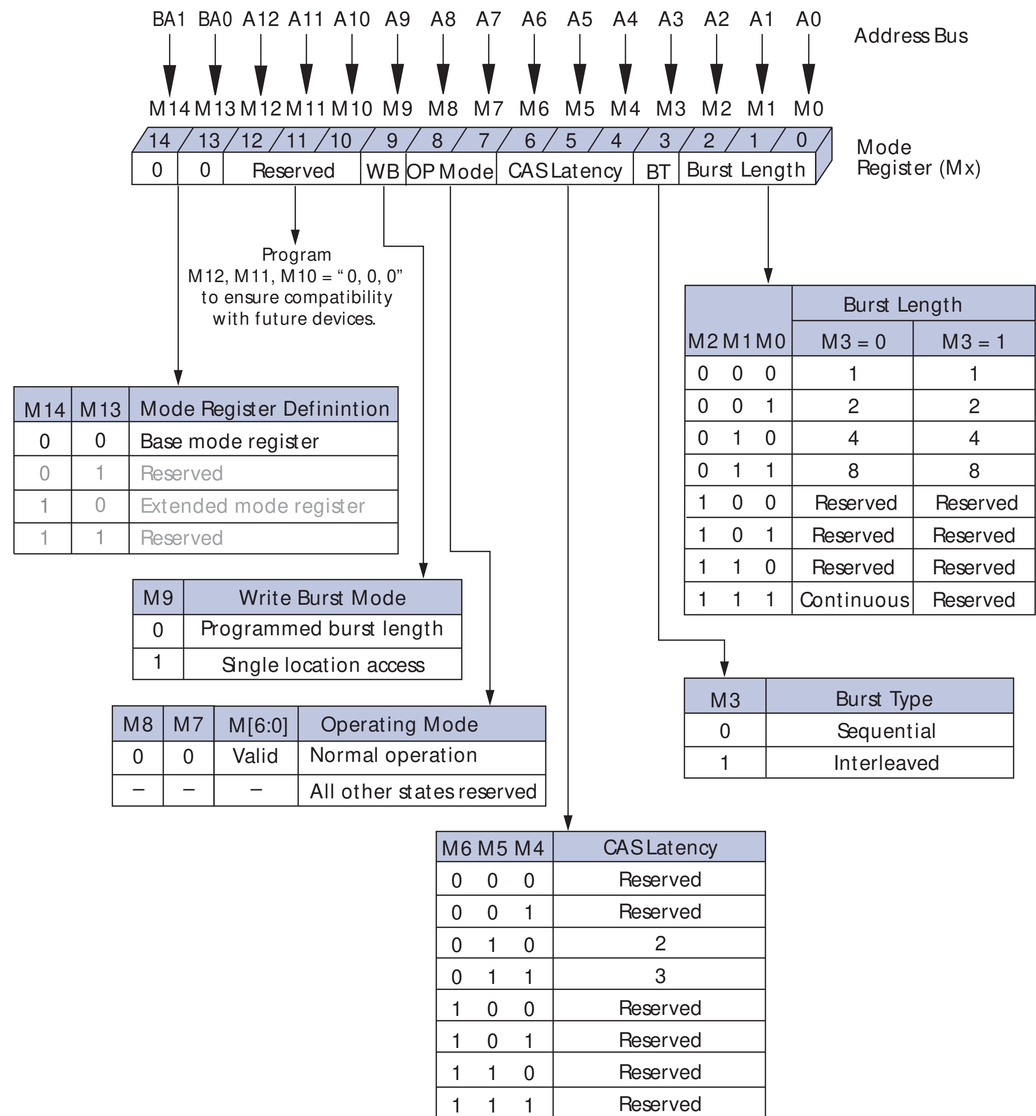
Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the BL, the burst type, and the starting column address, as shown in Table 4 on page 15.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Figure 6: Mode Register Definition



M14	M13	Mode Register Defininition
0	0	Base mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

M9	Write Burst Mode
0	Programmed burst length
1	Single location access

M8	M7	M[6:0]	Operating Mode
0	0	Valid	Normal operation
–	–	–	All other states reserved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Continuous	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Table 4: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Continuous Page	n = A[8:0]			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4..., ...Cn - 1, Cn...	Not supported

CAS Latency (CL)

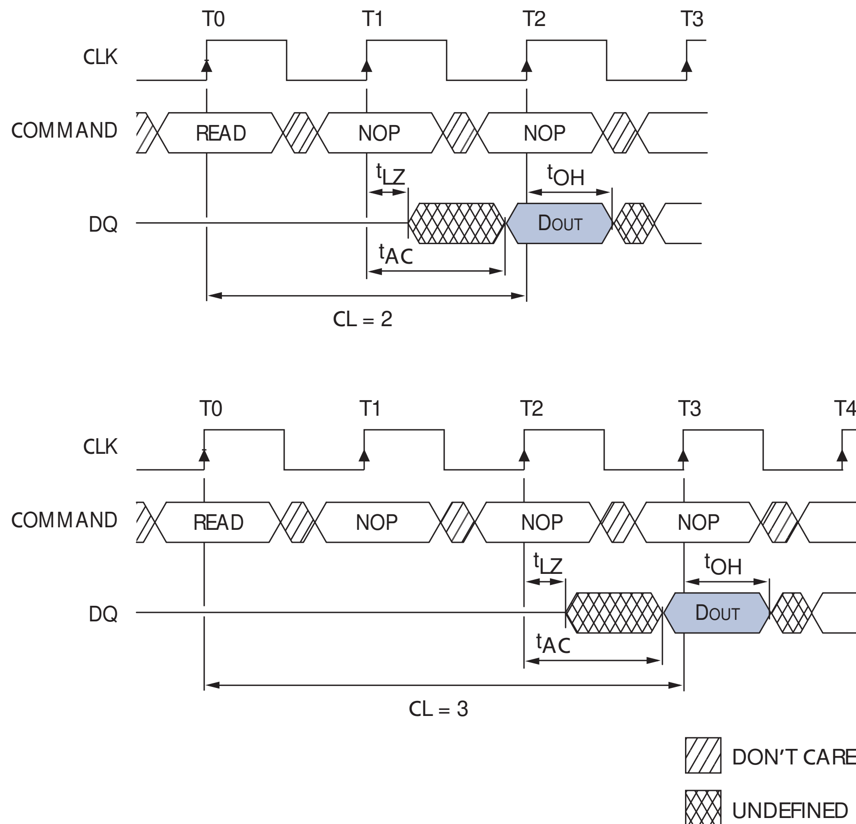
The CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge $n + m$. The DQs will start driving as a result of the clock edge one cycle earlier ($n + m - 1$), and provided that the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 7 on page 16.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Figure 7: CAS Latency



Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the BL programmed via M[2:0] applies to both READ and WRITE bursts; when M9 = 1, the programmed BL applies to READ bursts, but write accesses are single-location accesses.

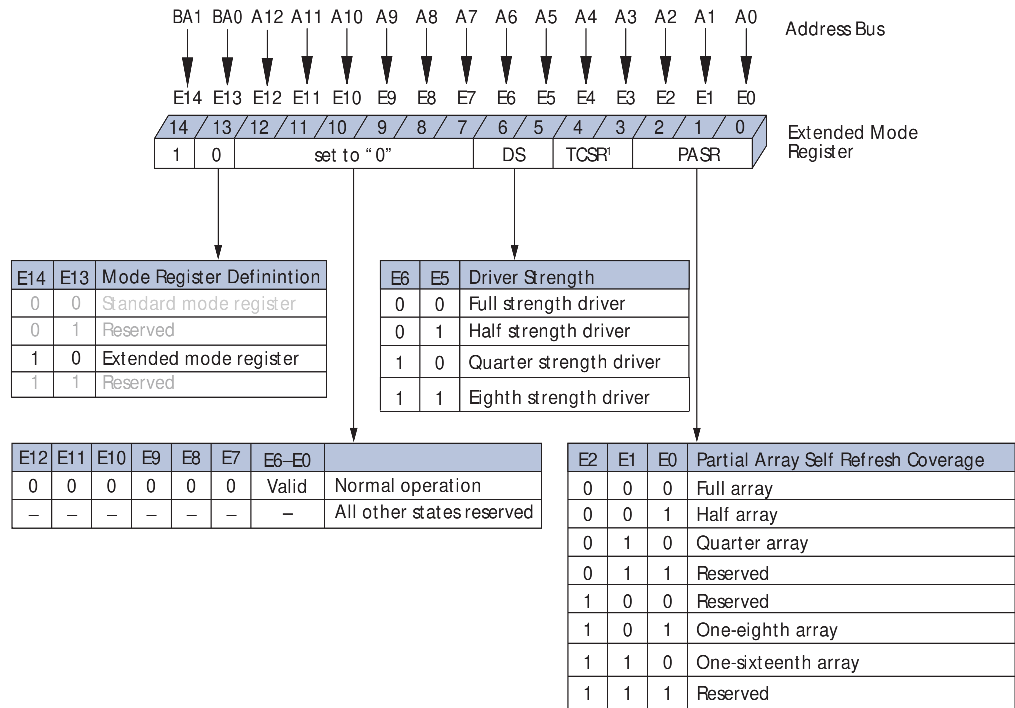
Extended Mode Register (EMR)

The low-power EMR controls the functions beyond those controlled by the mode register. These additional functions are special features of the mobile device. They include temperature-compensated self refresh (TCSR) control, partial-array self refresh (PASR), and output drive strength.

The low-power EMR is programmed via the MODE REGISTER SET command and retains the stored information until it is programmed again or the device loses power.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Figure 8: EMR Definition



E14	E13	Mode Register Definintion
0	0	Standard mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

E6	E5	Driver Strength
0	0	Full strength driver
0	1	Half strength driver
1	0	Quarter strength driver
1	1	Eighth strength driver

E12	E11	E10	E9	E8	E7	E6–E0	
0	0	0	0	0	0	Valid	Normal operation
–	–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial Array Self Refresh Coverage
0	0	0	Full array
0	0	1	Half array
0	1	0	Quarter array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array
1	1	0	One-sixteenth array
1	1	1	Reserved

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. Once the values are entered, the EMR settings will be retained even after exiting deep power-down mode.

Temperature-Compensated Self Refresh (TCSR)

On this version of the Mobile SDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Therefore, it is recommended not to program or use the temperature-compensated self refresh control bits in the extended mode register.

Programming of the TCSR bits has no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the partial-array self refresh (PASR) feature allows the controller to select the amount of memory that will be refreshed during self refresh. The following refresh options are available.

1. All banks (banks 0, 1, 2, and 3).
2. Two banks (banks 0 and 1; BA1 = 0).
3. One bank (bank 0; BA1 = BA0 = 0).
4. Half bank (bank 0; BA1 = BA0 = row address MSB = 0).
5. Quarter bank (bank 0; BA1 = BA0; row address MSB = row address MSB -1 = 0).

WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during self refresh. It is important to note that data in banks 2 and 3 will be lost when the two-bank option is used.

Driver Strength

Bits E5 and E6 of the EMR can be used to select the driver strength of the DQ outputs. This value should be set according to the application's requirements.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Commands

Table 5 provides a quick reference of available commands. This is followed by a written description of each command. Three additional truth tables appear following "Operations" on page 23. These tables provide current state/next state information.

Table 5: Truth Table – Commands and DQM Operation
Notes 1 and 2 apply to all commands

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	4
NO OPERATION (NOP)	L	H	H	H	X	X	X	4
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	5
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/Col	X	6
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/Col	Valid	6
BURST TERMINATE or deep power-down (Enter deep power-down mode)	L	H	H	L	X	X	X	3, 7, 8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	9
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	10, 11
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	12
Write enable/output enable	X	X	X	X	L	X	Active	
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and deep power-down.
2. All states and sequences not shown are reserved and/or illegal.
3. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQs column reads a don't care state to illustrate that the BURST TERMINATE command can occur when there is no data present.
4. DESELECT and NOP are functionally interchangeable.
5. BA[1:0] provide bank address and A[12:0] provide row address.
6. BA[1:0] provide bank address; A[9:0] provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
7. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
8. This command is a BURST TERMINATE if CKE is HIGH, deep power-down if CKE is LOW.
9. A10 LOW: BA[1:0] determine which bank is precharged. A10 HIGH: all banks are precharged and BA[1:0] are "Don't Care."
10. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
11. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
12. BA[1:0] select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA[1:0] are reserved.) A[12:0] provide the op-code to be written to the selected mode register.

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER (LMR)

The mode register is loaded via inputs A[12:0] and BA[1:0]. (See "Mode Register" on page 13.) The LMR and LOAD EXTENDED MODE REGISTER (LEMR) commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA[1:0] inputs selects the bank, and the address provided selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA[1:0] inputs selects the bank, and the address provided selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA[1:0] inputs selects the bank, and the address provides the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA[1:0] select the bank. Otherwise BA[1:0] are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or continuous page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in “Operations” on page 23.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAM. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP has been met after the PRECHARGE command, as shown in “Operations” on page 23.

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The 256Mb SDRAM requires 8192 AUTO REFRESH cycles every 64ms (^{t}REF). Providing a distributed AUTO REFRESH command every 7.8125µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RFC), once every 64ms.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued every 7.8125µs or less as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the continuous page burst mode, where auto precharge does not apply. Auto precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in "Operations" on page 23.

Deep Power-Down

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power to the memory array. Data will not be retained once the device enters deep power-down mode.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Operations

Bank/Row Activation

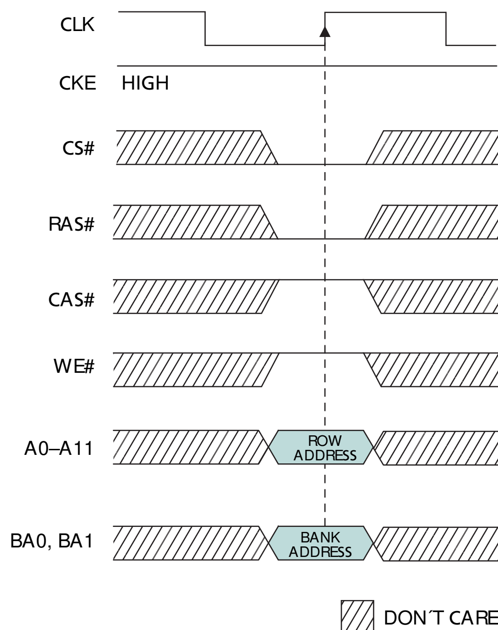
Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 9).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 10 on page 24, which covers any case where $2 < {}^{t}RCD\ (MIN)/{}^{t}CK \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

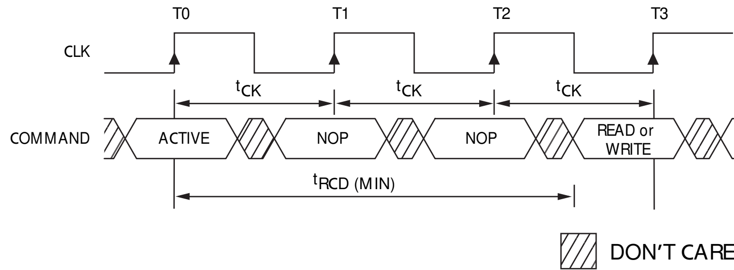
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 9: Activating a Specific Row in a Specific Bank



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Figure 10: Example: Meeting ^{t}RCD (MIN) When 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3



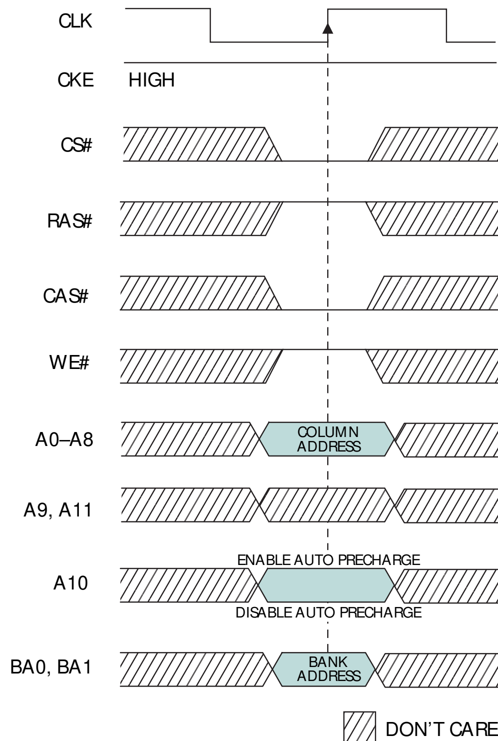
READs

READ bursts are initiated with a READ command, as shown in Figure 11.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CL after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 7 on page 16 shows general timing for each possible CL setting.

Figure 11: READ Command



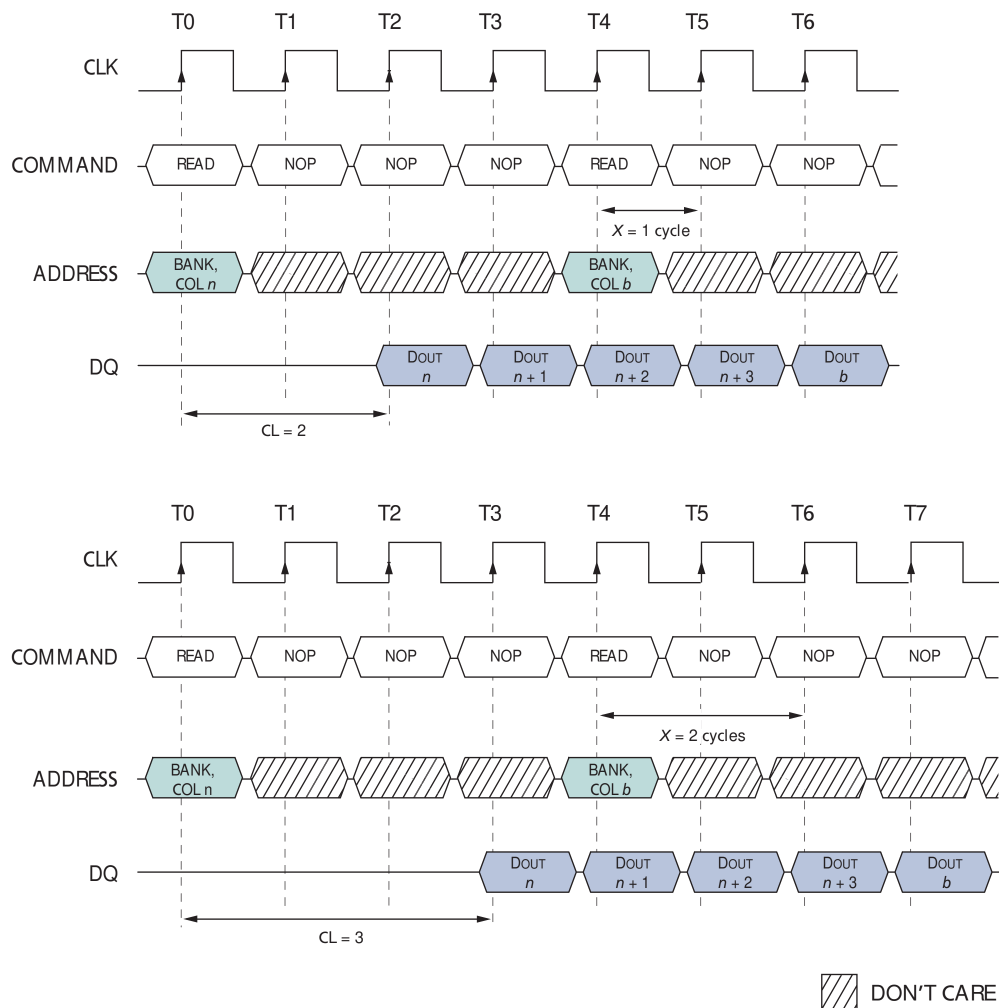
Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A continuous page burst will proceed until terminated (at the end of the page, it will wrap to the start address and continue).

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where x = CL - 1.

Figure 7 on page 16 shows for CL of two and three; data element $n + 3$ is either the last of a burst of four or the last desired of a longer burst. The 256Mb SDRAM uses a pipelined architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 12 on page 25, or each subsequent READ may be performed to a different bank.

Figure 12: Consecutive READ Bursts



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2006 Micron Technology, Inc. All rights reserved.