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SDR SDRAM

MT48LC4M32B2 – 1 Meg x 32 x 4 Banks

Features

- PC100-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh mode (not available on AT devices)
- Auto refresh
  - 64ms, 4096-cycle refresh (commercial and industrial)
  - 16ms, 4096-cycle refresh (automotive)
- LVTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply
- Supports CAS latency (CL) of 1, 2, and 3

Options	Marking
• Configuration	
– 4 Meg x 32 (1 Meg x 32 x 4 banks)	4M32B2
• Package – OCPL[1]	
– 86-pin TSOP II (400 mil)	TG
– 86-pin TSOP II (400 mil) Pb-free	P
– 90-ball VFBGA (8mm x 13mm)	F5
– 90-ball VFBGA (8mm x 13mm) Pb-free	B5
• Timing (cycle time)	
– 6ns (167 MHz)	-6A[2]
– 6ns (167 MHz)	-6[3]
– 7ns (143 MHz)	-7[3]
• Revision	:G/:L
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
– Automotive (–40°C to +105°C)	AT[4]

Notes:
1. Off-center parting line.
2. Available only on Revision L.
3. Available only on Revision G.
4. Contact Micron for availability.

Table 1: Key Timing Parameters

CL = CAS (READ) latency

Speed Grade	Clock Frequency (MHz)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-6A	167	3-3-3	18	18	18
-6	167	3-3-3	18	18	18
-7	143	3-3-3	20	20	21

Table 2: Address Table

Parameter	4 Meg x 32
Configuration	1 Meg x 32 x 4 banks
Refresh count	4K
Row addressing	4K A[11:0]
Bank addressing	4 BA[1:0]
Column addressing	256 A[7:0]

Table 3: 128Mb (x32) SDR Part Numbering

Part Numbers	Architecture
MT48LC4M32B2TG	4 Meg x 32
MT48LC4M32B2P	4 Meg x 32
MT48LC4M32B2F5[1]	4 Meg x 32
MT48LC4M32B2B5[1]	4 Meg x 32

Note: 1. FBGA Device Decoder: www.micron.com/decoder.

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General Description

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM with asynchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 33,554,432-bit banks is organized as 4096 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank; A[11:0] select the row).The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 64Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

The devices offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

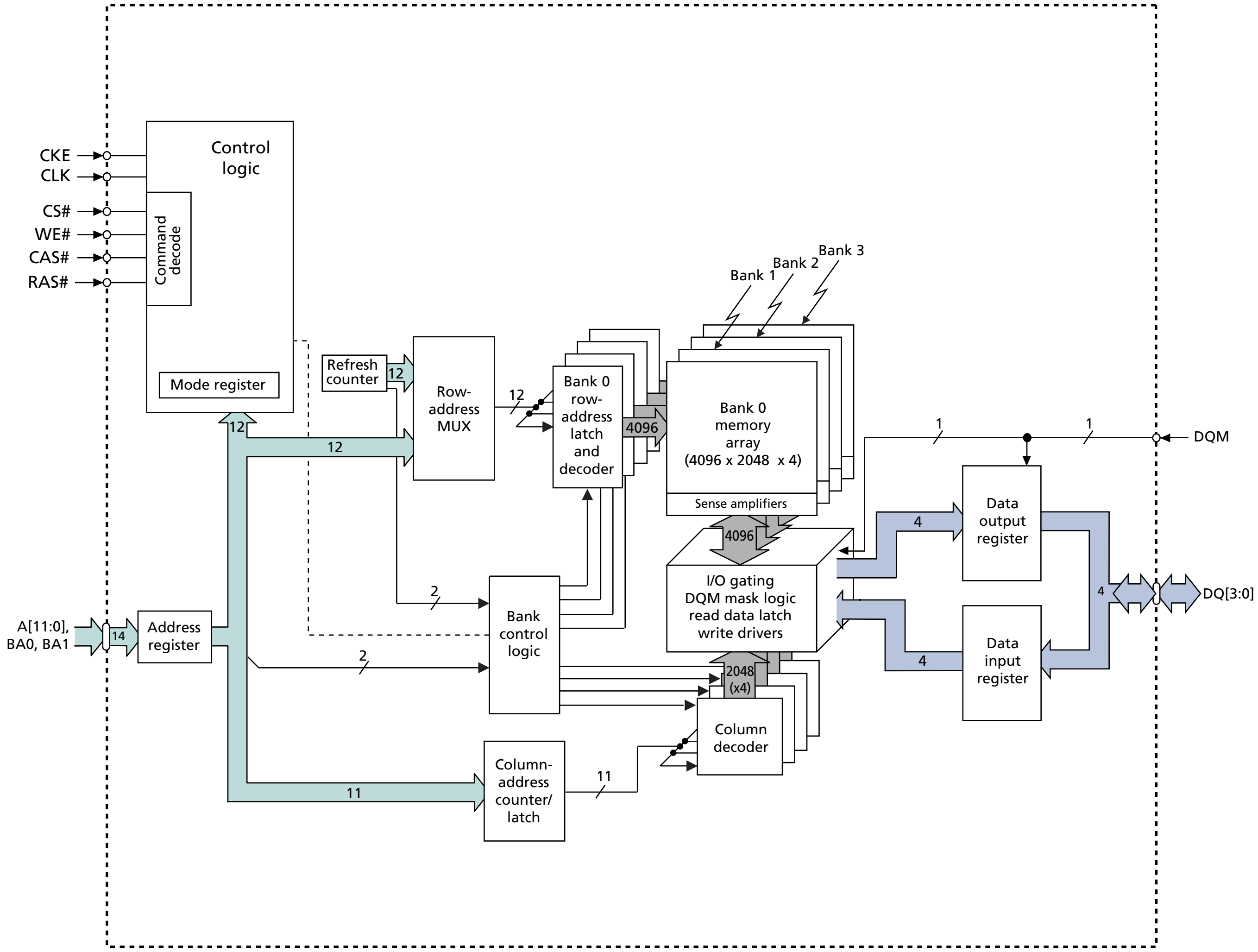
Automotive Temperature

The automotive temperature (AT) option adheres to the following specifications:

- 16ms refresh rate
- Self refresh not supported
- Ambient and case temperature cannot be less than –40°C or greater than 105°C

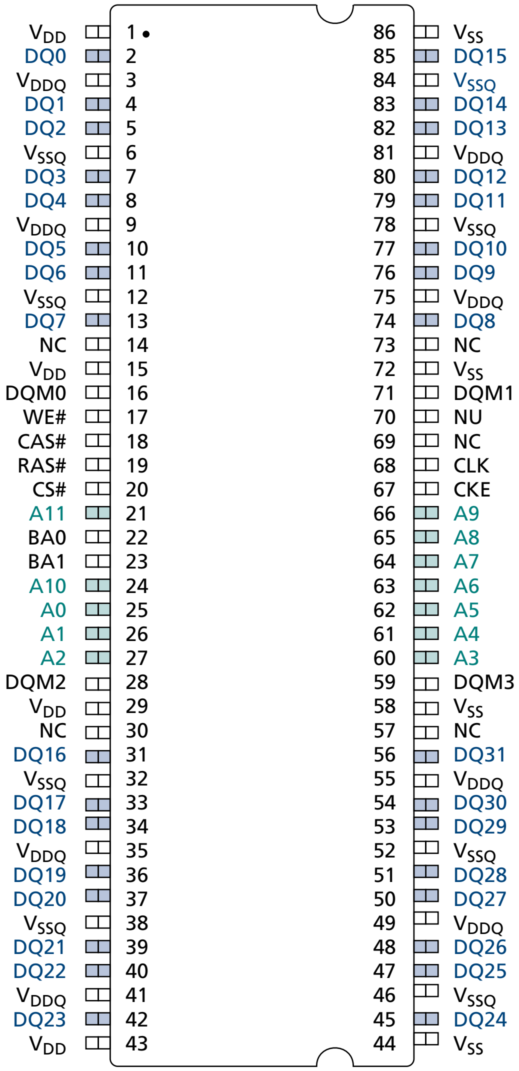
Functional Block Diagram

Figure 1: 4 Meg x 32 Functional Block Diagram



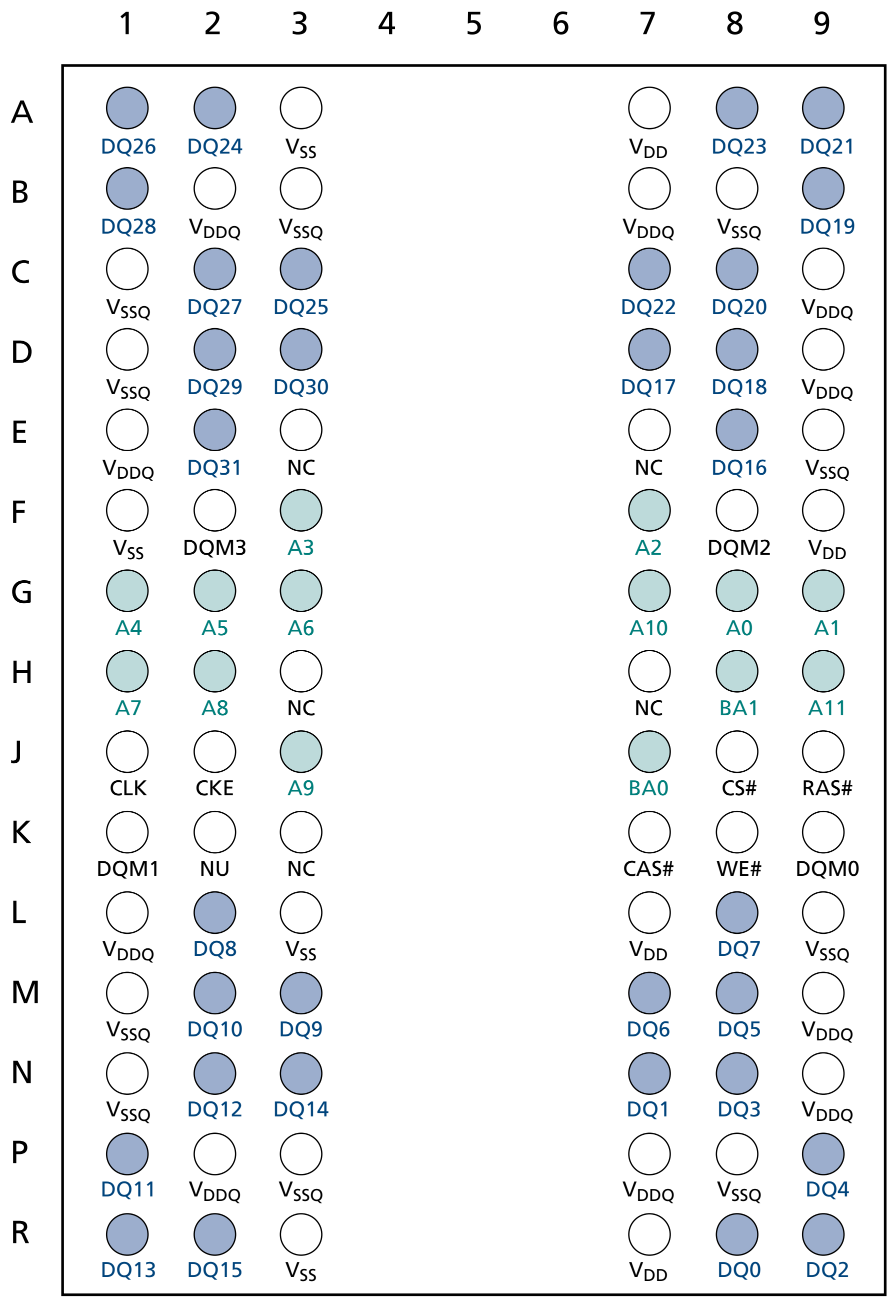
Pin and Ball Assignments and Descriptions

Figure 2: 86-Pin TSOP Pin Assignments (Top View)



Note: 1. Package may or may not be assembled with a location notch.

Figure 3: 90-Ball FBGA Ball Assignments (Top View)



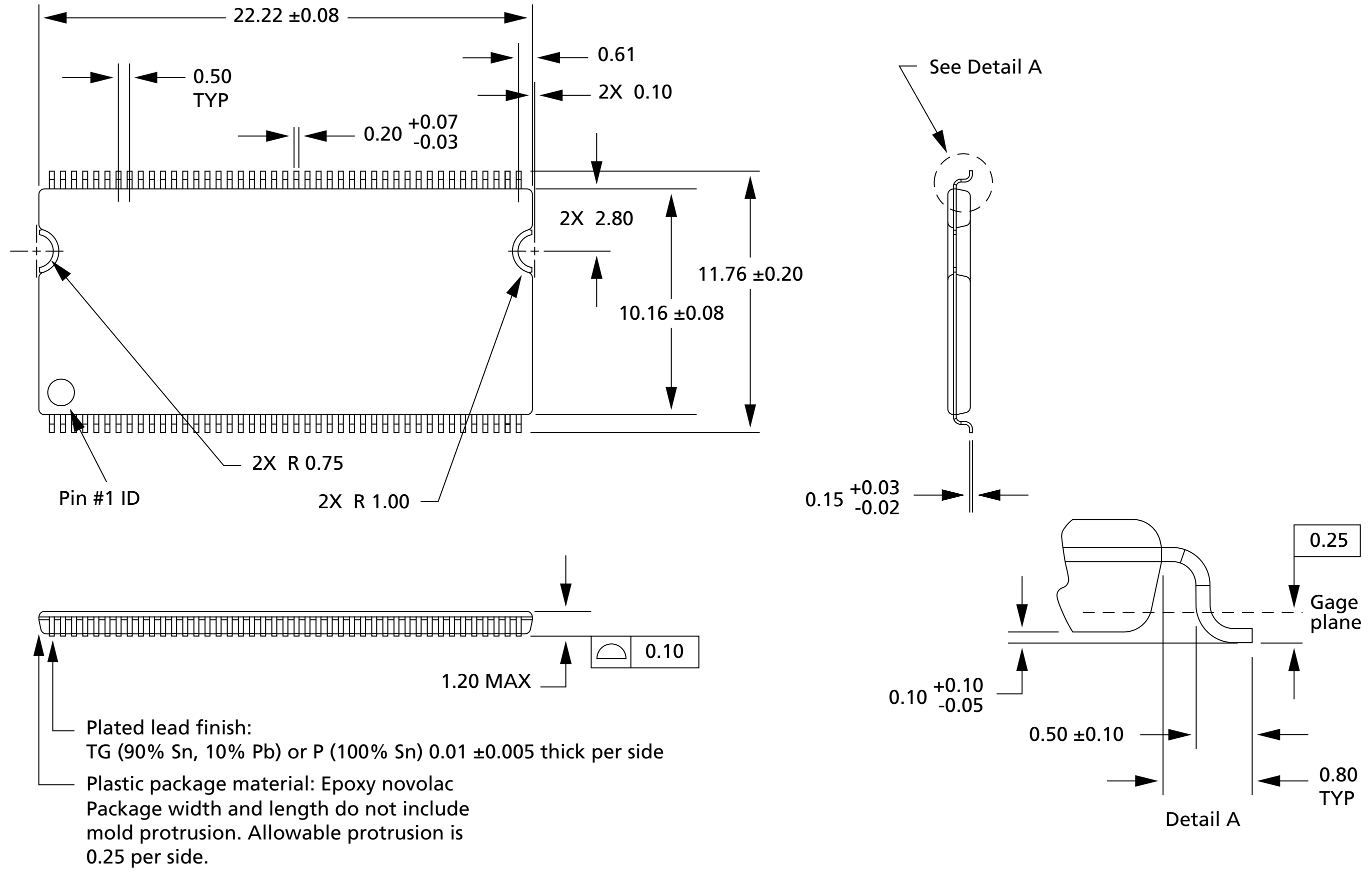
	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	V_{SS}				V_{DD}	DQ23	DQ21
B	DQ28	V_{DDQ}	V_{SSQ}				V_{DDQ}	V_{SSQ}	DQ19
C	V_{SSQ}	DQ27	DQ25				DQ22	DQ20	V_{DDQ}
D	V_{SSQ}	DQ29	DQ30				DQ17	DQ18	V_{DDQ}
E	V_{DDQ}	DQ31	NC				NC	DQ16	V_{SSQ}
F	V_{SS}	DQM3	A3				A2	DQM2	V_{DD}
G	A4	A5	A6				A10	A0	A1
H	A7	A8	NC				NC	BA1	A11
J	CLK	CKE	A9				BA0	CS#	RAS#
K	DQM1	NU	NC				CAS#	WE#	DQM0
L	V_{DDQ}	DQ8	V_{SS}				V_{DD}	DQ7	V_{SSQ}
M	V_{SSQ}	DQ10	DQ9				DQ6	DQ5	V_{DDQ}
N	V_{SSQ}	DQ12	DQ14				DQ1	DQ3	V_{DDQ}
P	DQ11	V_{DDQ}	V_{SSQ}				V_{DDQ}	V_{SSQ}	DQ4
R	DQ13	DQ15	V_{SS}				V_{DD}	DQ0	DQ2

Table 4: Pin/Ball Descriptions

Symbol	Type	Description
CLK	Input	**Clock:** CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	**Clock enable:** CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while CS# is HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	**Command inputs:** CAS#, RAS#, and WE# (along with CS#) define the command being entered.
DQM[3:0]	Input	**Input/output mask:** DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are High-Z (two-clock latency) during a READ cycle. DQM0 corresponds to DQ[7:0], DQM1 corresponds to DQ[15:8], DQM2 corresponds to DQ[23:16], and DQM3 corresponds to DQ[31:24]. DQM[3:0] are considered the same state when referenced as DQM.
BA[1:0]	Input	**Bank address inputs:** BA[1:0] define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A[11:0]	Input	**Address inputs:** A[11:0] are sampled during the ACTIVE command (row address A[10:0]) and READ or WRITE command (column address A[7:0] with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA[1:0] (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ[31:0]	Input/ Output	**Data input/output:** Data bus.
NC	–	**No connect:** These pins should be left unconnected. Pin 70 is reserved for SSTL reference voltage supply.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Provides isolated ground to DQs for improved noise immunity.
V_{DD}	Supply	**Power supply:** 3.3V ±0.3V.
V_{SS}	Supply	Ground.

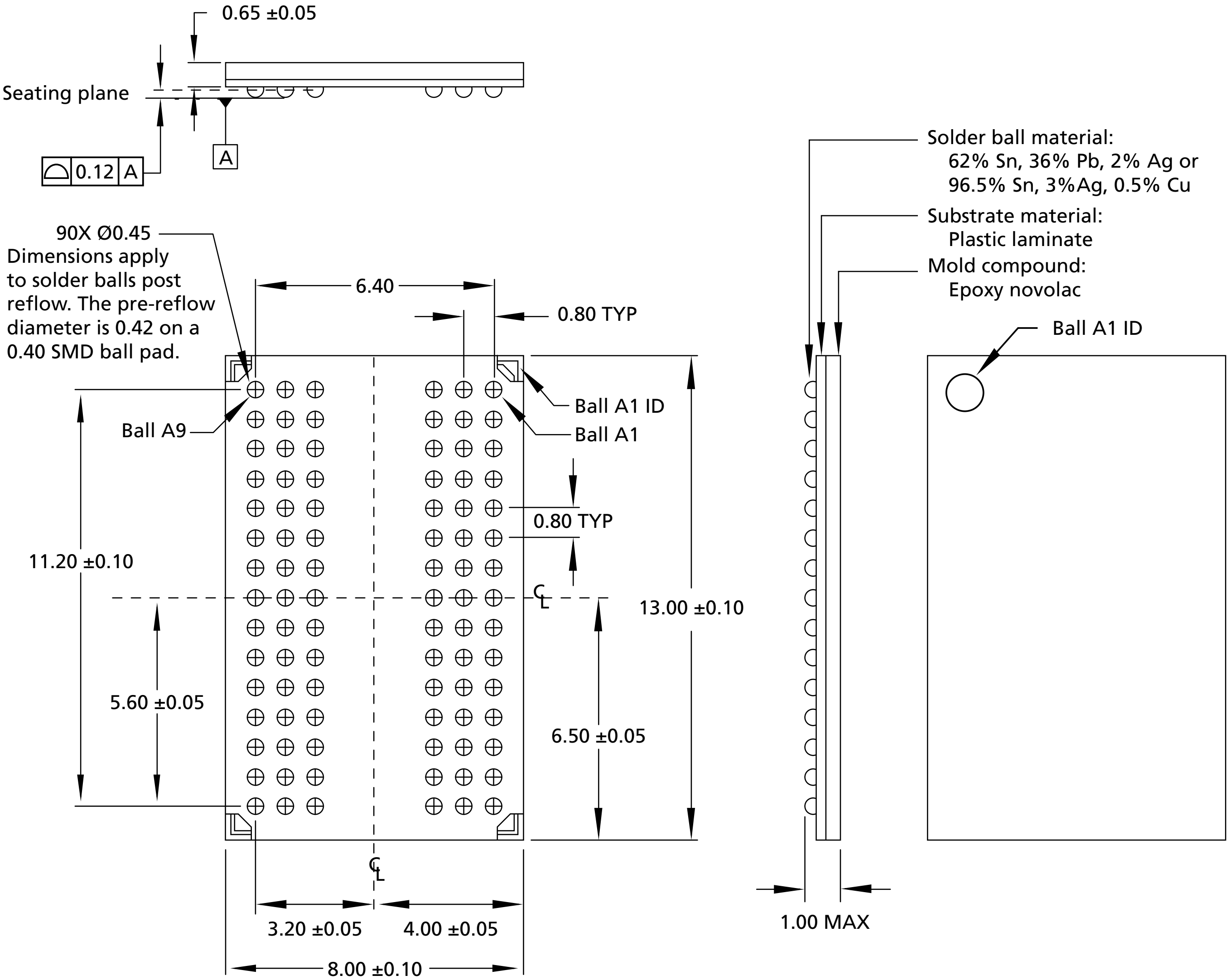
Package Dimensions

Figure 4: 86-Pin Plastic TSOP II (400 mil) – Package Codes TG/P



Notes:
1. All dimensions are in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. "2X" means the notch is present in two locations (both ends of the device).
4. Package may or may not be assembled with a location notch.

Figure 5: 90-Ball VFBGA (8mm x 13mm)



Notes:

1. All dimensions are in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. Recommended pad size for PCB is 0.33mm ±0.025mm.

Temperature and Thermal Impedance

It is imperative that the SDRAM device's temperature specifications, shown in Temperature Limits below, be maintained to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 6 (page 15) for the applicable die revision and packages being made available. These thermal impedance values vary according to the density, package, and particular design used for each device.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed in Table 6 (page 15). To ensure the compatibility of current and future designs, contact Micron Applications Engineering to confirm thermal impedance values.

The SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Temperature Limits

Parameter		Symbol	Min	Max	Unit	Notes
Operating case temperature	Commercial	T_C	0	80	°C	1, 2, 3, 4
	Industrial		–40	90		
	Automotive		–40	105		
Junction temperature	Commercial	T_J	0	85	°C	3
	Industrial		–40	95		
	Automotive		–40	110		
Ambient temperature	Commercial	T_A	0	70	°C	3, 5
	Industrial		–40	85		
	Automotive		–40	105		
Peak reflow temperature		T_{PEAK}	–	260	°C	

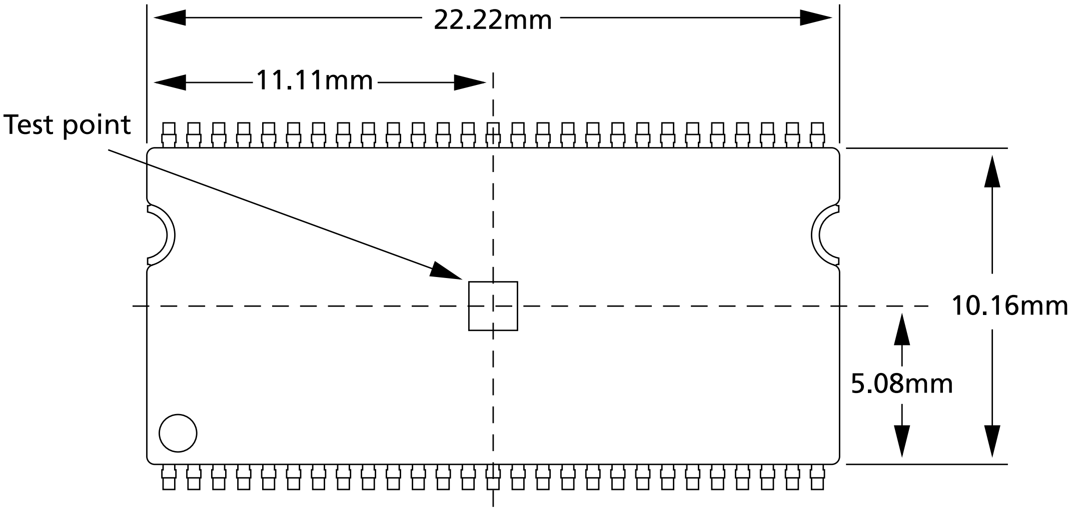
Notes:
1. MAX operating case temperature T_C is measured in the center of the package on the top side of the device, as shown in Figure 6 (page 15) and Figure 7 (page 16).
2. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
3. All temperature specifications must be satisfied.
4. The case temperature should be measured by gluing a thermocouple to the top-center of the component. This should be done with a 1mm bead of conductive epoxy, as defined by the JEDEC EIA/JESD51 standards. Take care to ensure that the thermocouple bead is touching the case.
5. Operating ambient temperature surrounding the package.

Table 6: Thermal Impedance Simulated Values

Die Revision	Package	Substrate	ΘJA (°C/W) Airflow = 0m/s	ΘJA (°C/W) Airflow = 1m/s	ΘJA (°C/W) Airflow = 2m/s	ΘJB (°C/W)	ΘJC (°C/W)
G	86-pin TSOP	Low Conductivity	82.2	65	59.7	49.4	10.3
		High Conductivity	55	47.2	45.1	40.6	
	90-ball VFBGA	Low Conductivity	64.6	50.8	45.3	37.5	1.8
		High Conductivity	48.2	41.1	38.1	32.1	
L	86-pin TSOP	Low Conductivity	122.3	105.6	98.1	89.5	20.7
		High Conductivity	101.9	93.5	88.8	87.6	
	90-ball VFBGA	Low Conductivity	76.8	63.1	63.1	50.1	10.4
		High Conductivity	56.3	49.6	49.6	43.5	

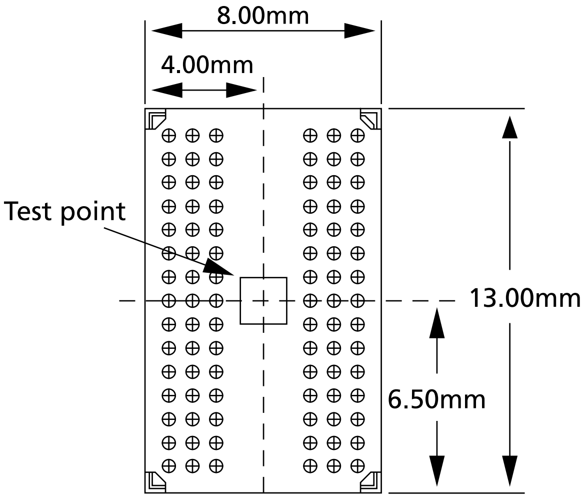
Notes:
1. For designs expected to last beyond the die revision listed, contact Micron Applications Engineering to confirm thermal impedance values.
2. Thermal resistance data is sampled from multiple lots, and the values should be viewed as typical.
3. These are estimates; actual results may vary.

Figure 6: Example: Temperature Test Point Location, 54-Pin TSOP (Top View)



Note: 1. Package may or may not be assembled with a location notch.

Figure 7: Example: Temperature Test Point Location, 90-Ball VFBGA (Top View)



Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Voltage/Temperature	Symbol	Min	Max	Unit
Voltage on V_{DD}, V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	–1	4.6	V
Voltage on inputs, NC, or I/O pins relative to V_{SS}	V_{IN}	–1	4.6	V
Storage temperature (plastic)	T_{STG}	–55	150	°C
Power dissipation		–	1	W

Table 8: DC Electrical Characteristics and Operating Conditions

Notes 1, 2 apply to all parameters and conditions; V_{DD}, V_{DDQ} = 3.3V ±0.3V

Parameter/Condition		Symbol	Min	Max	Unit	Notes
Supply voltage		V_{DD}, V_{DDQ}	3	3.6	V	
Input high voltage: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	3
Input low voltage: Logic 0; All inputs		V_{IL}	–0.3	0.8	V	3
Output high voltage: I_{OUT} = –4mA		V_{OH}	2.4	–	V	
Output low voltage: I_{OUT} = 4mA		V_{OL}	–	0.4	V	
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)		I_L	–5	5	µA	
Output leakage current: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}		I_{OZ}	–5	5	µA	
Operating temperature:	Commercial	T_A	0	70	°C	
	Industrial	T_A	–40	85	°C	
	Automotive	T_A	–40	105	°C	

Notes:
1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured:
   0°C ≤ T_A ≤ +70°C (commercial)
   –40°C ≤ T_A ≤ +85°C (industrial)
   –40°C ≤ T_A ≤ +105°C (automotive)
3. Based on ^tCK = 143 MHz for -7, 167 MHz for -6/6A.

Table 9: Capacitance

Parameter	Symbol	Min	Max	Unit
Input capacitance: CLK	C_{I1}	2.5	3.5	pF
Input capacitance: All other input-only pins	C_{I2}	2.5	3.8	pF
Input/output capacitance: DQs	C_{IO}	4	6	pF

Electrical Specifications – I_{DD} Parameters

Table 10: I_{DD} Specifications and Conditions – Revision G

Notes 1–5 apply to all parameters and conditions; V_{DD}, V_{DDQ} = 3.3V ±0.3V

Parameter/Condition		Symbol	Max -6	Max -7	Unit	Notes
Operating current: Active mode; Burst = 2; READ or WRITE; ^tRC = ^tRC (MIN); CL = 3		I_{DD1}	190	165	mA	6, 7, 8, 9
Standby current: Power-down mode; CKE = LOW; All banks idle		I_{DD2}	2	2	mA	
Standby current: Active mode; CS# = HIGH; CKE = HIGH; All banks active after ^tRCD met; No accesses in progress		I_{DD3}	65	55	mA	8, 9
Operating current: Burst mode; Continuous burst; READ or WRITE; All banks active; CL = 3		I_{DD4}	195	175	mA	6, 7, 8, 9
Auto refresh current: CS# = HIGH; CKE = HIGH; CL = 3	^tRFC = ^tRFC (MIN)	I_{DD5}	320	320	mA	6, 7, 8, 9, 10
Self refresh current: CKE ≤ 0.2V		I_{DD6}	2	2	mA	11, 12

Table 11: I_{DD} Specifications and Conditions – Revision L

Notes 1–5 apply to all parameters and conditions; V_{DD}, V_{DDQ} = 3.3V ±0.3V

Parameter/Condition		Symbol	Max -6A	Unit	Notes
Operating current: Active mode; Burst = 2; READ or WRITE; ^tRC = ^tRC (MIN); CL = 3		I_{DD1}	120	mA	6, 7, 8, 9
Standby current: Power-down mode; CKE = LOW; All banks idle		I_{DD2}	2.5	mA	
Standby current: Active mode; CS# = HIGH; CKE = HIGH; All banks active after ^tRCD met; No accesses in progress		I_{DD3}	45	mA	8, 9
Operating current: Burst mode; Continuous burst; READ or WRITE; All banks active; CL = 3		I_{DD4}	120	mA	6, 7, 8, 9
Auto refresh current: CS# = HIGH; CKE = HIGH; CL = 3	^tRFC = ^tRFC (MIN)	I_{DD5}	180	mA	6, 7, 8, 9, 10
Self refresh current: CKE ≤ 0.2V		I_{DD6}	3	mA	11, 12

Notes:
1. All voltages referenced to V_{SS}.
2. I_{DD} specifications are tested after the device is properly initialized.
3. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured for IT parts:
   0°C ≤ T_A ≤ +70°C
   –40°C ≤ T_A ≤ +85°C.
4. ^tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^tOH before going High-Z.
5. Other input signals are allowed to transition no more than once in any two-clock period and are otherwise at valid V_{IH} or V_{IL} levels.
6. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
7. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.

8. The I_{DD} current will decrease as CL is reduced. This is due to the fact that the maximum cycle rate is slower as CL is reduced.
9. JEDEC and PC100 specify three clocks.
10. AC timing and I_{DD} tests have V_{IL} = 0.25 and V_{IH} = 2.75, with timing referenced to the 1.5V crossover point.
11. Enables on-chip refresh and address counters.
12. CKE is HIGH during refresh command period ^{t}RFC (MIN), or else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.

Electrical Specifications – AC Operating Conditions

Table 12: Electrical Characteristics and Recommended AC Operating Conditions

Notes 1–6 apply to all parameters and conditions

Parameter		Symbol	-6A^{9}		-6		-7		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Access time from CLK (positive edge)	CL = 3	^{t}AC(3)	–	5.4	–	5.5	–	5.5	ns	
	CL = 2	^{t}AC(2)	–	7.5	–	7.5	–	8	ns	
	CL = 1	^{t}AC(1)	–	17	–	17	–	17	ns	
Address hold time		^{t}AH	0.8	–	1.0	–	1.0	–	ns	
Address setup time		^{t}AS	1.5	–	1.5	–	2	–	ns	
CLK high-level width		^{t}CH	2.5	–	2.5	–	2.75	–	ns	
CLK low-level width		^{t}CL	2.5	–	2.5	–	2.75	–	ns	
Clock cycle time	CL = 3	^{t}CK(3)	6	–	6	–	7	–	ns	10
	CL = 2	^{t}CK(2)	10	–	10^{9}	–	10	–	ns	10
	CL = 1	^{t}CK(1)	20	–	20^{9}	–	20	–	ns	10
CKE hold time		^{t}CKH	0.8	–	1.0	–	1.0	–	ns	
CKE setup time		^{t}CKS	1.5	–	1.5	–	2	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	0.8	–	1.0	–	1.0	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	1.5	–	1.5	–	2	–	ns	
Data-in hold time		^{t}DH	0.8	–	1.0	–	1.0	–	ns	
Data-in setup time		^{t}DS	1.5	–	1.5	–	2	–	ns	
Data-out High-Z time	CL = 3	^{t}HZ(3)	–	5.4	–	5.5	–	5.5	ns	8
	CL = 2	^{t}HZ(2)	–	7.5	–	7.5	–	8	ns	8
	CL = 1	^{t}HZ(1)	–	17	–	17	–	17	ns	8
Data-out Low-Z time		^{t}LZ	1	–	1	–	1	–	ns	
Data-out hold time (load)		^{t}OH	3	–	2	–	2.5	–	ns	
Data-out hold time (no load)		^{t}OH*n*	1.8	–	1.8	–	1.8	–	ns	7
ACTIVE-to-PRECHARGE command		^{t}RAS	42	120,000	42	120,000	42	120,000	ns	
ACTIVE-to-ACTIVE command period		^{t}RC	60	–	60	–	70	–	ns	11
AUTO REFRESH period		^{t}RFC	60	–	60	–	70	–	ns	
ACTIVE-to-READ or WRITE delay		^{t}RCD	18	–	18	–	20	–	ns	
Refresh period (4096 rows)		^{t}REF	–	64	–	64	–	64	ms	
Refresh period – automotive (4096 rows)		^{t}REF$_{AT}$	–	16	–	16	–	16	ms	
PRECHARGE command period		^{t}RP	18	–	18	–	20	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	12	–	12	–	15	–	ns	12
Transition time		^{t}T	0.3	1.2	0.3	1.2	0.3	1.2	ns	3
WRITE recovery time		^{t}WR	1 CLK + 7ns	–	1 CLK + 6ns	–	1 CLK + 7ns	–	^{t}CK	13
			12	–	12	–	14	–	ns	14

Table 12: Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes 1–6 apply to all parameters and conditions

Parameter	Symbol	-6A[9]		-6		-7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Exit SELF REFRESH-to-ACTIVE command	^{t}XSR	67	–	70	–	70	–	ns	15

Table 13: AC Functional Characteristics

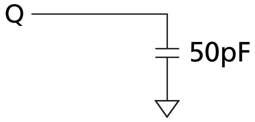
Notes 1–6 apply to all parameters and conditions

Parameter		Symbol	-6	-6A	-7	Unit	Notes
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	1	^{t}CK	
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	1	^{t}CK	16
CKE to clock enable or power-down exit setup mode		^{t}PED	1	1	1	^{t}CK	
DQM to input data delay		^{t}DQD	0	0	0	^{t}CK	
DQM to data mask during WRITEs		^{t}DQM	0	0	0	^{t}CK	
DQM to data High-Z during READs		^{t}DQZ	2	2	2	^{t}CK	
WRITE command to input data delay		^{t}DWD	0	0	0	^{t}CK	
Data-in to ACTIVE command	CL = 3	^{t}DAL(3)	5	4	5	^{t}CK	17
	CL = 2	^{t}DAL(2)	4	4	4	^{t}CK	17
	CL = 1	^{t}DAL(1)	3	3	3	^{t}CK	17
Data-in to PRECHARGE command		^{t}DPL	3	3	3	^{t}CK	18
Last data-in to burst STOP command		^{t}BDL	1	1	1	^{t}CK	
Last data-in to new READ/WRITE command		^{t}CDL	1	1	1	^{t}CK	
Last data-in to burst PRECHARGE command		^{t}RDL	2	2	2	^{t}CK	18
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	2	^{t}CK	
Data-out to High-Z from PRECHARGE command	CL = 3	^{t}ROH(3)	3	3	3	^{t}CK	
	CL = 2	^{t}ROH(2)	2	2	2	^{t}CK	
	CL = 1	^{t}ROH(1)	1	1	1		

Notes:

1. Minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range is ensured:
   $0^\circ C \le T_A \le +70^\circ C$ (commercial)
   $-40^\circ C \le T_A \le +85^\circ C$ (industrial)
   $-40^\circ C \le T_A \le +105^\circ C$ (automotive)
2. Minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range is ensured for IT parts:
   $0^\circ C \le T_A \le +70^\circ C$
   $-40^\circ C \le T_A \le +85^\circ C$
3. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 1ns.

5. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
6. Outputs measured at 1.5V with equivalent load:



7. Parameter guaranteed by design. Note 6 does not apply to ^{t}OHn .
8. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
9. Not applicable for Revision G.
10. V_{IH} overshoot: $V_{IH,max} = V_{DDQ} + 1.2V$ for a pulse width ≤3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{IL,min} = -1.2V$ for a pulse width ≤3ns, and the pulse width cannot be greater than one third of the cycle rate.
11. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.
12. Auto precharge mode only.
13. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
14. ^{t}CK = 7ns for -7, 6ns for -6/6A.
15. Address transitions average on transition every two clocks.
16. Timing is specified by ^{t}CKS. Clock(s) specified as a reference only at minimum cycle rate.
17. Timing is specified by ^{t}WR plus ^{t}RP. Clock(s) specified as a reference only at minimum cycle rate.
18. Timing is specified by ^{t}WR.

Functional Description

In general, 128Mb SDRAM devices (1 Meg x 32 x 4 banks) are quad-bank DRAM that operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 33,554,432-bit banks is organized as 4096 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank; A[11:0] select the row). The address bits (A[7:0]) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Commands

The following table provides a quick reference of available commands, followed by a written description of each command. Additional Truth Tables (Table 15 (page 30), Table 16 (page 32), and Table 17 (page 34)) provide current state/next state information.

Table 14: Truth Table – Commands and DQM Operation

Note 1 applies to all parameters and conditions

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	L	H	H	X	Bank/row	X	2
READ (select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/col	Valid	3
BURST TERMINATE	L	H	H	L	X	X	Active	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	8
Write enable/output enable	X	X	X	X	L	X	Active	9
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	9

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A[0:*n*] provide row address (where A*n* is the most significant address bit), BA0 and BA1 determine which bank is made active.
3. A[0:*i*] provide column address (where *i* = the most significant column address for a given device configuration). A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature. BA0 and BA1 determine which bank is being read from or written to.
4. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQ column reads a “Don’t Care” state to illustrate that the BURST TERMINATE command can occur when there is no data present.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: all banks precharged and BA0, BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. A[11:0] define the op-code written to the mode register.
9. Activates or deactivates the DQ during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the device, regardless of whether the CLK signal is enabled. The device is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to the selected device (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER (LMR)

The mode registers are loaded via inputs A[*n:0*] (where A*n* is the most significant address term), BA0, and BA1(see Mode Register (page 37)). The LOAD MODE REGISTER command can only be issued when all banks are idle and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to activate a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

Figure 8: ACTIVE Command