Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SDR SDRAM

MT48LC128M4A2 – 32 Meg x 4 x 4 banks
MT48LC64M8A2 – 16 Meg x 8 x 4 banks
MT48LC32M16A2 – 8 Meg x 16 x 4 banks

Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh mode
- Auto refresh
  - 64ms, 8192-cycle refresh (commercial and industrial)
- LVTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply

Options — Marking

- Configurations
  - 128 Meg x 4 (32 Meg x 4 x 4 banks) — 128M4
  - 64 Meg x 8 (16 Meg x 8 x 4 banks) — 64M8
  - 32 Meg x 16 (8 Meg x 16 x 4 banks) — 32M16
- Write recovery (^{t}WR)
  - ^{t}WR = 2 CLK[1] — A2
- Plastic package – OCPL[2]
  - 54-pin TSOP II (400 mil) (standard) — TG
  - 54-pin TSOP II (400 mil) Pb-free — P
- Timing – cycle time
  - 7.5ns @ CL = 3 (PC133) — -75
  - 7.5ns @ CL = 2 (PC133) — -7E[3]
- Self refresh
  - Standard — None
  - Low power — L[4]
- Operating temperature range
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C to +85°C) — IT
- Revision — :C

Notes:
1. See technical note TN-48-05 on Micron's Web site.
2. Off-center parting line.
3. Available on x4 and x8 only.
4. Contact Micron for availability.

Table 1: Key Timing Parameters

CL = CAS (READ) latency

Speed Grade	Clock Frequency	Access Time		Setup Time	Hold Time
		CL = 2	CL = 3		
-7E	143 MHz	–	5.4ns	1.5ns	0.8ns
-75	133 MHz	–	5.4ns	1.5ns	0.8ns
-7E	133 MHz	5.4ns	–	1.5ns	0.8ns
-75	100 MHz	6ns	–	1.5ns	0.8ns

Table 2: Address Table

Parameter	32 Meg x 4	32 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row addressing	8K A[12:0]	8K A[12:0]	8K A[12:0]
Bank addressing	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]
Column addressing	4K A[9:0], A11, A12	2K A[9:0], A11	1K A[9:0]

Table 3: 512Mb SDR Part Numbering

Part Numbers	Architecture	Package
MT48LC128M4A2P	128 Meg x 4	54-pin TSOP II
MT48LC128M4A2TG	128 Meg x 4	54-pin TSOP II
MT48LC64M8A2P	64 Meg x 8	54-pin TSOP II
MT48LC64M8A2TG	64 Meg x 8	54-pin TSOP II
MT48LC32M16A2P	32 Meg x 16	54-pin TSOP II
MT48LC32M16A2TG	32 Meg x 16	54-pin TSOP II

Contents

List of Figures

List of Tables

General Description

The 512Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 134,217,728-bit banks is organized as 8192 rows by 4096 columns by 4 bits. Each of the x8's 134,217,728-bit banks is organized as 8192 rows by 2048 columns by 8 bits. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank; A[12:0] select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 512Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 512Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Functional Block Diagrams

Figure 1: 128 Meg x 4 Functional Block Diagram

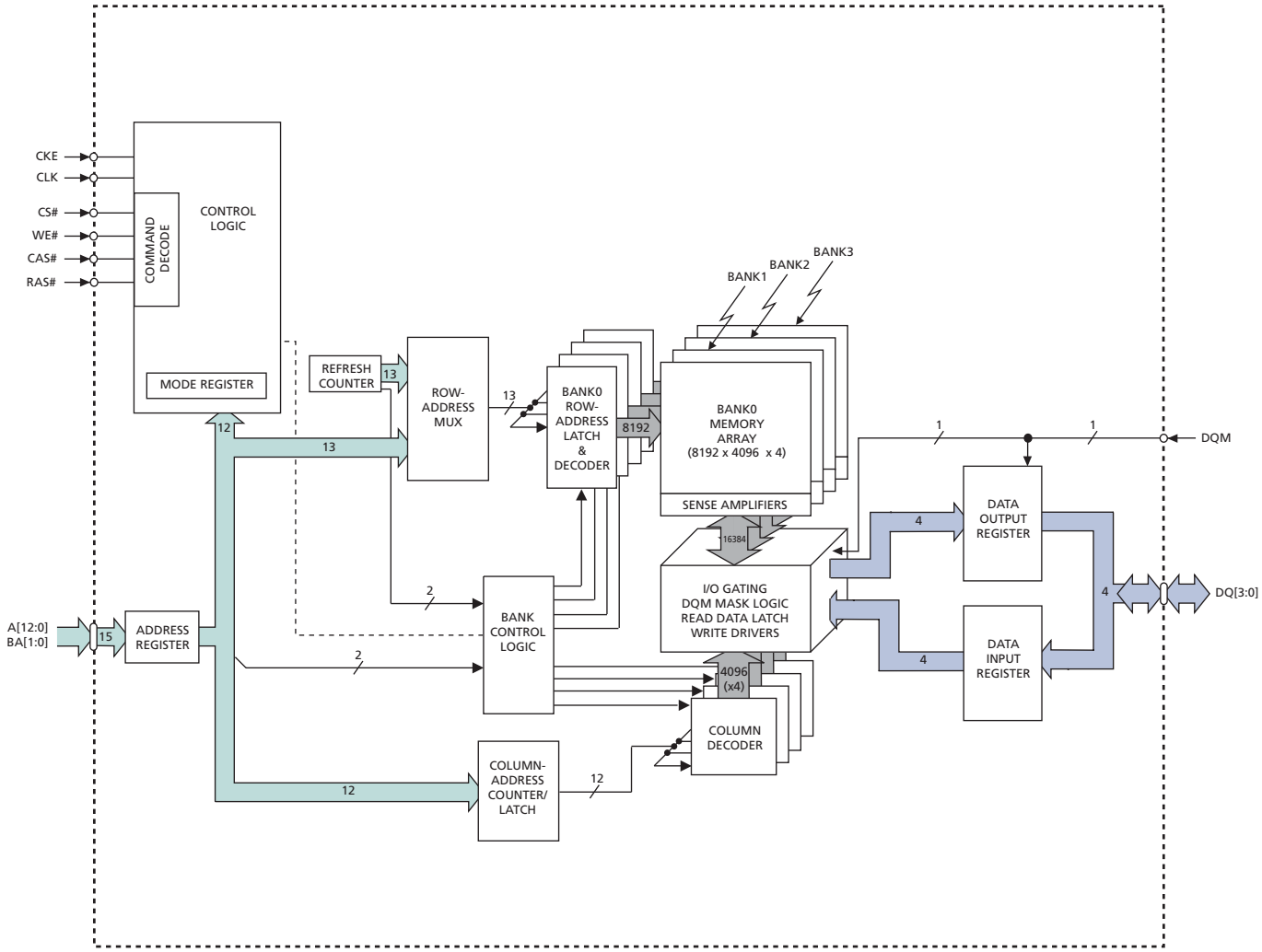


Figure 2: 64 Meg x 8 Functional Block Diagram

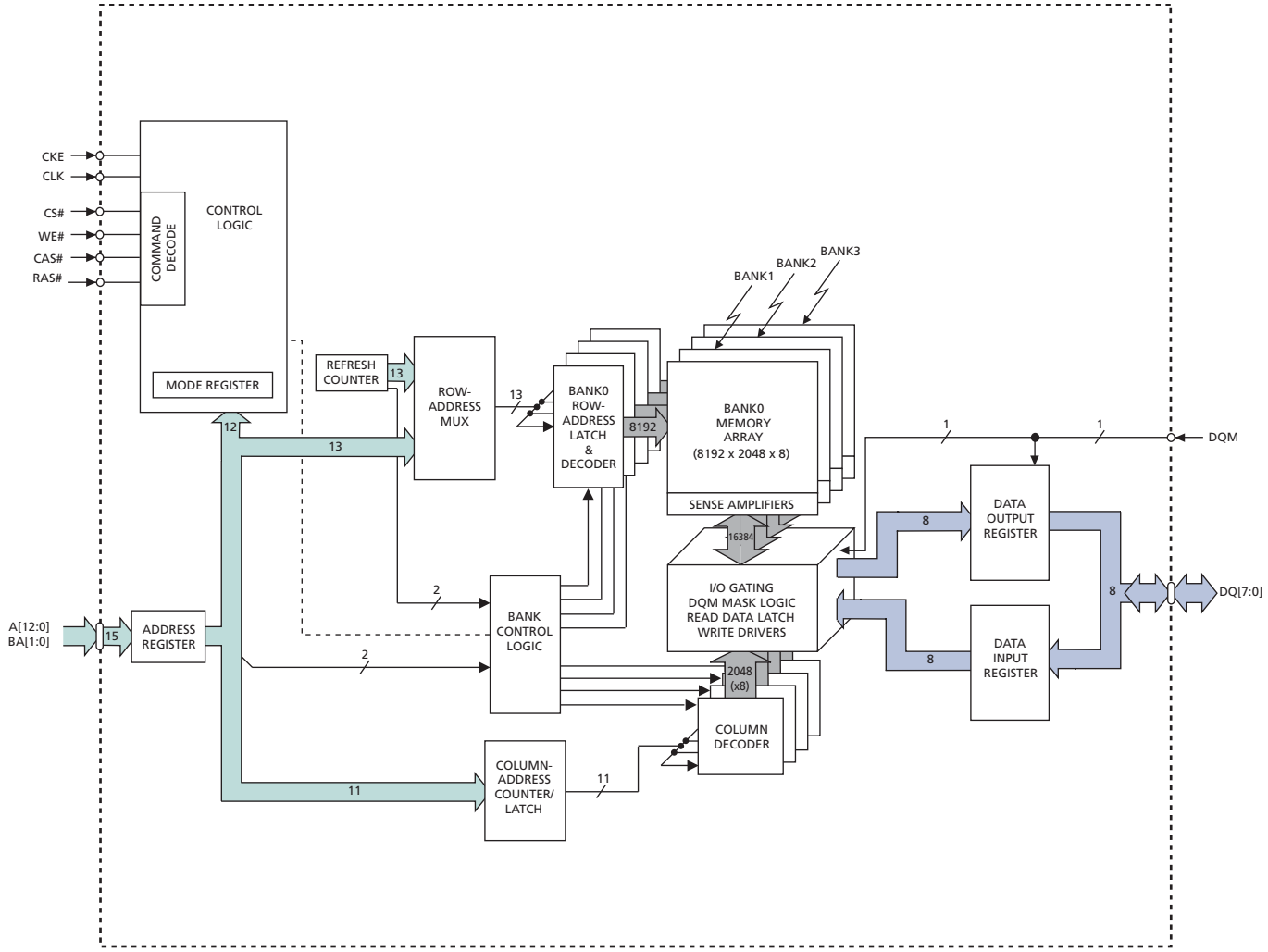
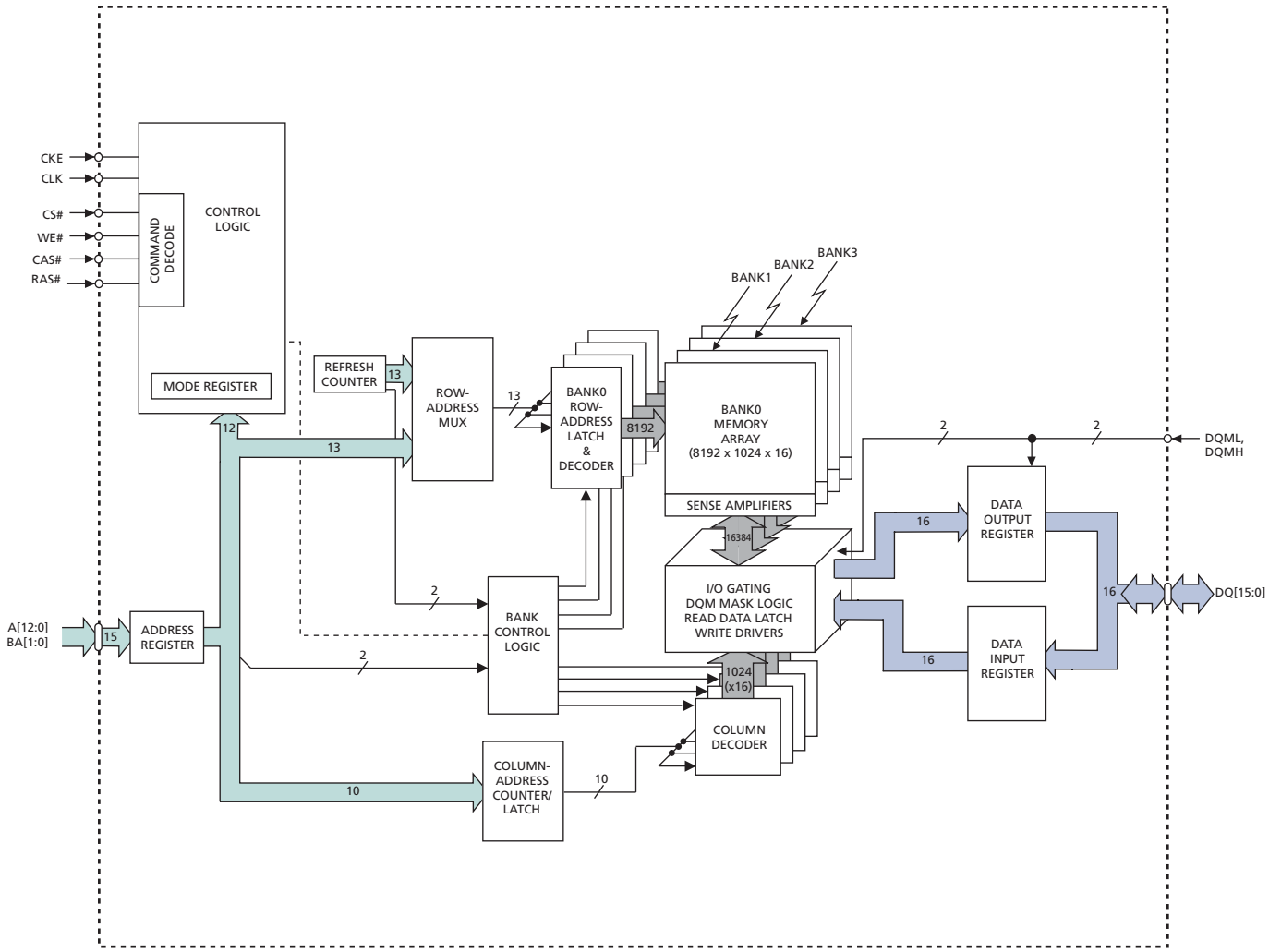
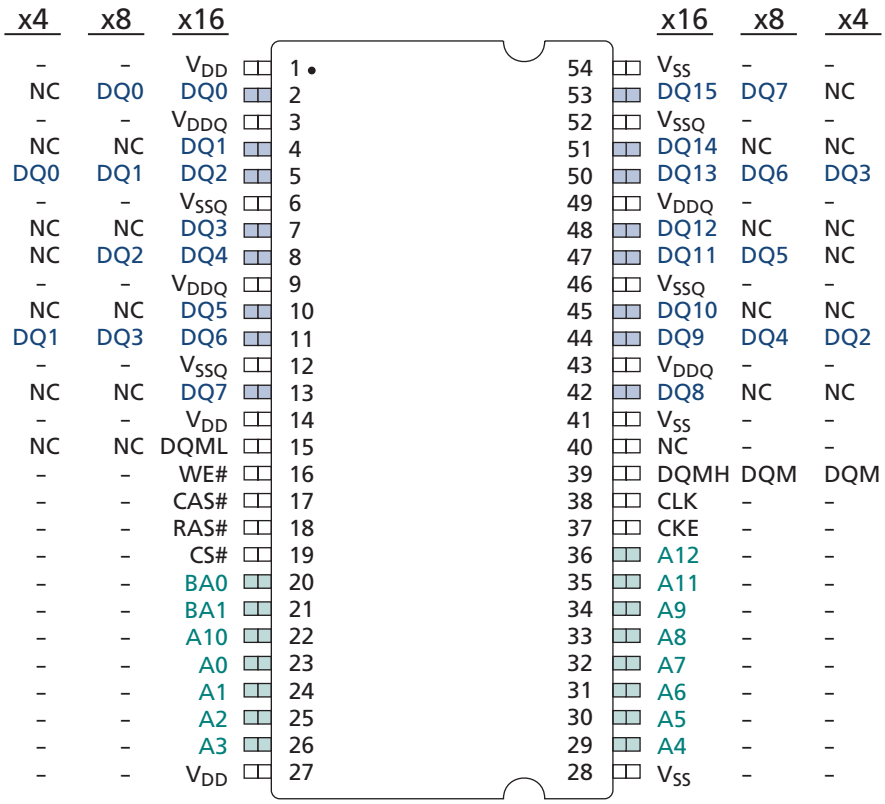


Figure 3: 32 Meg x 16 Functional Block Diagram



Pin and Ball Assignments and Descriptions

Figure 4: 54-Pin TSOP (Top View)



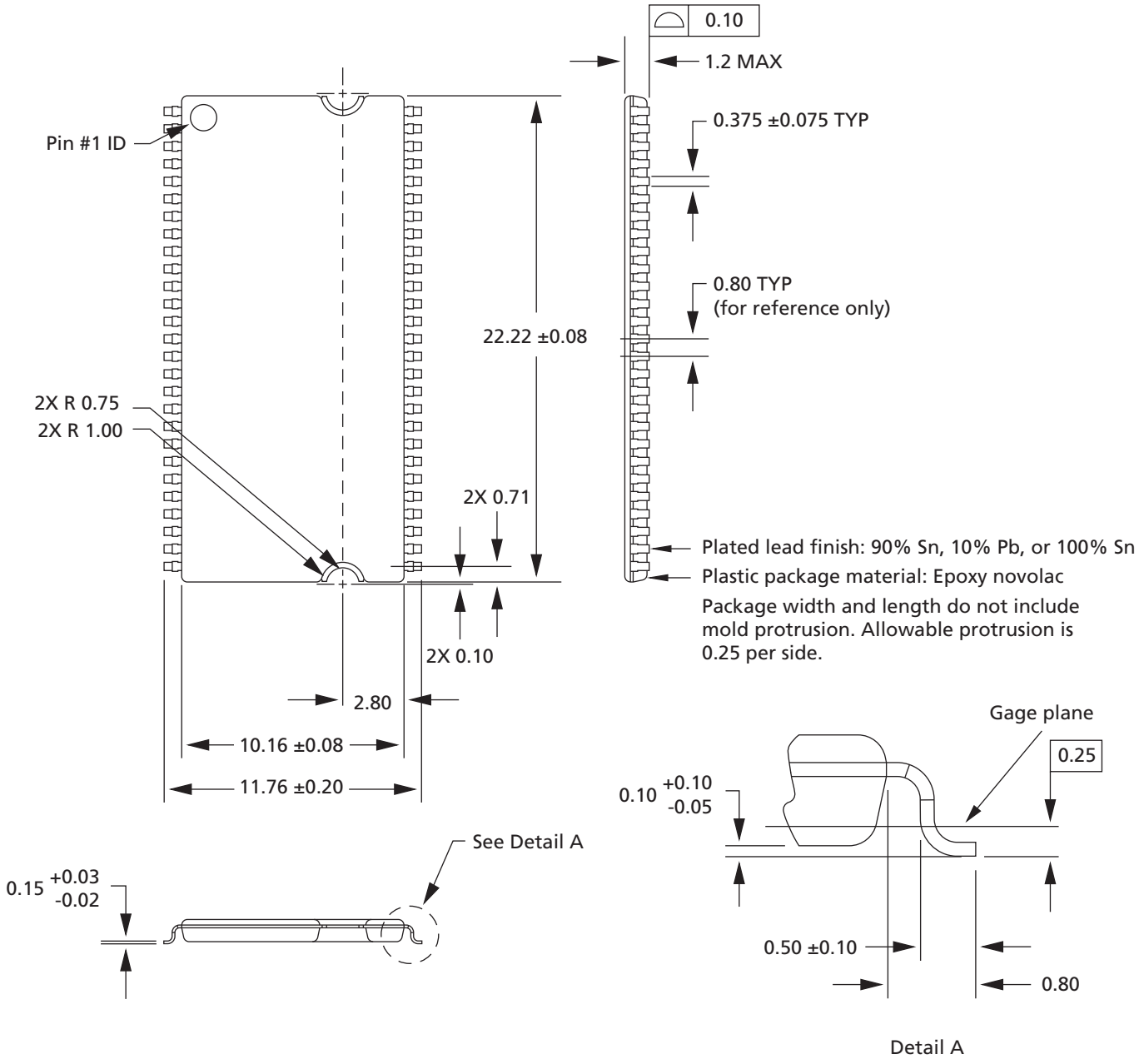
Notes:
1. The # symbol indicates that the signal is active LOW. A dash (-) indicates that the x8 and x4 pin function is the same as the x16 pin function.
2. Package may or may not be assembled with a location notch.

Table 4: Pin and Ball Descriptions

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while CS# is HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
x4, x8: DQM x16: DQML, DQMH LDQM, UDQM (54-ball)	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ[7:0], and DQMH corresponds to DQ[15:8]. DQML and DQMH are considered same state when referenced as DQM.
BA[1:0]	Input	Bank address input(s): BA[1:0] define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A[12:0]	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0], A11, and A12 for x4; A[9:0] and A11 for x8; A[9:0] for x16; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
x16: DQ[15:0]	I/O	Data input/output: Data bus for x16 (pins 4, 7, 10, 13, 15, 42, 45, 48, and 51 are NC for x8; and pins 2, 4, 7, 8, 10, 13, 15, 42, 45, 47, 48, 51, and 53 are NC for x4).
x8: DQ[7:0]	I/O	Data input/output: Data bus for x8 (pins 2, 8, 47, 53 are NC for x4).
x4: DQ[3:0]	I/O	Data input/output: Data bus for x4.
V_{DDQ}	Supply	DQ power: DQ power to the die for improved noise immunity.
V_{SSQ}	Supply	DQ ground: DQ ground to the die for improved noise immunity.
V_{DD}	Supply	Power supply: +3.3V ±0.3V.
V_{SS}	Supply	Ground.
NC	–	These should be left unconnected.

Package Dimensions

Figure 5: 54-Pin Plastic TSOP (400 mil) – Package Codes TG/P



Notes:
1. All dimensions are in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. 2X means the notch is present in two locations (both ends of the device).
4. Package may or may not be assembled with a location notch.

Temperature and Thermal Impedance

It is imperative that the SDRAM device's temperature specifications, shown in Table 6 (page 14), be maintained to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 6 (page 14) for the applicable die revision and packages being made available. These thermal impedance values vary according to the density, package, and particular design used for each device.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed in Table 6 (page 14). To ensure the compatibility of current and future designs, contact Micron Applications Engineering to confirm thermal impedance values.

The SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Temperature Limits

Parameter		Symbol	Min	Max	Unit	Notes
Operating case temperature	Commercial	T_C	0	80	°C	1, 2, 3, 4
	Industrial		–40	90		
Junction temperature	Commercial	T_J	0	85	°C	3
	Industrial		–40	95		
Ambient temperature	Commercial	T_A	0	70	°C	3, 5
	Industrial		–40	85		
Peak reflow temperature		T_{PEAK}	–	260	°C	

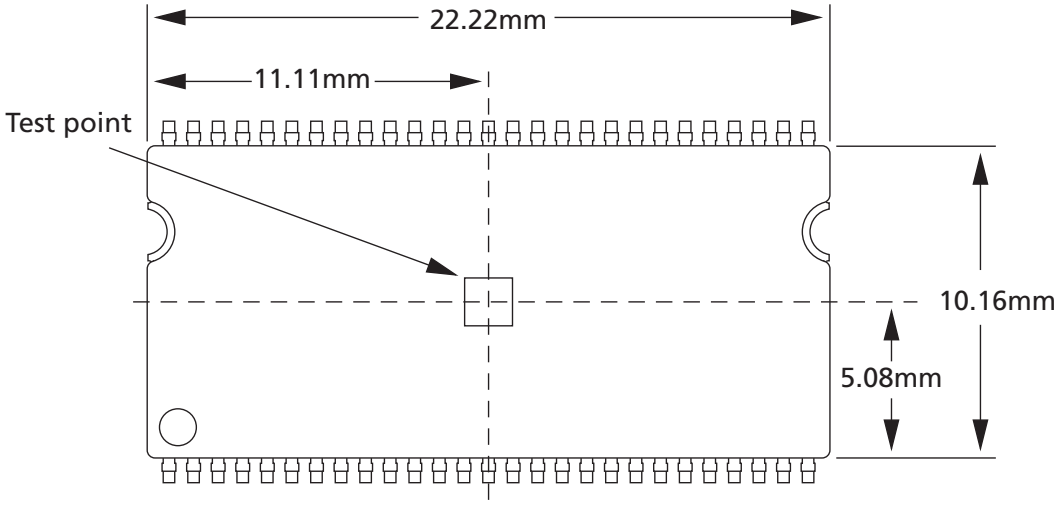
Notes:
1. MAX operating case temperature, TC, is measured in the center of the package on the top side of the device, as shown in Figure 6 (page 14).
2. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
3. All temperature specifications must be satisfied.
4. The case temperature should be measured by gluing a thermocouple to the top-center of the component. This should be done with a 1mm bead of conductive epoxy, as defined by the JEDEC EIA/JESD51 standards. Take care to ensure that the thermocouple bead is touching the case.
5. Operating ambient temperature surrounding the package.

Table 6: Thermal Impedance Simulated Values

Die Revision	Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)
D	54-pin TSOP	2-layer	62.6	48.4	44.2	19.2	6.7
		4-layer	39.2	32.3	30.6	19.3	

Notes:
1. For designs expected to last beyond the die revision listed, contact Micron Applications Engineering to confirm thermal impedance values.
2. Thermal resistance data is sampled from multiple lots, and the values should be viewed as typical.
3. These are estimates; actual results may vary.

Figure 6: Example: Temperature Test Point Location, 54-Pin TSOP (Top View)



Note:
1. Package may or may not be assembled with a location notch.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Voltage/Temperature	Symbol	Min	Max	Unit	Notes
Voltage on V_{DD}/V_{DDQ} supply relative to V_{SS}	V_{DD}/V_{DDQ}	–1	+4.6	V	1
Voltage on inputs, NC, or I/O balls relative to V_{SS}	V_{IN}	–1	+4.6		
Storage temperature (plastic)	T_{STG}	–55	+155	°C	
Power dissipation	–	–	1	W	

Note: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Table 8: DC Electrical Characteristics and Operating Conditions

Notes 1–3 apply to all parameters and conditions; V_{DD}/V_{DDQ} = +3.3V ±0.3V

Parameter/Condition		Symbol	Min	Max	Unit	Notes
Supply voltage		V_{DD}, V_{DDQ}	3	3.6	V	
Input high voltage: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	4
Input low voltage: Logic 0; All inputs		V_{IL}	–0.3	+0.8	V	4
Output high voltage: I_{OUT} = –4mA		V_{OH}	2.4	–	V	
Output low voltage: I_{OUT} = 4mA		V_{OL}	–	0.4	V	
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)		I_L	–5	5	µA	
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}		I_{OZ}	–5	5	µA	
Operating temperature:	Commercial	T_A	0	+70	˚C	
	Industrial	T_A	–40	+85	˚C	

Notes:
1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured; (0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), and –40°C ≤ TA ≤ +105°C (automotive)).
3. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. V_{IH} overshoot: $V_{IH,max} = V_{DDQ} + 2V$ for a pulse width ≤ 3ns, and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: $V_{IL,min} = –2V$ for a pulse width ≤3ns.

Table 9: Capacitance

Note 1 applies to all parameters and conditions

Package	Parameter	Symbol	Min	Max	Unit	Notes
TSOP "TG" package	Input capacitance: CLK	C_{L1}	2.5	3.5	pF	2
	Input capacitance: All other input-only balls	C_{L2}	2.5	3.8	pF	3
	Input/output capacitance: DQ	C_{L0}	4	6	pF	4

Notes:
1. This parameter is sampled. V_{DD}, V_{DDQ} = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
2. PC100 specifies a maximum of 4pF.
3. PC100 specifies a maximum of 5pF.
4. PC100 specifies a maximum of 6.5pF.
5. PC133 specifies a minimum of 2.5pF.
6. PC133 specifies a minimum of 2.5pF.
7. PC133 specifies a minimum of 3.0pF.

Electrical Specifications – I_{DD} Parameters

Table 10: I_{DD} Specifications and Conditions (-7E, -75)

Notes 1–5 apply to all parameters and conditions; V_{DD}/V_{DDQ} = +3.3V ±0.3V

Parameter/Condition		Symbol	Max		Unit	Notes
			-7E	-75		
Operating current: Active mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}	120	110	mA	6, 9, 10, 13
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2}	3.5	3.5	mA	13
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3}	45	45	mA	6, 8, 10, 13
Operating current: Burst mode; Page burst; READ or WRITE; All banks active		I_{DD4}	125	115	mA	6, 9, 10, 13
Auto refresh current: CKE = HIGH; CS# = HIGH	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}	255	255	mA	6, 8, 9, 10, 13, 14
	^{t}RFC = 7.813µs	I_{DD6}	6	6	mA	
Self refresh current: CKE ≤ 0.2V	Standard	I_{DD7}	6	6	mA	
	Low power (L)	I_{DD7}	3	3	mA	7

Notes:
1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured; (0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), and –40°C ≤ TA ≤ +105°C (automotive)).
3. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC operating and I_{DD} test conditions have V_{IL} = 0V and V_{IH} = 3.0V using a measurement reference level of 1.5V. If the input transition time is longer than 1ns, then the timing is measured from $V_{IL,\ max}$ and $V_{IH,min}$ and no longer from the 1.5V midpoint. CLK should always be 1.5V referenced to crossover. Refer to Micron technical note TN-48-09.
5. I_{DD} specifications are tested after the device is properly initialized.
6. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
7. Enables on-chip refresh and address counters.
8. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
9. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
10. Address transitions average one transition every two clocks.
11. PC100 specifies a maximum of 4pF.
12. PC100 specifies a maximum of 5pF.
13. For -75, CL = 3 and tCK = 7.5ns; for -7E, CL = 2 and tCK = 7.5ns.
14. CKE is HIGH during REFRESH command period ^{t}RFC (MIN) else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.

Electrical Specifications – AC Operating Conditions

Table 11: Electrical Characteristics and Recommended AC Operating Conditions (-7E, -75)

Notes 1, 2, 4, 5, 7, and 20 apply to all parameters and conditions

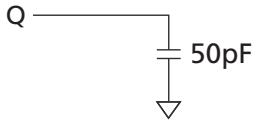
Parameter		Symbol	-7E		-75		Unit	Notes
			Min	Max	Min	Max		
Access time from CLK (positive edge)	CL = 3	tAC(3)	–	5.4	–	5.4	ns	18
	CL = 2	tAC(2)	–	5.4	–	6		
Address hold time		tAH	0.8	–	0.8	–	ns	
Address setup time		tAS	1.5	–	1.5	–	ns	
CLK high-level width		tCH	2.5	–	2.5	–	ns	
CLK low-level width		tCL	2.5	–	2.5	–	ns	
Clock cycle time	CL = 3	tCK(3)	7	–	7.5	–	ns	14
	CL = 2	tCK(2)	7.5	–	10	–		
CKE hold time		tCKH	0.8	–	0.8	–	ns	
CKE setup time		tCKS	1.5	–	1.5	–	ns	21
CS#, RAS#, CAS#, WE#, DQM hold time		tCMH	0.8	–	0.8	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		tCMS	1.5	–	1.5	–	ns	
Data-in hold time		tDH	0.8	–	0.8	–	ns	
Data-in setup time		tDS	1.5	–	1.5	–	ns	
Data-out High-Z time	CL = 3	tHZ(3)	–	5.4	–	5.4	ns	6
	CL = 2	tHZ(2)	–	5.4	–	6	ns	
Data-out Low-Z time		tLZ	1	–	1	–	ns	
Data-out hold time (load)		tOH	2.7	–	2.7	–	ns	
Data-out hold time (no load)		tOH*n*	1.8	–	1.8	–	ns	19
ACTIVE-to-PRECHARGE command		tRAS	37	120,000	44	120,000	ns	
ACTIVE-to-ACTIVE command period		tRC	60	–	66	–	ns	23
ACTIVE-to-READ or WRITE delay		tRCD	15	–	20	–	ns	
Refresh period (8192 rows)		tREF	–	64	–	64	ms	
AUTO REFRESH period		tRFC	66	–	66	–	ns	
PRECHARGE command period		tRP	15	–	20	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		tRRD	14	–	15	–	tCK	
Transition time		tT	0.3	1.2	0.3	1.2	ns	3
WRITE recovery time		tWR	1 CLK + 7ns	–	1 CLK + 7.5ns	–	ns	15
			14	–	15	–		16
Exit SELF REFRESH-to-ACTIVE command		tXSR	67	–	75	–	ns	12

Table 12: AC Functional Characteristics (-7E, -75)

Notes 1–5 and note 7 apply to all parameters and conditions

Parameter		Symbol	-7E	-75	Unit	Notes
Last data-in to burst STOP command		tBDL	1	1	tCK	11
READ/WRITE command to READ/WRITE command		tCCD	1	1	tCK	11
Last data-in to new READ/WRITE command		tCDL	1	1	tCK	11
CKE to clock disable or power-down entry mode		tCKED	1	1	tCK	8
Data-in to ACTIVE command		tDAL	4	5	tCK	9, 13
Data-in to PRECHARGE command		tDPL	2	2	tCK	10, 13
DQM to input data delay		tDQD	0	0	tCK	11
DQM to data mask during WRITEs		tDQM	0	0	tCK	11
DQM to data High-Z during READs		tDQZ	2	2	tCK	11
WRITE command to input data delay		tDWD	0	0	tCK	11
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	tCK	17
CKE to clock enable or power-down exit setup mode		tPED	1	1	tCK	8
Last data-in to PRECHARGE command		tRDL	2	2	tCK	10, 13
Data-out High-Z from PRECHARGE command	CL = 3	tROH(3)	3	3	tCK	11
	CL = 2	tROH(2)	2	2	tCK	11

Notes:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C commercial temperature, -40°C ≤ T_A ≤ +85°C industrial temperature, and -40°C ≤ T_A ≤ +105°C automotive temperature) is ensured.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
3. AC characteristics assume tT = 1ns.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. Outputs measured at 1.5V with equivalent load:



6. tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet tOH before going High-Z.
7. AC operating and I_{DD} test conditions have V_{IL} = 0V and V_{IH} = 3.0V using a measurement reference level of 1.5V. If the input transition time is longer than 1ns, then the timing is measured from $V_{IL,max}$ and $V_{IH,min}$ and no longer from the 1.5V midpoint. CLK should always be 1.5V referenced to crossover. Refer to Micron technical note TN-48-09.
8. Timing is specified by tCKS. Clock(s) specified as a reference only at minimum cycle rate.
9. Timing is specified by tWR plus tRP. Clock(s) specified as a reference only at minimum cycle rate.
10. Timing is specified by tWR.

11. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
12. CLK must be toggled a minimum of two times during this period.
13. Based on ^{t}CK = 7.5ns for -75 and -7E, 6ns for -6A.
14. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
15. Auto precharge mode only. The precharge timing budget (^{t}RP) begins at 7ns for -7E and 7.5ns for -75 after the first clock delay and after the last WRITE is executed.
16. Precharge mode only.
17. JEDEC and PC100 specify three clocks.
18. ^{t}AC for -75/-7E at CL = 3 with no load is 4.6ns and is guaranteed by design.
19. Parameter guaranteed by design.
20. PC100 specifies a maximum of 6.5pF.
21. For operating frequencies ≤ 45 MHz, ^{t}CKS = 3.0ns.
22. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 6ns for -6A after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
23. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

Functional Description

In general, 512Mb SDRAM devices (32 Meg x 4 x 4 banks, 16 Meg x 8 x 4 banks, and 16 Meg x 16 x 4 banks) are quad-bank DRAM that operate at 3.3V and include a synchronous interface. All signals are registered on the positive edge of the clock signal, CLK. Each of the x8's 134,217,728-bit banks is organized as 8192 rows by 4096 columns by 4 bits. Each of the x8's 134,217,728-bit banks is organized as 8192 rows by 2048 columns by 8 bits. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A[12:0] select the row). The address bits (x4: A[9:0], A11, ***A12***; x8: A[9:0], ***A11***; x16: ***A[9:0]***) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Commands

The following table provides a quick reference of available commands, followed by a written description of each command. Additional Truth Tables (Table 14 (page 28), Table 15 (page 30), and Table 16 (page 32)) provide current state/next state information.

Table 13: Truth Table – Commands and DQM Operation

Note 1 applies to all parameters and conditions

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	L	H	H	X	Bank/row	X	2
READ (select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/col	Valid	3
BURST TERMINATE	L	H	H	L	X	X	Active	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	8
Write enable/output enable	X	X	X	X	L	X	Active	9
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	9

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A[0:*n*] provide row address (where A*n* is the most significant address bit), BA0 and BA1 determine which bank is made active.
3. A[0:*i*] provide column address (where *i* = the most significant column address for a given device configuration). A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature. BA0 and BA1 determine which bank is being read from or written to.
4. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQ column reads a "Don't Care" state to illustrate that the BURST TERMINATE command can occur when there is no data present.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: all banks precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. A[11:0] define the op-code written to the mode register.
9. Activates or deactivates the DQ during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the device, regardless of whether the CLK signal is enabled. The device is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to the selected device (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

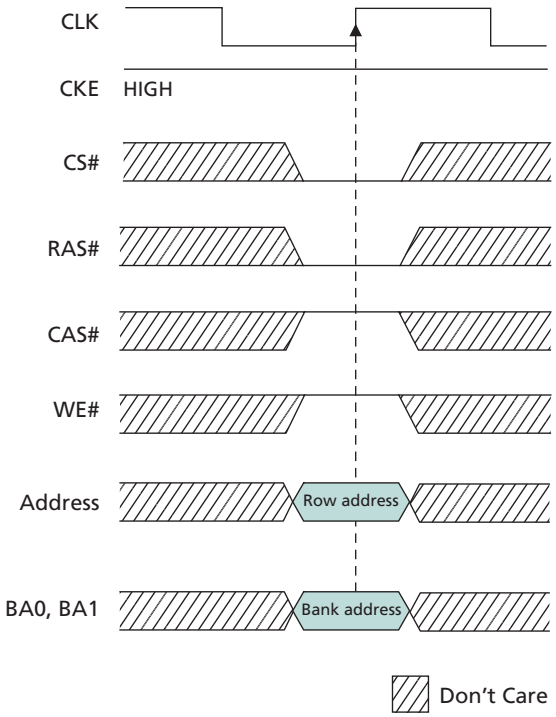
LOAD MODE REGISTER (LMR)

The mode registers are loaded via inputs A[*n:0]* (where A*n* is the most significant address term), BA0, and BA1 (see Mode Register (page 35)). The LOAD MODE REGISTER command can only be issued when all banks are idle and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to activate a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

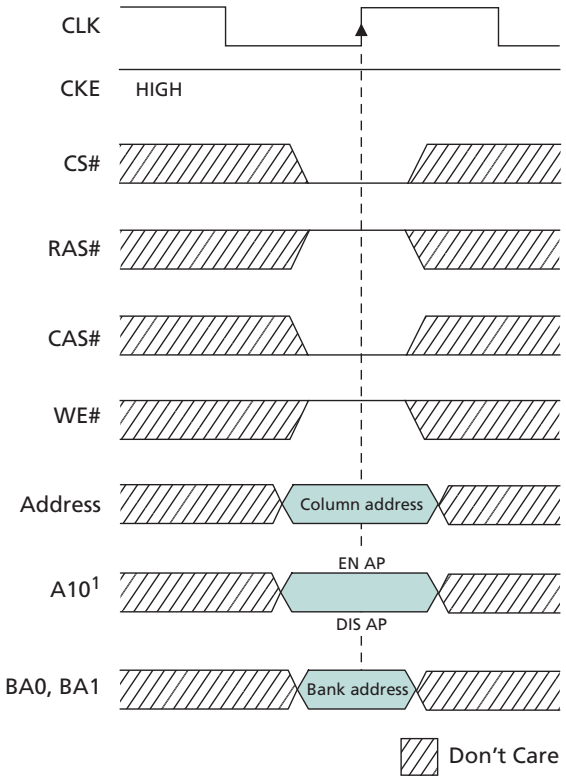
Figure 7: ACTIVE Command



READ

The READ command is used to initiate a burst read access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the READ burst; if auto precharge is not selected, the row remains open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

Figure 8: READ Command

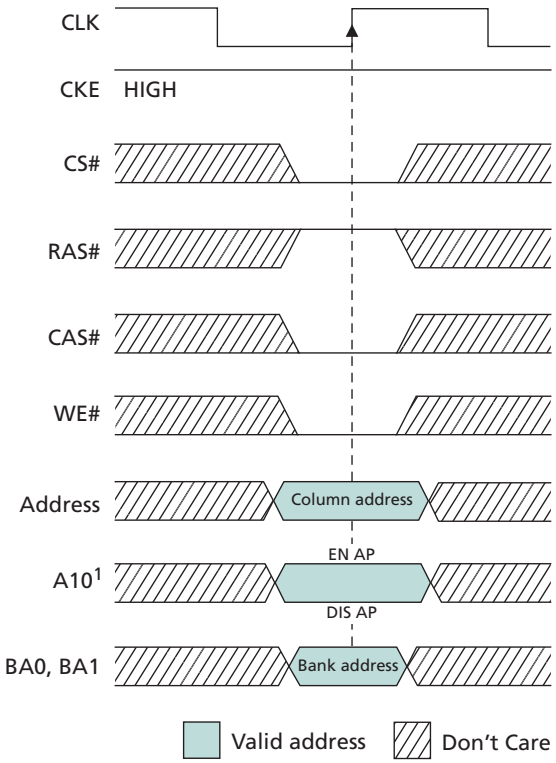


Note: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the write burst; if auto precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQ is written to the memory array, subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data is written to memory; if the DQM signal is registered HIGH, the corresponding data inputs are ignored and a WRITE is not executed to that byte/column location.

Figure 9: WRITE Command



Note: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge.