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SDR SDRAM

MT48LC32M4A2 – 8 Meg x 4 x 4 Banks
MT48LC16M8A2 – 4 Meg x 8 x 4 Banks
MT48LC8M16A2 – 2 Meg x 16 x 4 Banks

Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths (BL): 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh modes: Standard and low power (not available on AT devices)
- Auto Refresh
  - 64ms, 4096-cycle refresh (commercial and industrial)
  - 16ms, 4096-cycle refresh (automotive)
- LVTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply

Options	Marking
• Configurations	
– 32 Meg x 4 (8 Meg x 4 x 4 banks)[1]	32M4
– 16 Meg x 8 (4 Meg x 8 x 4 banks)	16M8
– 8 Meg x 16 (2 Meg x 16 x 4 banks)	8M16
• Write recovery (^{t}WR)	
– ^{t}WR = 2 CLK	A2

Options	Marking
• Plastic package – OCPL[2]	
– 54-pin TSOP II (400 mil)	TG
– 54-pin TSOP II (400 mil) Pb-free	P
– 60-ball TFBGA (8mm x 16mm)	FB[1]
– 60-ball TFBGA (8mm x 16mm) Pb-free	BB[1]
– 54-ball VFBGA (x16 only) (8mm x 8mm)	F4
– 54-ball VFBGA (x16 only) (8mm x 8mm) Pb-free	B4
• Timing – cycle time	
– 7.5ns @ CL = 3 (PC133)	-75[3]
– 7.5ns @ CL = 2 (PC133)	-7E
– 6.0ns @ CL = 3 (x16 only)	-6A
• Self refresh	
– Standard	None
– Low power	L[3]
• Revision	:G/:L
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
– Automotive (–40°C to +105°C)	AT[1]

Notes:
1. Contact Micron for availability.
2. Off-center parting line.
3. Only available on Revision G.

Table 1: Key Timing Parameters

CL = CAS (READ) latency

Speed Grade	Clock Frequency (MHz)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-6A	167	3-3-3	18	18	18
-75	133	3-3-3	20	20	20
-7E	133	2-2-2	15	15	15

Table 2: Address Table

Parameter	32 Meg x 4	16 Meg x 8	8 Meg x 16
Configuration	8 Meg x 4 x 4 banks	4 Meg x 8 x 4 banks	2 Meg x 16 x 4 banks
Refresh count	4K	4K	4K
Row addressing	4K A[11:0]	4K A[11:0]	4K A[11:0]
Bank addressing	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]
Column addressing	2K A[9:0], A11	1K A[9:0]	512 A[8:0]

Table 3: 128Mb SDR Part Numbering

Part Numbers	Architecture
MT48LC32M4A2TG	32 Meg x 4
MT48LC32M4A2P	32 Meg x 4
MT48LC16M8A2TG	16 Meg x 8
MT48LC16M8A2P	16 Meg x 8
MT48LC16M8A2FB	16 Meg x 8
MT48LC16M8A2BB	16 Meg x 8
MT48LC8M16A2TG	8 Meg x 16
MT48LC8M16A2P	8 Meg x 16
MT48LC8M16A2B4	8 Meg x 16
MT48LC8M16A2F4	16 Meg x 16

Note: 1. FBGA Device Decoder: www.micron.com/decoder

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General Description

The 128Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 33,554,432-bit banks is organized as 4096 rows by 2048 columns by 4 bits. Each of the x8's 33,554,432-bit banks is organized as 4096 rows by 1024 columns by 8 bits. Each of the x16's 33,554,432-bit banks is organized as 4096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank; A[11:0] select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 128Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 128Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

The devices offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Automotive Temperature

The automotive temperature (AT) option adheres to the following specifications:

- 16ms refresh rate
- Self refresh not supported
- Ambient and case temperature cannot be less than –40°C or greater than +105°C

Functional Block Diagrams

Figure 1: 32 Meg x 4 Functional Block Diagram

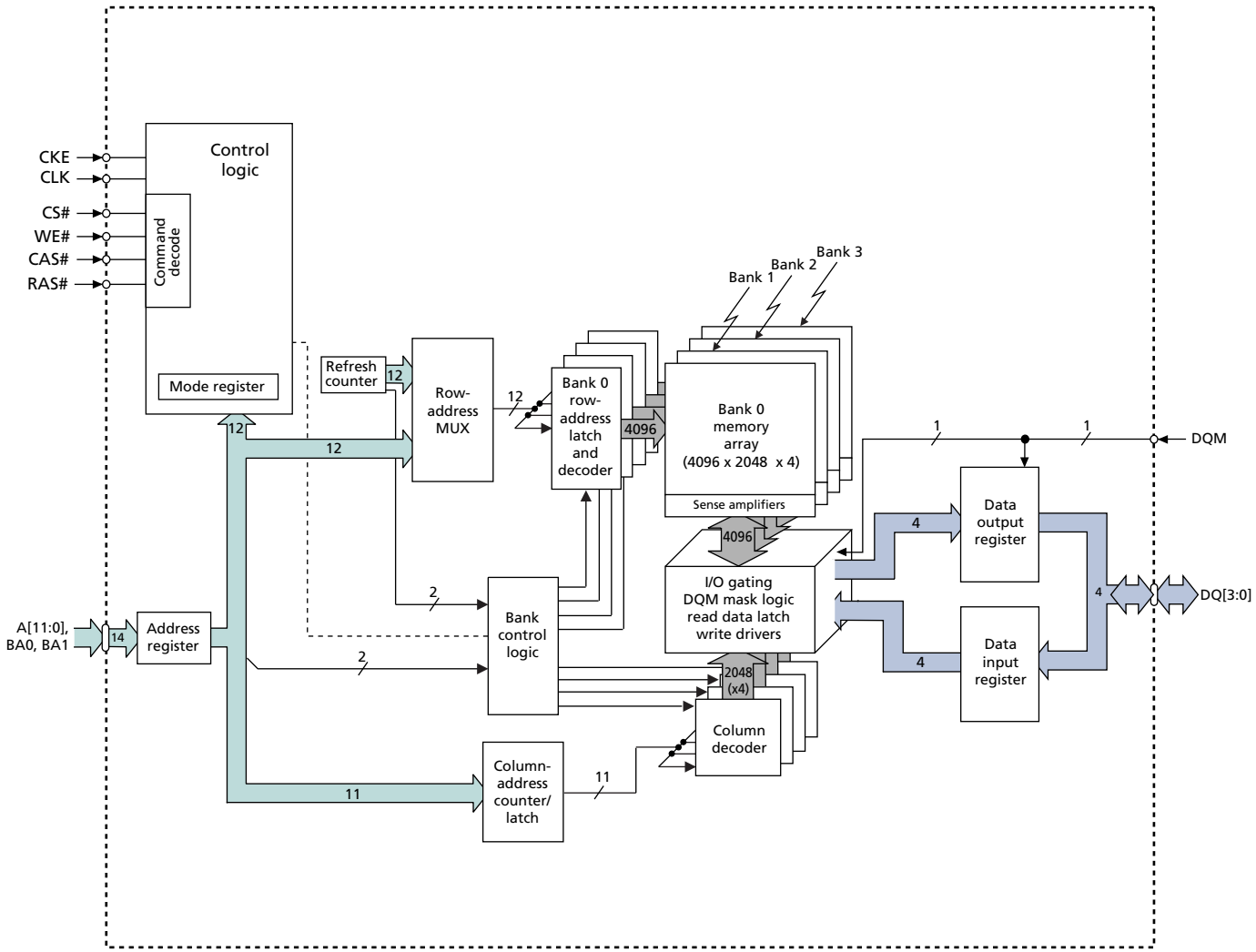


Figure 2: 16 Meg x 8 Functional Block Diagram

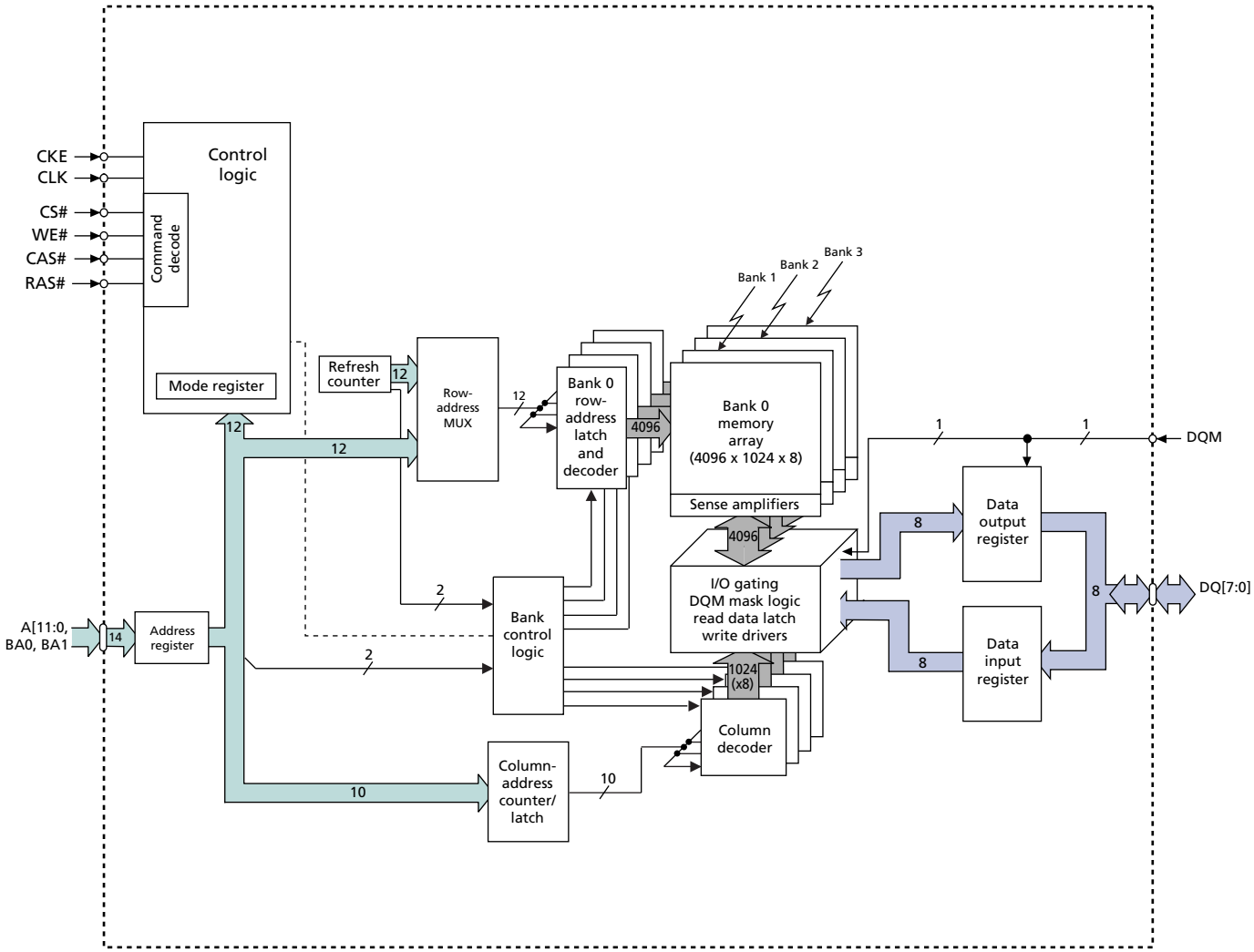
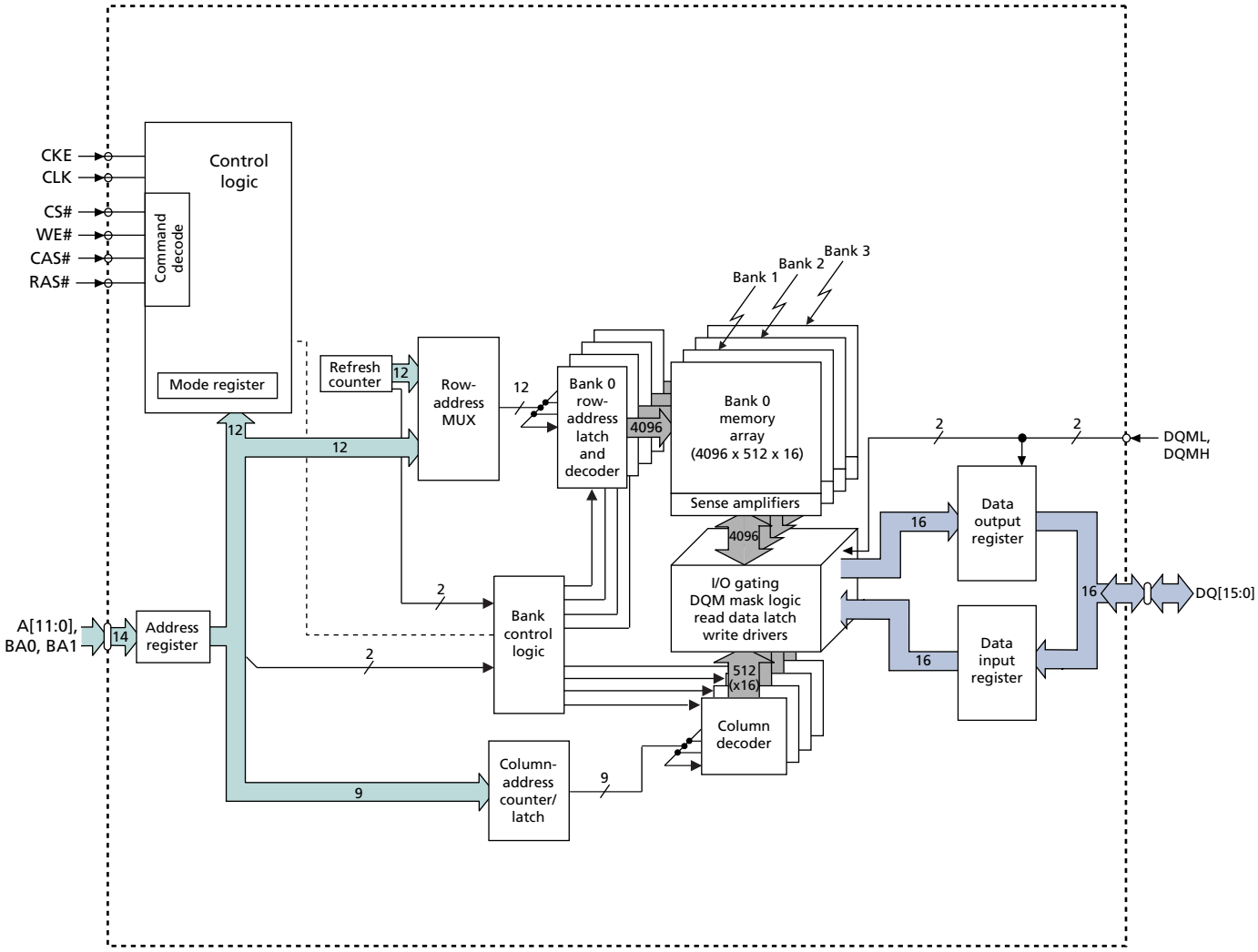
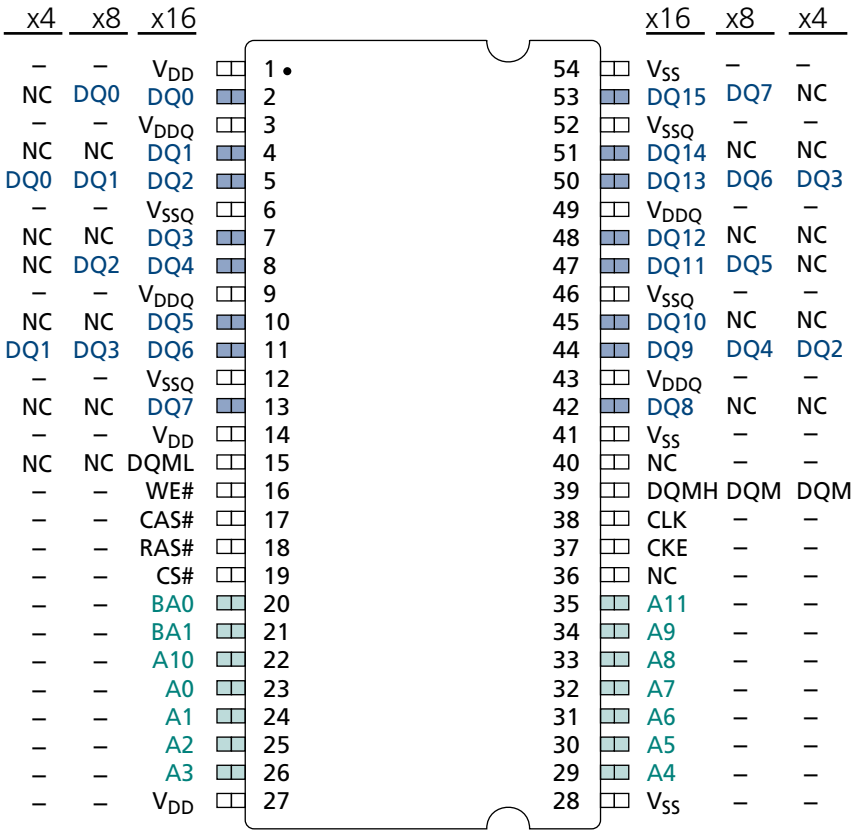


Figure 3: 8 Meg x 16 Functional Block Diagram



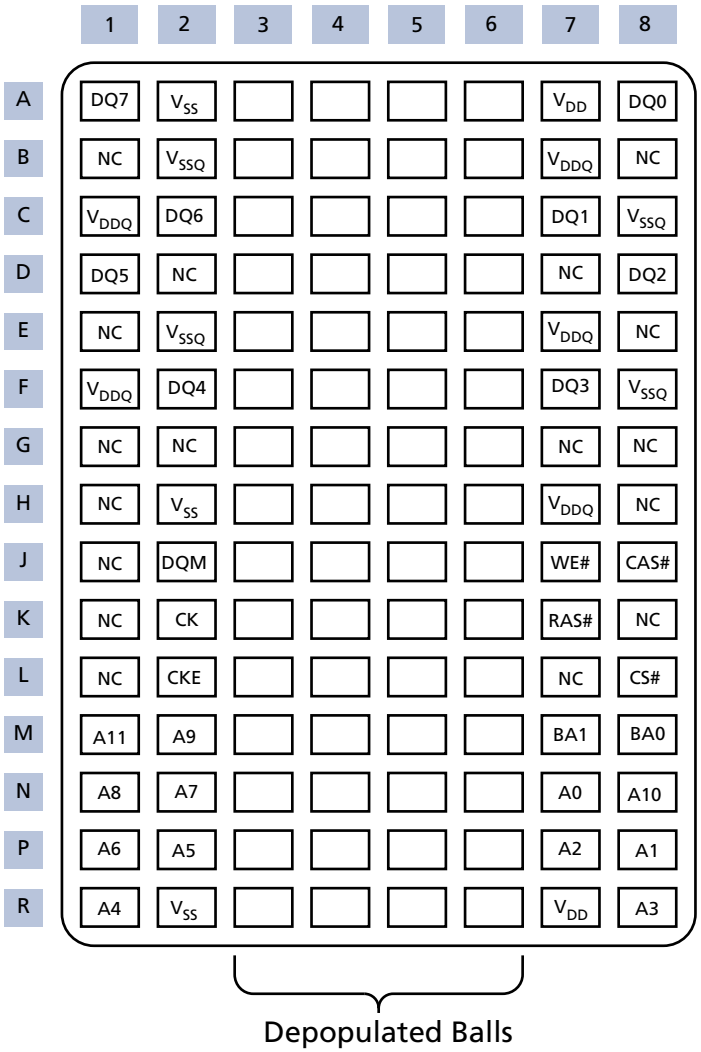
Pin and Ball Assignments and Descriptions

Figure 4: 54-Pin TSOP (Top View)



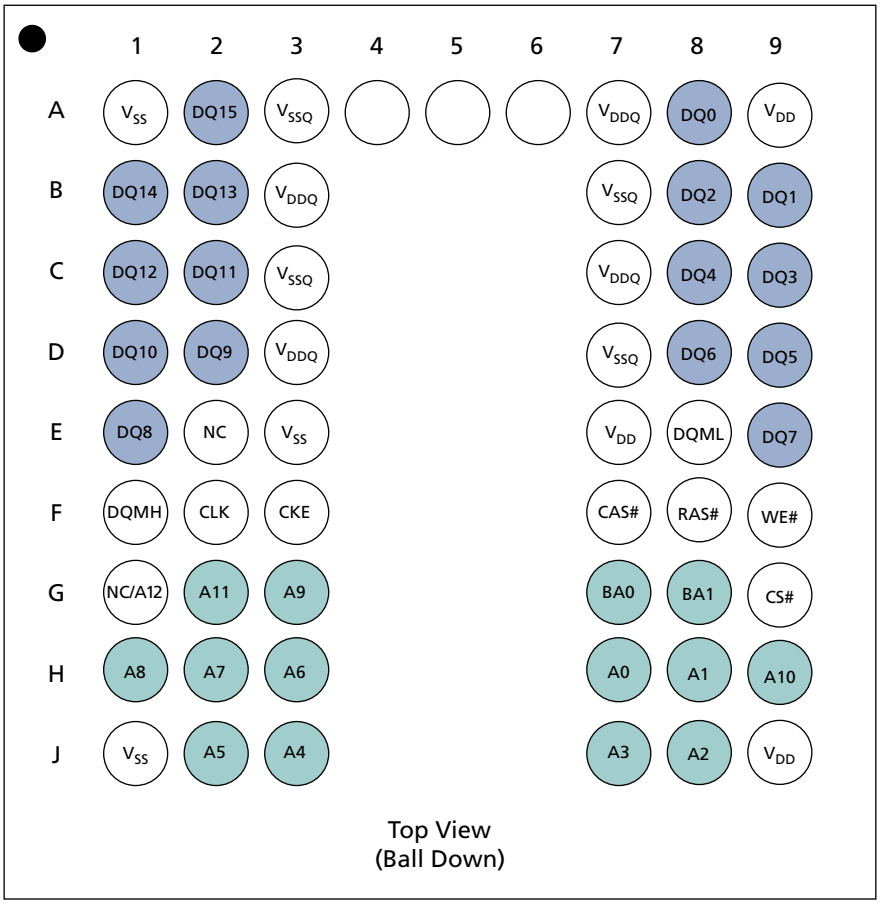
Notes: 1. A dash (–) indicates x8 and x4 pin function is same as x16 pin function.
2. Package may or may not be assembled with a location notch.

Figure 5: 60-Ball FBGA (TopView)



Note: 1. The balls at A4, A5, and A6 are not in the physical package. They are included in the drawing to illustrate that rows 4, 5, and 6 exist but contain no balls.

Figure 6: 54-Ball VFBGA (Top View)



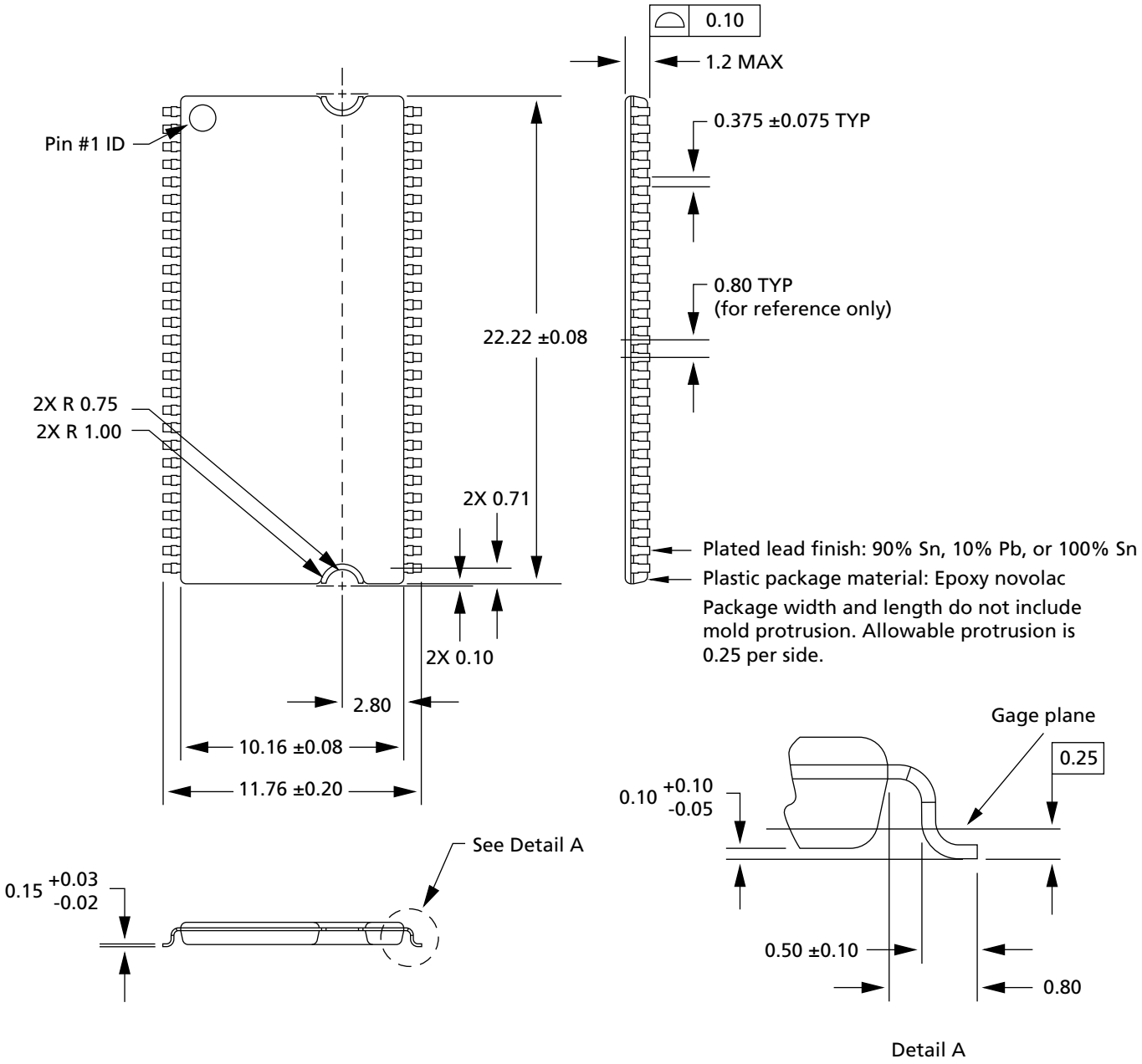
Note: 1. The balls at A4, A5, and A6 are not in the physical package. They are included in the drawing to illustrate that rows 4, 5, and 6 exist but contain no balls.

Table 4: Pin and Ball Descriptions

Symbol	Type	Description
CLK	Input	**Clock:** CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	**Clock enable:** CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while CS# is HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	**Command inputs:** CAS#, RAS#, and WE# (along with CS#) define the command being entered.
x4, x8: DQM x16: DQML, DQMH	Input	**Input/output mask:** DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are High-Z (two-clock latency) during a READ cycle. On the x4 and x8, DQML (pin 15) is NC; DQMH is DQM. On the x16, DQML corresponds to DQ[7:0] and DQMH corresponds to DQ[15:8]. DQML and DQMH are considered same-state when referenced as DQM.
BA[1:0]	Input	**Bank address input(s):** BA[1:0] define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A[11:0]	Input	**Address inputs:** A[11:0] are sampled during the ACTIVE command (row address A[11:0]) and READ or WRITE command (column address A[9:0] and A11 for x4; A[9:0] for x8; A[8:0] for x16; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10 HIGH) or bank selected by BA[1:0] (A10 LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
x16: DQ[15:0]	I/O	**Data input/output:** Data bus for x16 (pins 4, 7, 10, 13, 42, 45, 48, and 51 are NC for x8; and pins 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, and 53 are NC for x4).
x8: DQ[7:0]	I/O	**Data input/output:** Data bus for x8 (pins 2, 8, 47, 53 are NC for x4 TSOP; balls A8, D8, D1, and A1 are NC for x4 FBGA).
x4: DQ[3:0]	I/O	**Data input/output:** Data bus for x4.
V_{DDQ}	Supply	**DQ power:** Isolated DQ power to the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated DQ ground to the die for improved noise immunity.
V_{DD}	Supply	**Power supply:** 3.3V ±0.3V.
V_{SS}	Supply	Ground.
NC	–	**No connect:** These should be left unconnected. For x4 and x8 parts, G1 is a no connect; it is A12 for 256Mb and 512Mb devices.

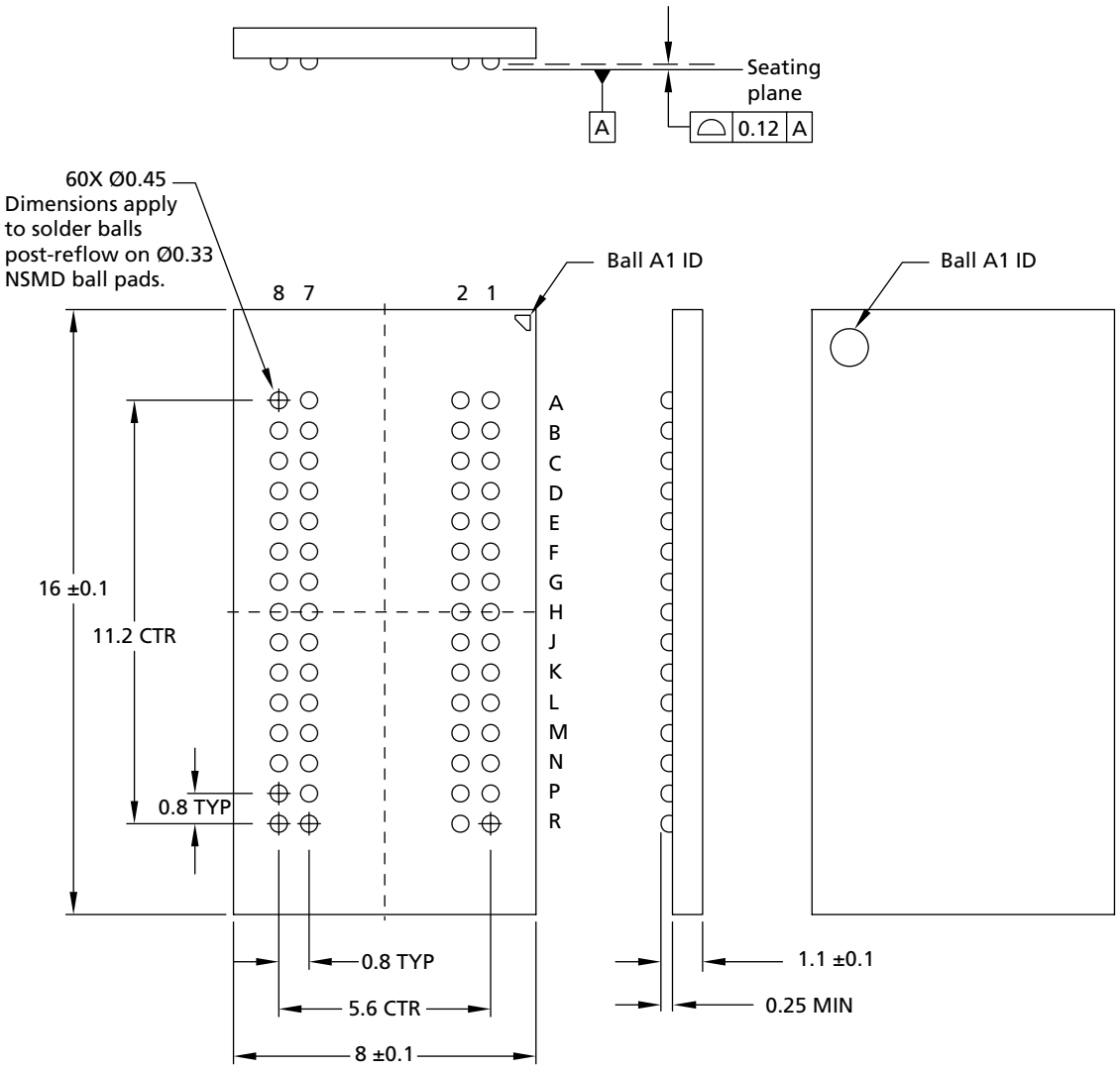
Package Dimensions

Figure 7: 54-Pin Plastic TSOP (400 mil)



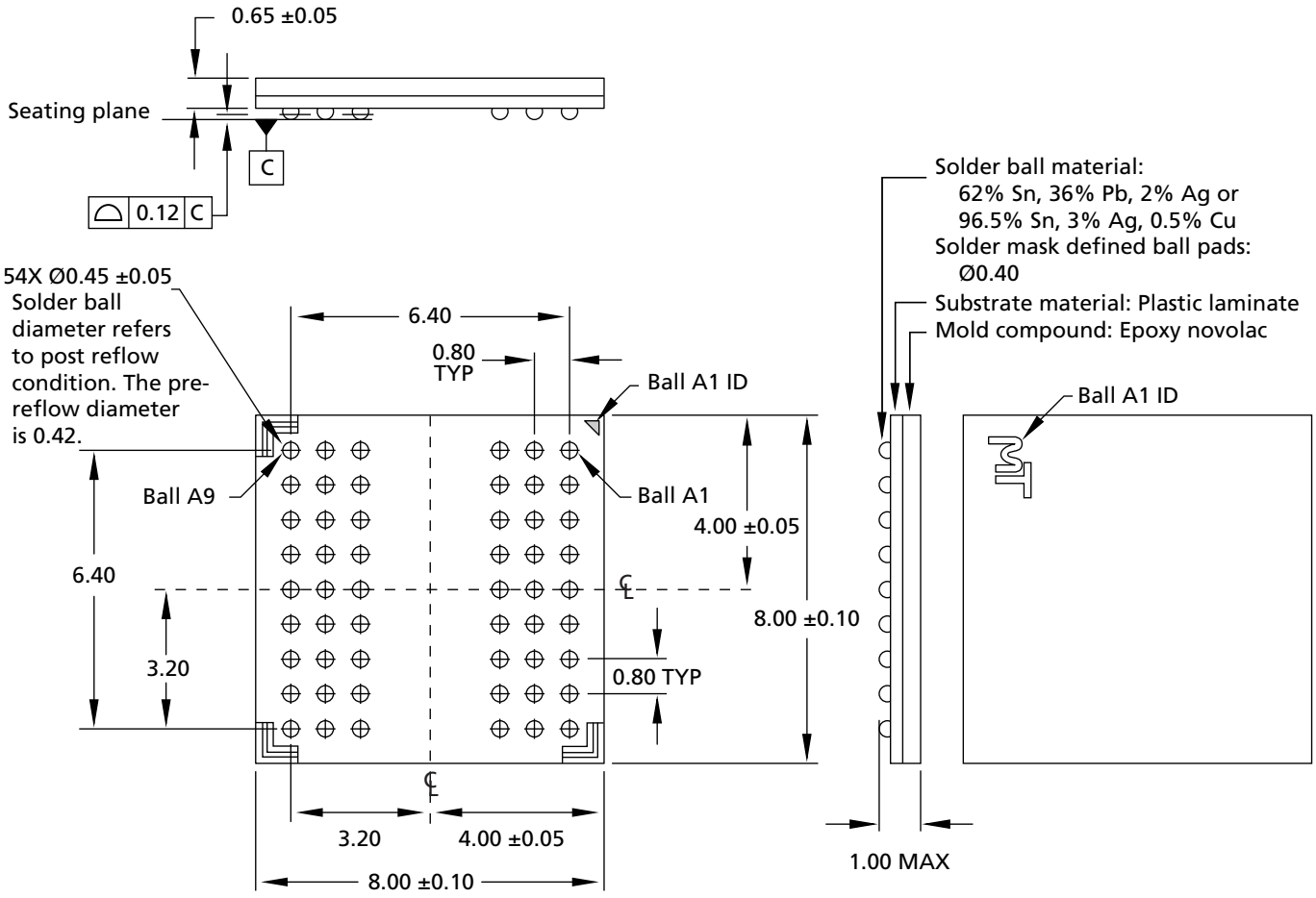
Notes:
1. All dimensions are in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. 2X means the notch is present in two locations (both ends of the device).
4. Package may or may not be assembled with a location notch.

Figure 8: 60-Ball TFBGA (x8 Device), 8mm x 16mm – Package Code FB/BB



Notes:
1. All dimensions are in millimeters.
2. Recommended pad size for PCB is 0.33mm ±0.025mm.
3. Topside part-marking decoder is available at www.micron.com/decoder.

Figure 9: 54-Ball VFBGA (x16 Device), 8mm x 8mm – Package Code F4/B4



Notes:
1. All dimensions are in millimeters.
2. Recommended pad size for PCB is 0.40mm SMD.
3. Topside part-marking decoder is available at www.micron.com/decoder.

Temperature and Thermal Impedance

It is imperative that the SDRAM device's temperature specifications, shown in Temperature Limits below, be maintained to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Thermal Impedance Simulated Values for the applicable die revision and packages being made available. These thermal impedance values vary according to the density, package, and particular design used for each device.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed in Thermal Impedance Simulated Values. To ensure the compatibility of current and future designs, contact Micron Applications Engineering to confirm thermal impedance values.

The SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Temperature Limits

Parameter		Symbol	Min	Max	Unit	Notes
Operating case temperature	Commercial	T_C	0	80	°C	1, 2, 3, 4
	Industrial		–40	90		
	Automotive		–40	105		
Junction temperature	Commercial	T_J	0	85	°C	3
	Industrial		–40	95		
	Automotive		–40	110		
Ambient temperature	Commercial	T_A	0	70	°C	3, 5
	Industrial		–40	85		
	Automotive		–40	105		
Peak reflow temperature		T_{PEAK}	–	260	°C	

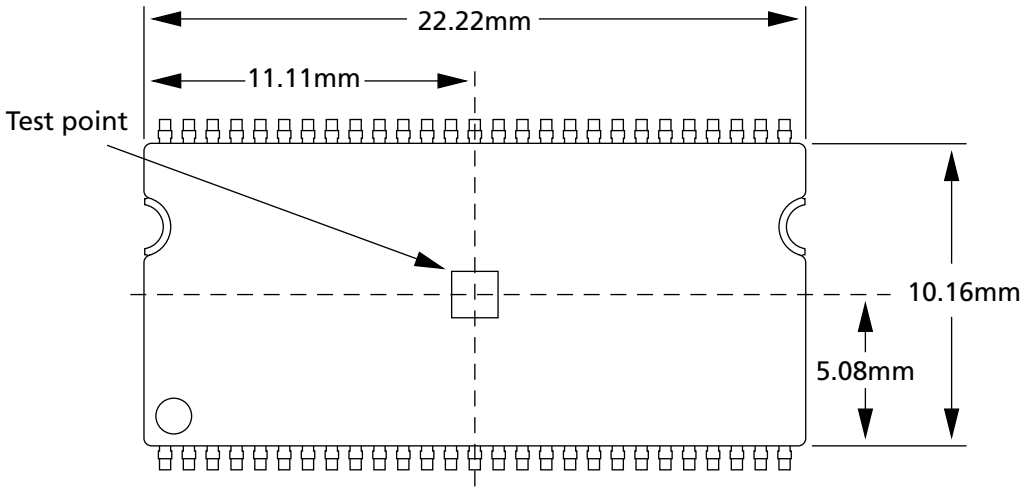
Notes:
1. MAX operating case temperature, T_C, is measured in the center of the package on the top side of the device, as shown in Figure 10 (page 20), Figure 11 (page 21), and Figure 12 (page 21).
2. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
3. All temperature specifications must be satisfied.
4. The case temperature should be measured by gluing a thermocouple to the top-center of the component. This should be done with a 1mm bead of conductive epoxy, as defined by the JEDEC EIA/JESD51 standards. Take care to ensure that the thermocouple bead is touching the case.
5. Operating ambient temperature surrounding the package.

Table 6: Thermal Impedance Simulated Values

Die Revision	Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)
G	54-pin TSOP (TG, P)	Low Conductivity	86.2	67.8	62	46.9	11.3
		High Conductivity	58.9	50.7	47.6	41.5	
	54-ball VFBGA (B4, F4)	Low Conductivity	72.1	57.3	50.6	36	4.1
		High Conductivity	54.5	46.6	42.8	35.5	
	60-ball FBGA (BB, FB)	Low Conductivity	70.9	56.8	50.3	36.3	1.9
		High Conductivity	54.6	47.3	43.5	36.3	
L	54-pin TSOP (TG, P)	Low Conductivity	122.3	105.6	98.1	89.5	20.7
		High Conductivity	101.9	93.5	88.8	87.6	
	54-ball VFBGA (B4, F4)	Low Conductivity	96.9	81.9	81.9	69.5	11.5
		High Conductivity	74.0	66.3	62.7	60.7	
	60-ball FBGA (BB, FB)	Low Conductivity	68.8	55.9	51.1	42.1	10.9
		High Conductivity	47.9	42.0	39.9	34.9	

Notes:
1. For designs expected to last beyond the die revision listed, contact Micron Applications Engineering to confirm thermal impedance values.
2. Thermal resistance data is sampled from multiple lots, and the values should be viewed as typical.
3. These are estimates; actual results may vary.

Figure 10: Example: Temperature Test Point Location, 54-Pin TSOP (Top View)



Note: 1. Package may or may not be assembled with a location notch.

Figure 11: Example: Temperature Test Point Location, 54-Ball VFBGA (Top View)

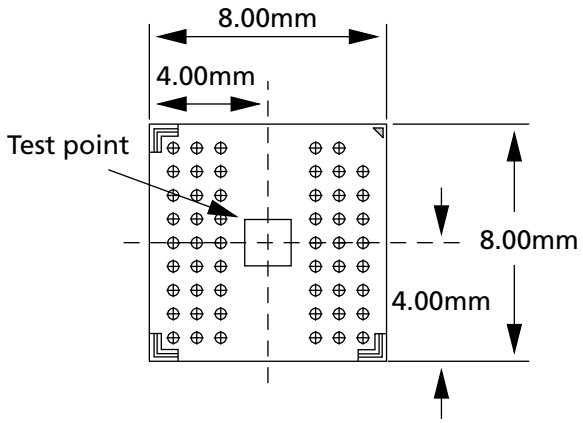
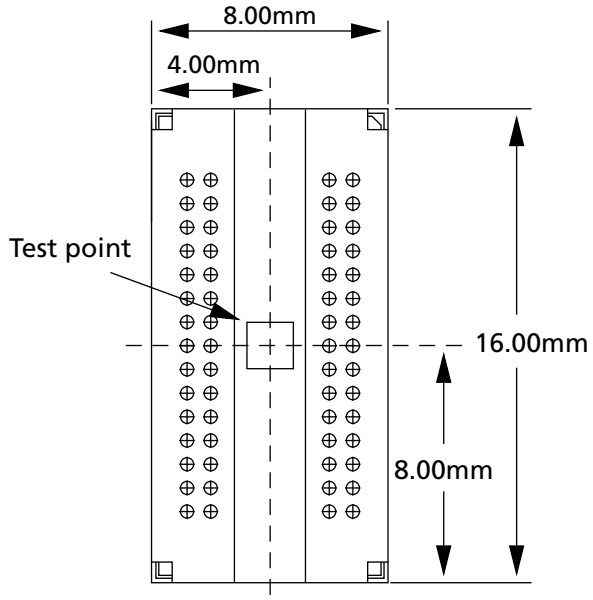


Figure 12: Example: Temperature Test Point Location, 60-Ball FBGA (Top View)



Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Voltage/Temperature		Symbol	Min	Max	Unit
Voltage on V_{DD}/V_{DDQ} supply relative to V_{SS}		V_{DD}/V_{DDQ}	–1	4.6	V
Voltage on inputs, NC, or I/O balls relative to V_{SS}		V_{IN}	–1	4.6	
Operating temperature:	Commercial	T_A	0	70	°C
	Industrial	T_A	–40	85	
Storage temperature (plastic)		T_{STG}	–55	150	°C
Power dissipation		–	1		W

Table 8: DC Electrical Characteristics and Operating Conditions

Notes 1–3 apply to all parameters and conditions; V_{DD}/V_{DDQ} = +3.3V ±0.3V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{DD}, V_{DDQ}	3	3.6	V	
Input high voltage: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	4
Input low voltage: Logic 0; All inputs	V_{IL}	–0.3	0.8	V	4
Output high voltage: I_{OUT} = –4mA	V_{OH}	2.4	–	V	
Output low voltage: I_{OUT} = 4mA	V_{OL}	–	0.4	V	
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)	I_L	–5	5	µA	
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	I_{OZ}	–5	5	µA	

Notes:
1. All voltages referenced to V_{SS}.
2. Minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range is ensured:
   0°C ≤ T_A ≤ +70°C (commercial)
   –40°C ≤ T_A ≤ +85°C (industrial)
   –40°C ≤ T_A ≤ +105°C (automotive)
3. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. V_{IH} overshoot: $V_{IH,max}$ = V_{DDQ} + 2V for a pulse width ≤3ns, and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: $V_{IL,min}$ = –2V for a pulse width ≤3ns.

Table 9: Capacitance

Note 1 applies to all parameters and conditions

Package	Parameter	Symbol	Min	Max	Unit	Notes
TSOP package	Input capacitance: CLK	C_{L1}	2.5	3.5	pF	2
	Input capacitance: All other input-only balls	C_{L2}	2.5	3.8	pF	3
	Input/output capacitance: DQ	C_{L0}	4.0	6.0	pF	4
FBGA package	Input capacitance: CLK	C_{L1}	1.5	3.5	pF	5
	Input capacitance: All other input-only balls	C_{L2}	1.5	3.8	pF	6
	Input/output capacitance: DQ	C_{L0}	3	6	pF	4

Notes:
1. This parameter is sampled. V_{DD}, V_{DDQ} = 3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
2. PC100 specifies a maximum of 4pF.
3. PC100 specifies a maximum of 5pF.
4. PC100 specifies a maximum of 6.5pF.
5. PC133 specifies a minimum of 2.5pF.
6. PC133 specifies a minimum of 2.5pF.

Electrical Specifications – I_{DD} Parameters

Table 10: I_{DD} Specifications and Conditions – Revision G

Notes 1–5 apply to all parameters and conditions; V_{DD}/V_{DDQ} = 3.3V ±0.3V

Parameter/Condition		Symbol	Max			Unit	Notes
			-6A	-7E	-75		
Operating current: Active mode; Burst = 2; READ or WRITE; tRC = tRC (MIN)		I_{DD1}	170	160	150	mA	6, 7, 8, 9
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2}	2	2	2	mA	9
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress		I_{DD3}	50	50	50	mA	6, 8, 9, 10
Operating current: Burst mode; Page burst; READ or WRITE; All banks active		I_{DD4}	165	165	150	mA	6, 7, 8, 9
Auto refresh current: CKE = HIGH; CS# = HIGH	tRFC = tRFC (MIN)	I_{DD5}	330	330	310	mA	6, 7, 8, 9, 10
	tRFC = 15.625µs	I_{DD6}	3	3	3	mA	11
	tRFC = 3.906µs (AT)	I_{DD6}	6	6	6	mA	
Self refresh current: CKE ≤ 0.2V	Standard	I_{DD7}	2	2	2	mA	12
	Low power (L)	I_{DD7}	–	1	1	mA	

Table 11: I_{DD} Specifications and Conditions – Revision L

Notes 1–5 apply to all parameters and conditions; V_{DD}/V_{DDQ} = 3.3V ±0.3V

Parameter/Condition		Symbol	Max			Unit	Notes
			-6A	-7E	-75		
Operating current: Active mode; Burst = 2; READ or WRITE; tRC = tRC (MIN)		I_{DD1}	100	100	100	mA	6, 7, 8, 9
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2}	2.5	2.5	2.5	mA	9
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress		I_{DD3}	35	35	35	mA	6, 8, 9, 10
Operating current: Burst mode; Page burst; READ or WRITE; All banks active		I_{DD4}	100	100	100	mA	6, 7, 8, 9
Auto refresh current: CKE = HIGH; CS# = HIGH	tRFC = tRFC (MIN)	I_{DD5}	150	150	150	mA	6, 7, 8, 9, 10
	tRFC = 15.625µs	I_{DD6}	4	4	4	mA	11
	tRFC = 3.906µs (AT)	I_{DD6}	6	6	6	mA	
Self refresh current: CKE ≤ 0.2V	Standard	I_{DD7}	3	3	3	mA	12

Notes:
1. All voltages referenced to V_{SS}.
2. Minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range is ensured:
   0°C ≤ T_A ≤ +70°C (commercial)
   -40°C ≤ T_A ≤ +85°C (industrial)

-40°C ≤ T_A ≤ +105°C (automotive)

3. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC operating and I_{DD} test conditions have V_{IL} = 0V and V_{IH} = 3.0V using a measurement reference level of 1.5V. If the input transition time is longer than 1ns, then the timing is measured from $V_{IL,max}$ and $V_{IH,min}$ and no longer from the 1.5V midpoint. CLK should always be 1.5V referenced to crossover. Refer to Micron technical note TN-48-09.
5. I_{DD} specifications are tested after the device is properly initialized.
6. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
7. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
8. Address transitions average one transition every 2 clocks.
9. For -75, CL = 3 and ^{t}CK = 7.5ns; for -7E, CL = 2 and ^{t}CK = 7.5ns, and CL = 3 and ^{t}CK = 6ns.
10. Other input signals are allowed to transition no more than once every 2 clocks and are otherwise at valid V_{IH} or V_{IL} levels.
11. CKE is HIGH during refresh command period ^{t}RFC (MIN) else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.
12. Enables on-chip refresh and address counters.