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# SDR SDRAM

**MT48LC16M4A2 – 4 Meg x 4 x 4 Banks**

**MT48LC8M8A2 – 2 Meg x 8 x 4 Banks**

**MT48LC4M16A2 – 1 Meg x 16 x 4 Banks**

## Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full-page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh modes: standard and low-power (not available on AT devices)
- Auto refresh
  - 64ms, 4096-cycle refresh (commercial and industrial)
  - 16ms, 4096-cycle refresh (automotive)
- LVTTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply

## Options

- Configuration
  - 16 Meg x 4 (4 Meg x 4 x 4 banks)
  - 8 Meg x 8 (2 Meg x 8 x 4 banks)
  - 4 Meg x 16 (1 Meg x 16 x 4 banks)
- Write recovery (<sup>t</sup>WR)

## Marking

16M4<sup>3</sup>  
8M8  
4M16

## Options

- <sup>t</sup>WR = 2 CLK
- Plastic package – OCPL<sup>1</sup>
  - 54-pin TSOP II (400 mil)
  - 54-pin TSOP II (400 mil) Pb-free
  - 54-ball VFBGA (x16 only) (8mm x 8mm)
  - 54-ball VFBGA (x16 only) (8mm x 8mm)
- Timing – cycle time
  - 6ns @ CL = 3 (x16 only)
  - 6ns @ CL = 3
  - 7.5ns @ CL = 3 (PC133)
  - 7.5ns @ CL = 2 (PC133)
- Self refresh
  - Standard
  - Low-power
- Operating temperature range
  - Commercial (0°C to +70°C)
  - Industrial (–40°C to +85°C)
  - Automotive (–40°C to +105°C)
- Revision

## Marking

A2  
TG  
P  
F4  
B4<sup>2</sup>  
–6<sup>3</sup>  
–6A  
–75<sup>3</sup>  
–7E  
None  
L<sup>3</sup>  
None  
IT  
AT<sup>2</sup>  
:G, :J

- Notes:
1. Off-center parting line.
  2. Contact Micron for availability.
  3. Available only on Revision G.

**Table 1: Key Timing Parameters**

CL = CAS (READ) latency

Speed Grade	Clock Frequency (MHz)	Target <sup>t</sup> RCD- <sup>t</sup> RP-CL	<sup>t</sup> RCD (ns)	<sup>t</sup> RP (ns)	CL (ns)
-6	167	3-3-3	18	18	18
-6A	167	3-3-3	18	18	18
-75	133	3-3-3	20	20	20
-7E	133	2-2-2	15	15	15

**Table 2: Address Table**

Parameter	16 Meg x 4	8 Meg x 8	4 Meg x 16
Configuration	4 Meg x 4 x 4 banks	2 Meg x 8 x 4 banks	1 Meg x 16 x 4 banks
Refresh count	4K	4K	4K
Row addressing	4K A[11:0]	4K A[11:0]	4K A[11:0]
Bank addressing	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]
Column addressing	1K A[9:0]	512 A[8:0]	256 A[7:0]

**Table 3: 64Mb SDR Part Numbering**

Part Numbers	Architecture	Package
MT48LC16M4A2TG	16 Meg x 4	54-pin TSOP II
MT48LC16M4A2P	16 Meg x 4	54-pin TSOP II
MT48LC8M8A2TG	8 Meg x 8	54-pin TSOP II
MT48LC8M8A2P	8 Meg x 8	54-pin TSOP II
MT48LC4M16A2TG	4 Meg x 16	54-pin TSOP II
MT48LC4M16A2P	4 Meg x 16	54-pin TSOP II
MT48LC4M16A2B4 <sup>1</sup>	4 Meg x 16	54-ball VFBGA
MT48LC4M16A2F4 <sup>1</sup>	4 Meg x 16	54-ball VFBGA

Note: 1. FBGA Device Decoder: [www.micron.com/decoder](http://www.micron.com/decoder).

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## General Description

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 16,777,216-bit banks is organized as 4096 rows by 1024 columns by 4 bits. Each of the x8's 16,777,216-bit banks is organized as 4096 rows by 512 columns by 8 bits. Each of the x16's 16,777,216-bit banks is organized as 4096 rows by 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank; A[11:0] select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the  $2n$  rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 64Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAM devices offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

## Automotive Temperature

The automotive temperature (AT) option adheres to the following specifications:

- 16ms refresh rate
- Self refresh not supported
- Ambient and case temperature cannot be less than  $-40^{\circ}\text{C}$  or greater than  $+105^{\circ}\text{C}$



## Functional Block Diagrams

Figure 1: 16 Meg x 4 Functional Block Diagram

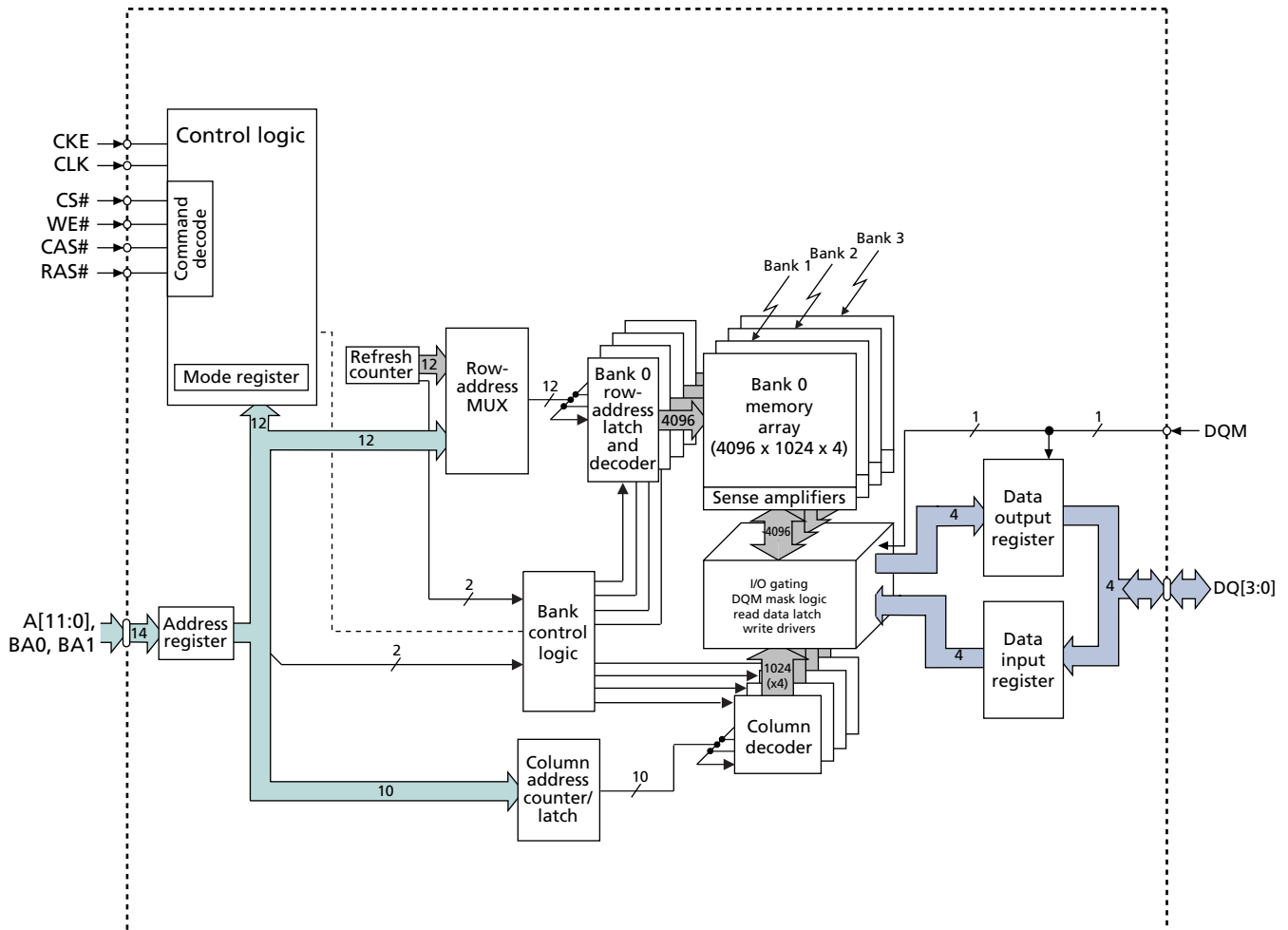


Figure 2: 8 Meg x 8 Functional Block Diagram

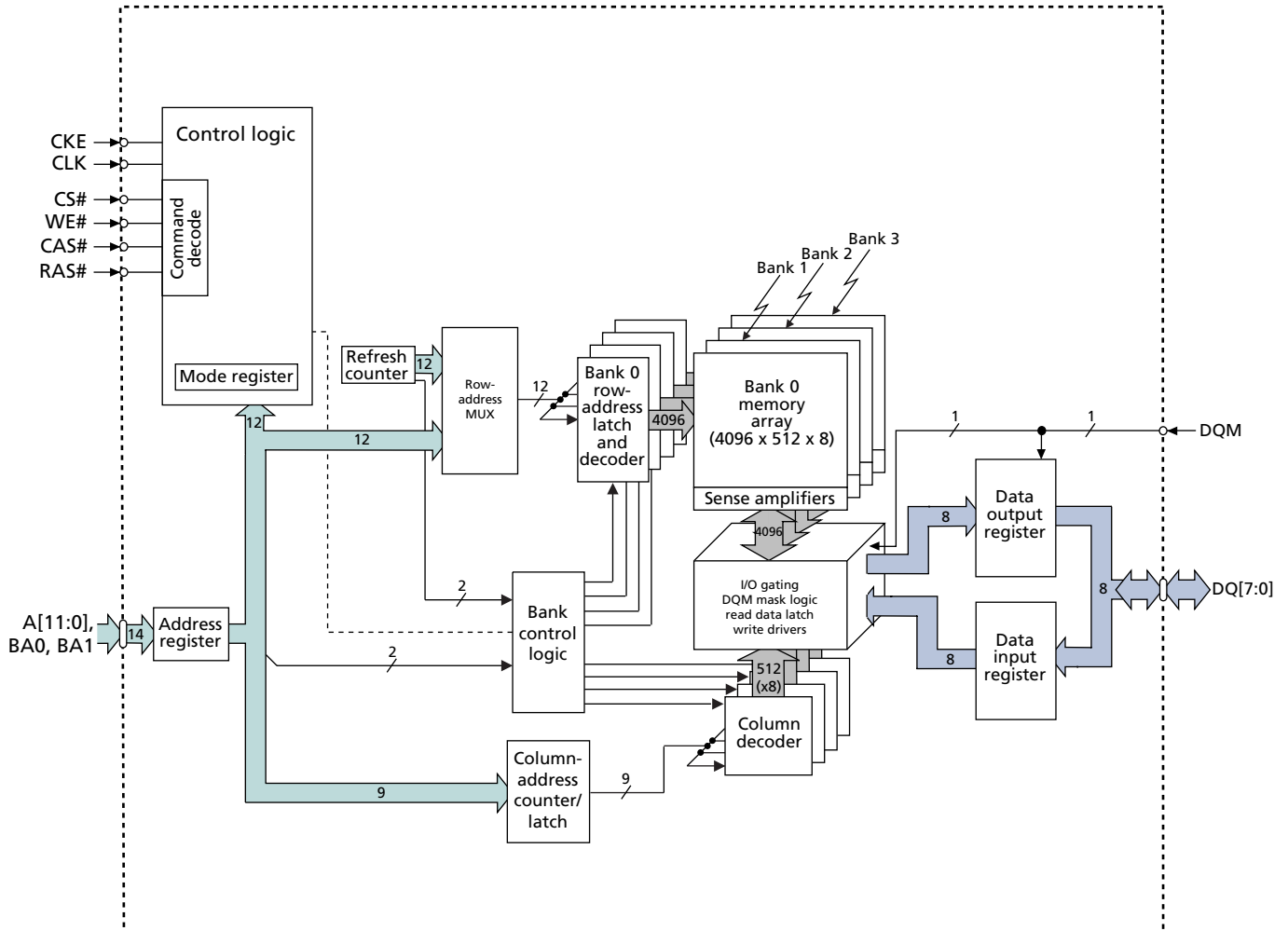
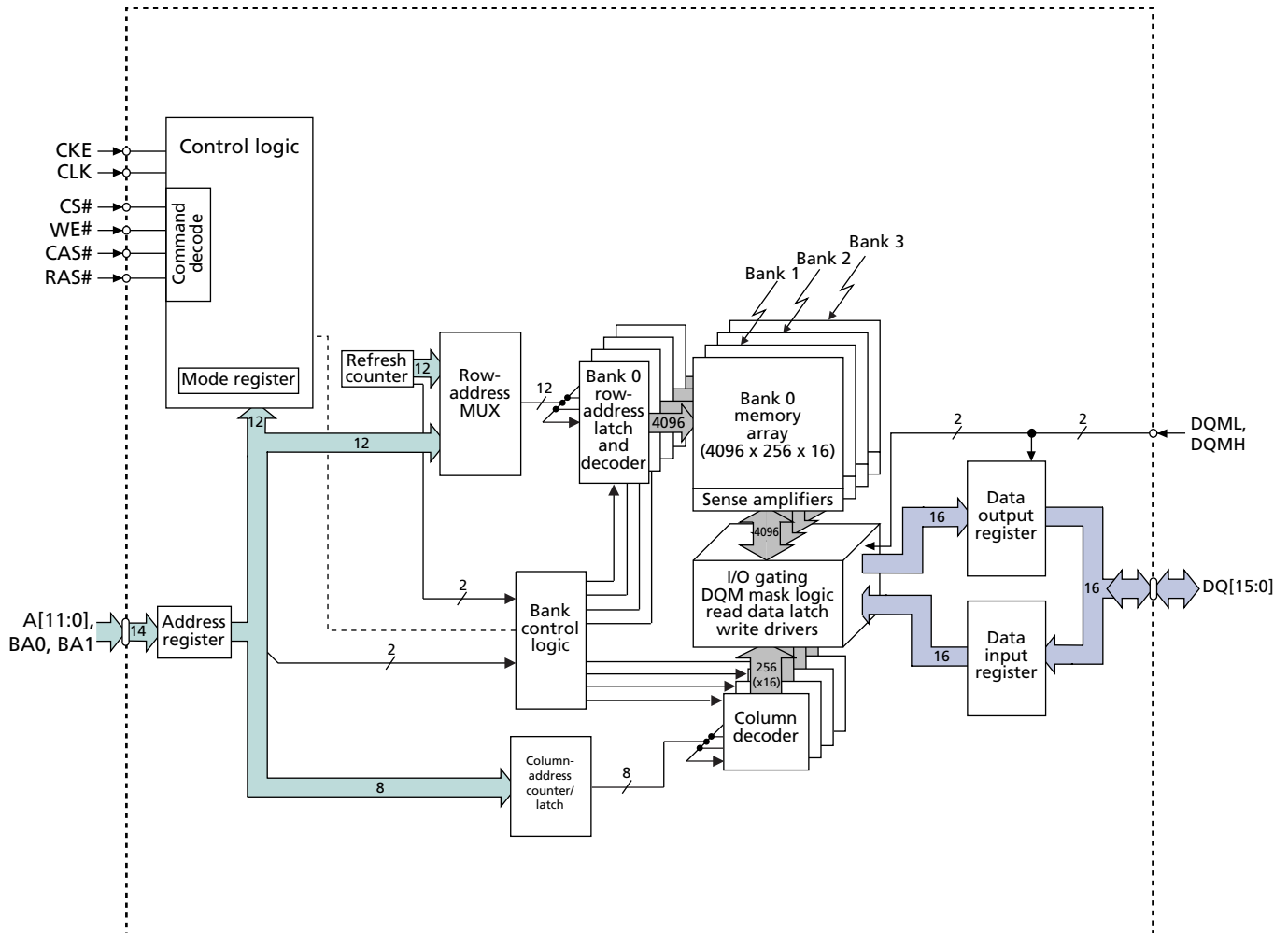


Figure 3: 4 Meg x 16 Functional Block Diagram



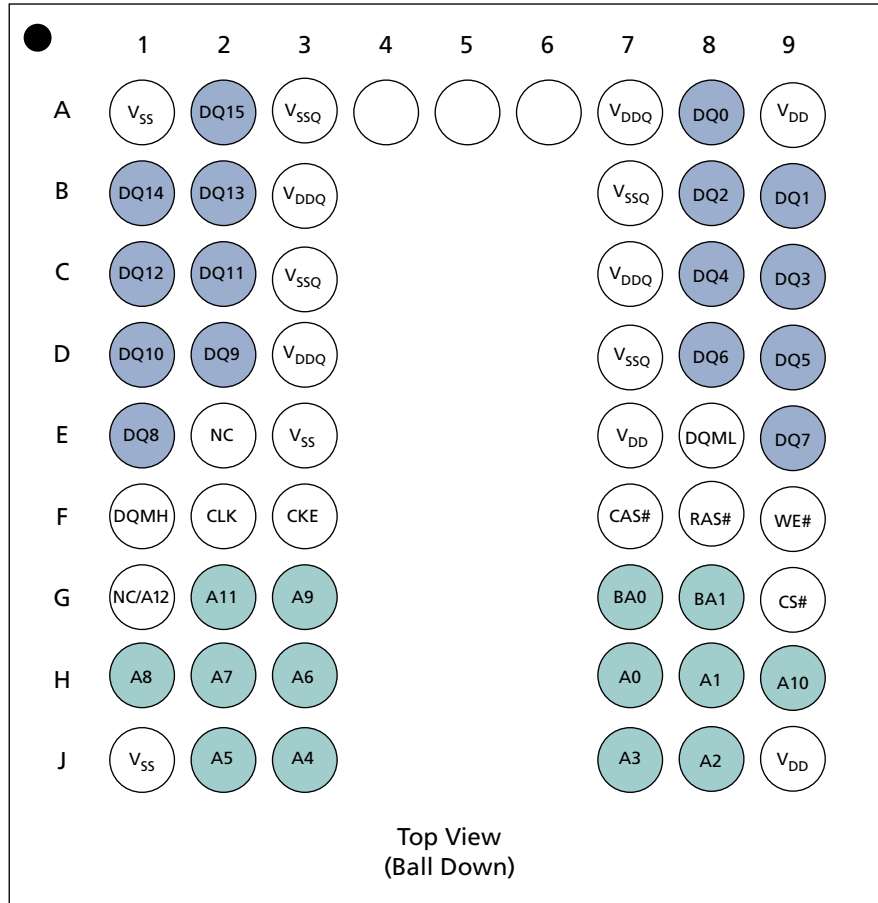
## Pin and Ball Assignments and Descriptions

**Figure 4: 54-Pin TSOP (Top View)**

x4	x8	x16				x16	x8	x4
-	-	V <sub>DD</sub>	□	1 •	54	□	V <sub>SS</sub>	-
NC	DQ0	DQ0	■	2	53	■	DQ15	DQ7
-	-	V <sub>DDQ</sub>	□	3	52	□	V <sub>SSQ</sub>	-
NC	NC	DQ1	■	4	51	■	DQ14	NC
DQ0	DQ1	DQ2	■	5	50	■	DQ13	DQ6
-	-	V <sub>SSQ</sub>	□	6	49	□	V <sub>DDQ</sub>	-
NC	NC	DQ3	■	7	48	■	DQ12	NC
NC	DQ2	DQ4	■	8	47	■	DQ11	DQ5
-	-	V <sub>DDQ</sub>	□	9	46	□	V <sub>SSQ</sub>	-
NC	NC	DQ5	■	10	45	■	DQ10	NC
DQ1	DQ3	DQ6	■	11	44	■	DQ9	DQ4
-	-	V <sub>SSQ</sub>	□	12	43	□	V <sub>DDQ</sub>	-
NC	NC	DQ7	■	13	42	■	DQ8	NC
-	-	V <sub>DD</sub>	□	14	41	□	V <sub>SS</sub>	-
NC	NC	DQML	□	15	40	□	NC	-
-	-	WE#	□	16	39	□	DQMH	DQM
-	-	CAS#	□	17	38	□	CLK	-
-	-	RAS#	□	18	37	□	CKE	-
-	-	CS#	□	19	36	□	NC	-
-	-	BA0	■	20	35	■	A11	-
-	-	BA1	■	21	34	■	A9	-
-	-	A10	■	22	33	■	A8	-
-	-	A0	■	23	32	■	A7	-
-	-	A1	■	24	31	■	A6	-
-	-	A2	■	25	30	■	A5	-
-	-	A3	■	26	29	■	A4	-
-	-	V <sub>DD</sub>	□	27	28	□	V <sub>SS</sub>	-

- Notes: 1. A dash (-) indicates that the x8 and x4 pin function is the same as the x16 pin function.  
 2. Package may or may not be assembled with a location notch.

**Figure 5: 54-Ball VFBGA x16 (Top View)**



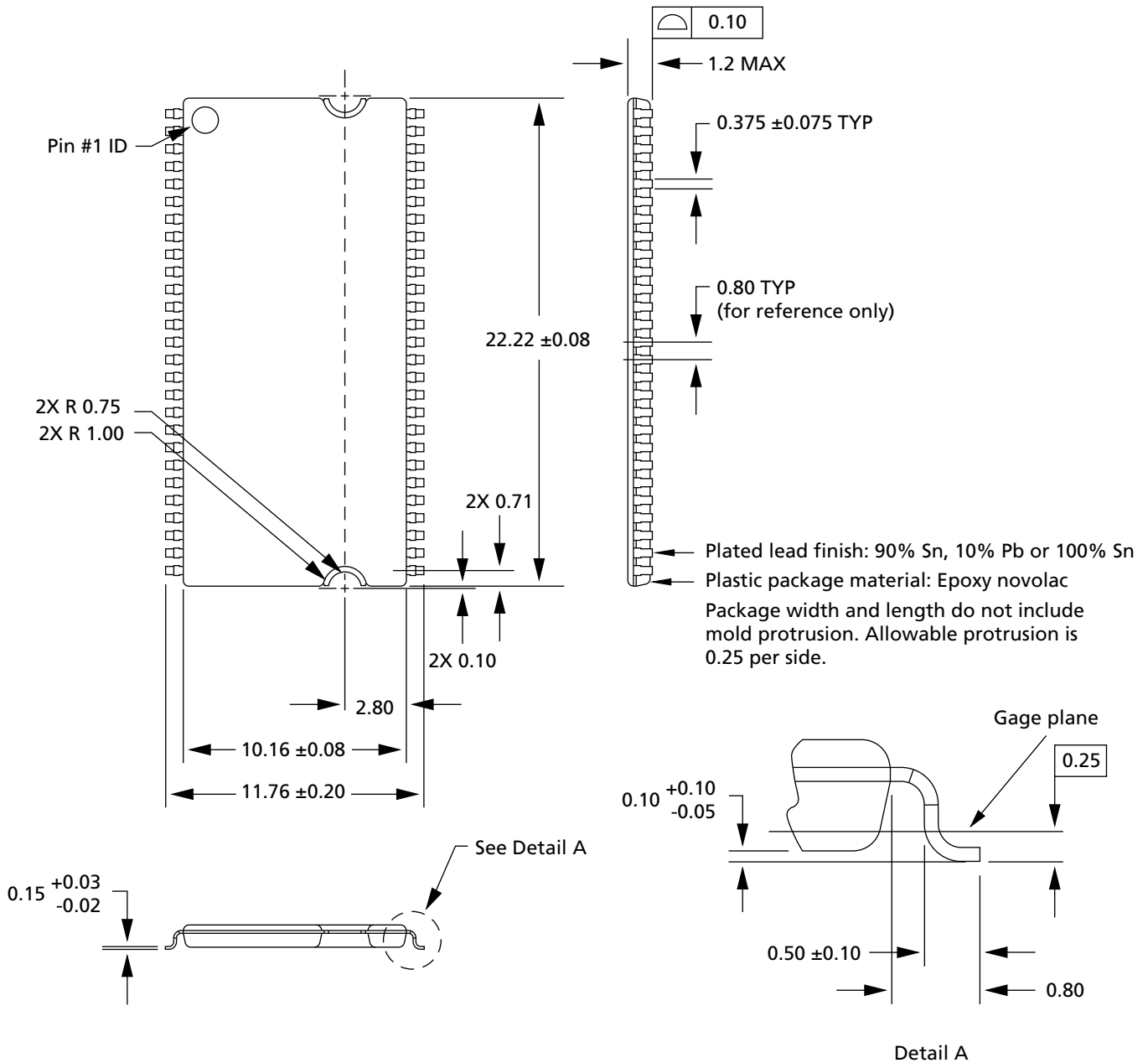
Note: 1. The balls at A4, A5, and A6 are absent from the physical package. They are included to illustrate that rows 4, 5, and 6 exist, but contain no solder balls.

**Table 4: Pin and Ball Descriptions**

Symbol	Type	Description
CLK	Input	<b>Clock:</b> CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	<b>Clock enable:</b> CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
CS#	Input	<b>Chip select:</b> CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while CS# is HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with CS#) define the command being entered.
x4, x8: DQM  x16: DQML, DQMH	Input	<b>Input/output mask:</b> DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are High-Z (two-clock latency) during a READ cycle. On the x4 and x8, DQML (pin 15) is NC; DQMH is DQM. On the x16, DQML corresponds to DQ[7:0] and DQMH corresponds to DQ[15:8]. DQML and DQMH are considered same-state when referenced as DQM.
BA[1:0]	Input	<b>Bank address input(s):</b> BA[1:0] define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A[11:0]	Input	<b>Address inputs:</b> A[11:0] are sampled during the ACTIVE command (row address A[11:0]) and READ or WRITE command (column address A[9:0] for x4; A[8:0] for x8; A[7:0] for x16; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10 HIGH) or bank selected by BA[1:0] (A1 LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
x16: DQ[15:0]	I/O	<b>Data input/output:</b> Data bus for x16 (pins 4, 7, 10, 13, 42, 45, 48, and 51 are NC for x8; and pins 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, and 53 are NC for x4).
x8: DQ[7:0]	I/O	<b>Data input/output:</b> Data bus for x8 (pins 2, 8, 47, 53 are NC for x4).
x4: DQ[3:0]	I/O	<b>Data input/output:</b> Data bus for x4.
V <sub>DDQ</sub>	Supply	<b>DQ power:</b> DQ power to the die for improved noise immunity.
V <sub>SSQ</sub>	Supply	<b>DQ ground:</b> DQ ground to the die for improved noise immunity.
V <sub>DD</sub>	Supply	<b>Power supply:</b> 3.3V ±0.3V.
V <sub>SS</sub>	Supply	Ground.
NC	–	<b>No connect:</b> These should be left unconnected.

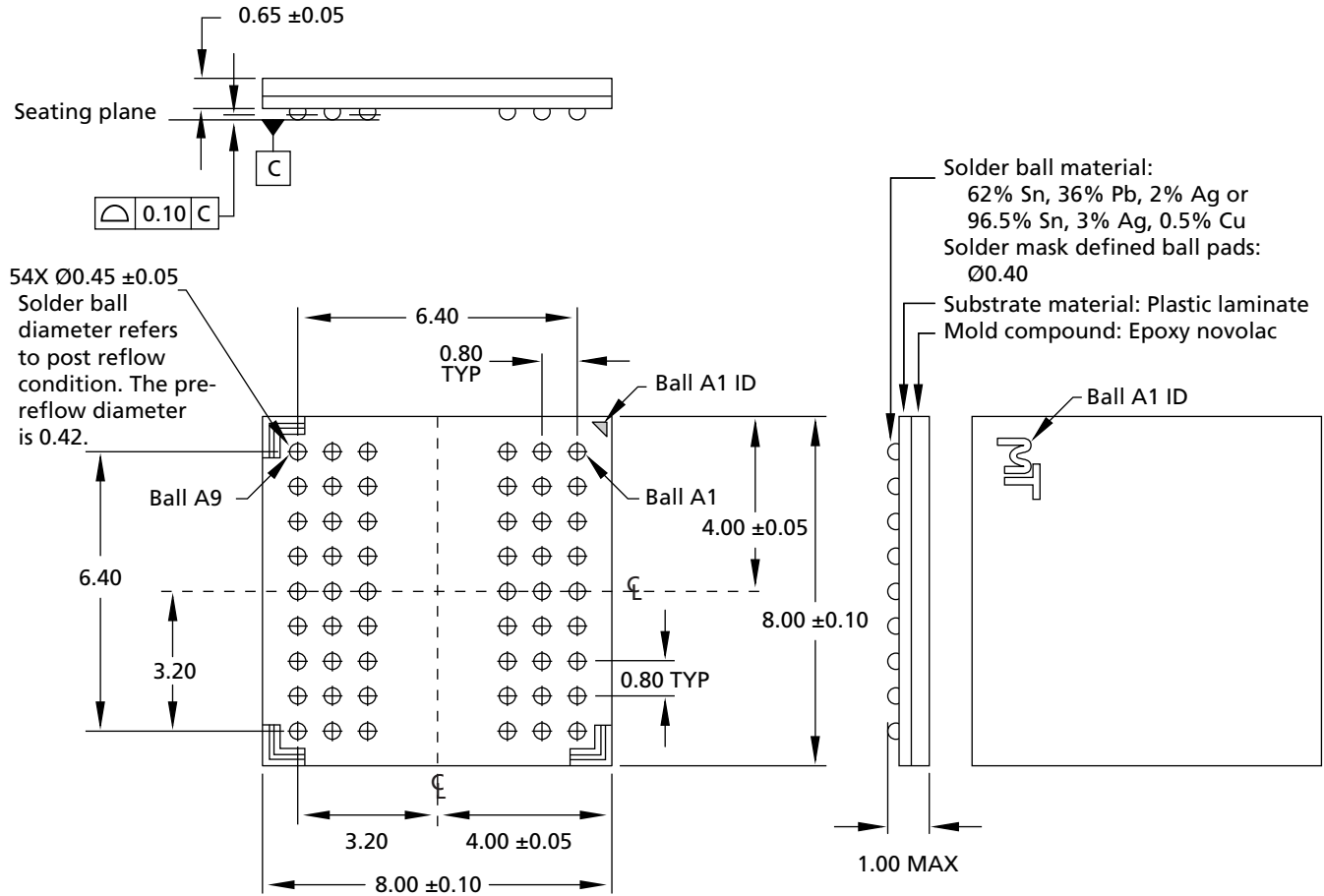
## Package Dimensions

**Figure 6: 54-Pin Plastic TSOP (400 mil) – Package Codes TG/P**



- Notes:
1. All dimensions are in millimeters.
  2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
  3. Package may or may not be assembled with a location notch.

**Figure 7: 54-Ball VFBGA (8mm x 8mm) – Package Codes F4/B4**



- Notes: 1. All dimensions are in millimeters.  
2. Recommended pad size =  $\varnothing 0.4$ mm SMD.



## Temperature and Thermal Impedance

It is imperative that the SDRAM device's temperature specifications, shown in Temperature Limits below, be maintained to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 6 (page 17) for the applicable die revision and packages being made available. These thermal impedance values vary according to the density, package, and particular design used for each device.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed in Table 6 (page 17). To ensure the compatibility of current and future designs, contact Micron Applications Engineering to confirm thermal impedance values.

The SDRAM device's safe junction temperature range can be maintained when the  $T_C$  specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

**Table 5: Temperature Limits**

Parameter		Symbol	Min	Max	Unit	Notes
Operating case temperature	Commercial	$T_C$	0	80	°C	1, 2, 3, 4
	Industrial		-40	90		
	Automotive		-40	105		
Junction temperature	Commercial	$T_J$	0	85	°C	3
	Industrial		-40	95		
	Automotive		-40	110		
Ambient temperature	Commercial	$T_A$	0	70	°C	3, 5
	Industrial		-40	85		
	Automotive		-40	105		
Peak reflow temperature		$T_{PEAK}$	-	260	°C	

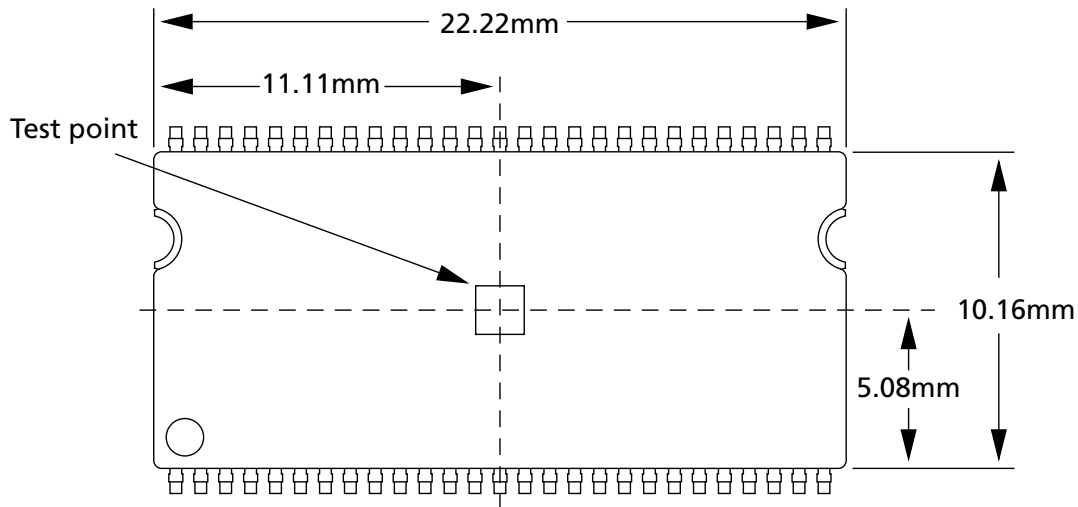
- Notes:
1. MAX operating case temperature,  $T_C$  is measured in the center of the package on the top side of the device, as shown in Figure 8 (page 17), and Figure 9 (page 18).
  2. Device functionality is not guaranteed if the device exceeds maximum  $T_C$  during operation.
  3. All temperature specifications must be satisfied.
  4. The case temperature should be measured by gluing a thermocouple to the top-center of the component. This should be done with a 1mm bead of conductive epoxy, as defined by the JEDEC EIA/JESD51 standards. Take care to ensure that the thermocouple bead is touching the case.
  5. Operating ambient temperature surrounding the package.

**Table 6: Thermal Impedance Simulated Values**

Die Revision	Package	Substrate	$\Theta_{JA}$ (°C/W) Airflow = 0m/s	$\Theta_{JA}$ (°C/W) Airflow = 1m/s	$\Theta_{JA}$ (°C/W) Airflow = 2m/s	$\Theta_{JB}$ (°C/W)	$\Theta_{JC}$ (°C/W)
G	54-pin TSOP	High Conductivity	70.5	61.2	57.2	54.6	13.7
	54-ball VFBGA	Low Conductivity	80.6	67.7	61.5	46.1	4.9
		High Conductivity	63.96	57.1	53.5	45.7	
J	54-pin TSOP	Low Conductivity	122.3	105.6	98.1	89.5	20.7
		High Conductivity	101.9	93.5	88.8	87.6	
	54-ball VFBGA	Low Conductivity	96.9	81.9	81.9	69.5	11.5
		High Conductivity	74.0	66.3	62.7	60.7	

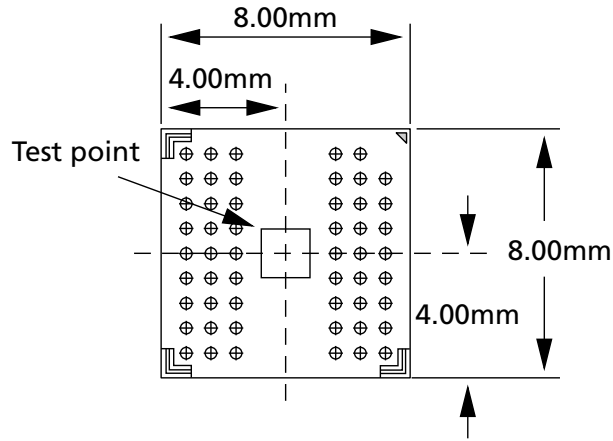
- Notes:
1. For designs expected to last beyond the die revision listed, contact Micron Applications Engineering to confirm thermal impedance values.
  2. Thermal resistance data is sampled from multiple lots, and the values should be viewed as typical.
  3. These are estimates; actual results may vary.

**Figure 8: Example: Temperature Test Point Location, 54-Pin TSOP (Top View)**



Note: 1. Package may or may not be assembled with a location notch.

Figure 9: Example: Temperature Test Point Location, 54-Ball VFBGA (Top View)



## Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 7: Absolute Maximum Ratings**

Voltage/Temperature	Symbol	Min	Max	Unit
Voltage on $V_{DD}/V_{DDQ}$ supply relative to $V_{SS}$	$V_{DD}/V_{DDQ}$	-1	4.6	V
Voltage on inputs, NC, or I/O balls relative to $V_{SS}$	$V_{IN}$	-1	4.6	
Storage temperature (plastic)	$T_{STG}$	-55	150	°C
Power dissipation	-	-	1	W

**Table 8: DC Electrical Characteristics and Operating Conditions**

Notes 1–3 apply to all parameters and conditions;  $V_{DD}/V_{DDQ} = 3.3V \pm 0.3V$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Supply voltage	$V_{DD}, V_{DDQ}$	3	3.6	V	
Input high voltage: Logic 1; All inputs	$V_{IH}$	2	$V_{DD} + 0.3$	V	4
Input low voltage: Logic 0; All inputs	$V_{IL}$	-0.3	0.8	V	4
Output high voltage: $I_{OUT} = -4mA$	$V_{OH}$	2.4	-	V	
Output low voltage: $I_{OUT} = 4mA$	$V_{OL}$	-	0.4	V	
Input leakage current: Any input $0V \leq V_{IN} \leq V_{DD}$ (All other balls not under test = 0V)	$I_L$	-5	5	$\mu A$	
Output leakage current: DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$	$I_{OZ}$	-5	-5	$\mu A$	
Operating temperature:	Commercial	$T_A$	0	70	°C
	Industrial	$T_A$	-40	85	°C
	Automotive	$T_A$	-40	105	°C

- Notes:
- All voltages referenced to  $V_{SS}$ .
  - The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured; ( $0^\circ C \leq T_A \leq +70^\circ C$  (commercial),  $-40^\circ C \leq T_A \leq +85^\circ C$  (industrial), and  $-40^\circ C \leq T_A \leq +105^\circ C$  (automotive)).
  - An initial pause of 100 $\mu s$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ( $V_{DD}$  and  $V_{DDQ}$  must be powered up simultaneously.  $V_{SS}$  and  $V_{SSQ}$  must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
  - $V_{IH}$  overshoot:  $V_{IH,max} = V_{DDQ} + 2V$  for a pulse width  $\leq 3ns$ , and the pulse width cannot be greater than one-third of the cycle rate.  $V_{IL}$  undershoot:  $V_{IL,min} = -2V$  for a pulse width  $\leq 3ns$ .

**Table 9: Capacitance**

Note 1 applies to all parameters and conditions

Package	Parameter	Symbol	Min	Max	Unit	Notes
TSOP package	Input capacitance: CLK	$C_{L1}$	2.5	3.5	pF	2
	Input capacitance: All other input-only balls	$C_{L2}$	2.5	3.8	pF	3
	Input/output capacitance: DQ	$C_{L0}$	4	6	pF	4
VFPGA package	Input capacitance: CLK	$C_{L1}$	1.5	3.5	pF	2
	Input capacitance: All other input-only balls	$C_{L2}$	1.5	3.8	pF	3
	Input/output capacitance: DQ	$C_{L0}$	3	6	pF	4

- Notes:
1. This parameter is sampled.  $V_{DD}$ ,  $V_{DDQ} = 3.3V$ ;  $f = 1$  MHz,  $T_A = 25^\circ C$ ; pin under test biased at 1.4V.
  2. PC100 specifies a maximum of 4pF.
  3. PC100 specifies a maximum of 5pF.
  4. PC100 specifies a maximum of 6.5pF.

## Electrical Specifications – I<sub>DD</sub> Parameters

**Table 10: I<sub>DD</sub> Specifications and Conditions – Revision G**

Notes 1–3 apply to all parameters and conditions; V<sub>DD</sub>/V<sub>DDQ</sub> = 3.3V ±0.3V

Parameter/Condition	Symbol	Max			Unit	Notes	
		-6	-7E	-75			
Operating current: Active mode; Burst = 2; READ or WRITE; t <sub>RC</sub> ≥ t <sub>RC</sub> (MIN)	I <sub>DD1</sub>	150	125	115	mA	4, 5, 6, 7	
Standby current: Power-down mode; All banks idle; CKE = LOW	I <sub>DD2</sub>	2	2	2	mA	7	
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after t <sub>RCD</sub> met; No accesses in progress	I <sub>DD3</sub>	60	45	45	mA	4, 6, 7, 8	
Operating current: Burst mode; Page burst; READ or WRITE; All banks active	I <sub>DD4</sub>	180	150	140	mA	4, 5, 6, 7	
Auto refresh current: CKE = HIGH; CS# = HIGH	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub>	250	230	210	mA	4, 5, 6, 7, 8, 9
	t <sub>RFC</sub> = 15.625μs	I <sub>DD6</sub>	3	3	3	mA	
	t <sub>RFC</sub> = 3.906μs (AT)	I <sub>DD6</sub>	6	6	6	mA	
Self refresh current: CKE ≤ 0.2V	Standard	I <sub>DD7</sub>	1	1	1	mA	10
	Low power (L)	I <sub>DD7</sub>	0.5	0.5	0.5	mA	

**Table 11: I<sub>DD</sub> Specifications and Conditions – Revision J**

Notes 1–3 apply to all parameters and conditions; V<sub>DD</sub>/V<sub>DDQ</sub> = 3.3V ±0.3V

Parameter/Condition	Symbol	Max			Unit	Notes	
		-6A	-7E	-75			
Operating current: Active mode; Burst = 2; READ or WRITE; t <sub>RC</sub> ≥ t <sub>RC</sub> (MIN)	I <sub>DD1</sub>	100	100	100	mA	4, 5, 6, 7	
Standby current: Power-down mode; All banks idle; CKE = LOW	I <sub>DD2</sub>	2.5	2.5	2.5	mA	7	
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after t <sub>RCD</sub> met; No accesses in progress	I <sub>DD3</sub>	35	35	35	mA	4, 6, 7, 8	
Operating current: Burst mode; Page burst; READ or WRITE; All banks active	I <sub>DD4</sub>	100	100	100	mA	4, 5, 6, 7	
Auto refresh current: CKE = HIGH; CS# = HIGH	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub>	150	150	150	mA	4, 5, 6, 7, 8, 9
	t <sub>RFC</sub> = 15.625μs	I <sub>DD6</sub>	4	4	4	mA	
	t <sub>RFC</sub> = 3.906μs (AT)	I <sub>DD6</sub>	6	6	6	mA	
Self refresh current: CKE ≤ 0.2V	Standard	I <sub>DD7</sub>	3	3	3	mA	10

- Notes:
1. All voltages referenced to V<sub>SS</sub>.
  2. Minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured:  
 0°C ≤ TA ≤ +70°C (commercial)  
 -40°C ≤ TA ≤ +85°C (industrial)

–40°C ≤ TA ≤ +105°C (automotive)

3. An initial pause of 100μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V<sub>DD</sub> and V<sub>DDQ</sub> must be powered up simultaneously. V<sub>SS</sub> and V<sub>SSQ</sub> must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the t<sub>REF</sub> refresh requirement is exceeded.
4. I<sub>DD</sub> is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. The I<sub>DD</sub> current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
6. Address transitions average one transition every two clocks.
7. For -75, CL = 3 and t<sub>CK</sub> = 7.5ns; for -7E, CL = 2 and t<sub>CK</sub> = 7.5ns; for -6, CL = 3 and t<sub>CK</sub> = 6ns.
8. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V<sub>IH</sub> or V<sub>IL</sub> levels.
9. CKE is HIGH during refresh command period t<sub>RFC</sub> (MIN) else CKE is LOW. The I<sub>DD6</sub> limit is actually a nominal value and does not result in a fail value.
10. Enables on-chip refresh and address counters.



## Electrical Specifications – AC Operating Conditions

**Table 12: Electrical Characteristics and Recommended AC Operating Conditions**

Notes 1–6 apply to all parameters and conditions

Parameter		Symbol	-6		-6A		-7E		-75		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Access time from CLK (positive edge)	CL = 3	$t_{AC(3)}$	–	5.5	–	5.4	–	5.4	–	5.4	ns	8
	CL = 2	$t_{AC(2)}$	–	7.5	–	7.5 <sup>7</sup>	–	5.4	–	6	ns	8
	CL = 1	$t_{AC(1)}$	–	17	–	17 <sup>7</sup>	–	–	–	–	ns	8
Address hold time		$t_{AH}$	1	–	0.8	–	0.8	–	0.8	–	ns	
Address setup time		$t_{AS}$	1.5	–	1.5	–	1.5	–	1.5	–	ns	
CLK high-level width		$t_{CH}$	2.5	–	2.5	–	2.5	–	2.5	–	ns	
CLK low-level width		$t_{CL}$	2.5	–	2.5	–	2.5	–	2.5	–	ns	
Clock cycle time	CL = 3	$t_{CK(3)}$	6	–	6	–	7	–	7.5	–	ns	9
	CL = 2	$t_{CK(2)}$	10	–	10 <sup>7</sup>	–	7.5	–	10	–	ns	9
	CL = 1	$t_{CK(1)}$	20	–	20 <sup>7</sup>	–	–	–	–	–	ns	9
CKE hold time		$t_{CKH}$	1	–	0.8	–	0.8	–	0.8	–	ns	
CKE setup time		$t_{CKS}$	1.5	–	1.5	–	1.5	–	1.5	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		$t_{CMH}$	1	–	0.8	–	0.8	–	0.8	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		$t_{CMS}$	1.5	–	1.5	–	1.5	–	1.5	–	ns	
Data-in hold time		$t_{DH}$	1	–	0.8	–	0.8	–	0.8	–	ns	
Data-in setup time		$t_{DS}$	1.5	–	1.5	–	1.5	–	1.5	–	ns	
Data-out High-Z time	CL = 3	$t_{HZ(3)}$	–	5.5	–	5.4	–	5.4	–	5.4	ns	10
	CL = 2	$t_{HZ(2)}$	–	7.5	–	7.5 <sup>7</sup>	–	5.4	–	6	ns	10
	CL = 1	$t_{HZ(1)}$	–	17	–	17 <sup>7</sup>	–	–	–	–	ns	10
Data-out Low-Z time		$t_{LZ}$	1	–	1	–	1	–	1	–	ns	
Data-out hold time (load)		$t_{OH}$	2	–	3	–	3	–	3	–	ns	
Data-out hold time (no load)		$t_{OHn}$	1.8	–	1.8	–	1.8	–	1.8	–	ns	11
ACTIVE-to-PRECHARGE command		$t_{RAS}$	42	120,000	42	120,000	37	120,000	44	120,000	ns	
ACTIVE-to-ACTIVE command period		$t_{RC}$	60	–	60	–	60	–	66	–	ns	12
ACTIVE-to-READ or WRITE delay		$t_{RCD}$	18	–	18	–	15	–	20	–	ns	
Refresh period (4096 rows)		$t_{REF}$	–	64	–	64	–	64	–	64	ms	
Refresh period – automotive (4096 rows)		$t_{REFAT}$	–	16	–	16	–	16	–	16	ms	
AUTO REFRESH period		$t_{RFC}$	60	–	60	–	66	–	66	–	ns	





**Table 12: Electrical Characteristics and Recommended AC Operating Conditions (Continued)**

Notes 1–6 apply to all parameters and conditions

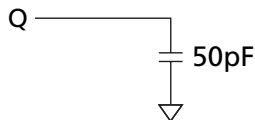
Parameter	Symbol	-6		-6A		-7E		-75		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
PRECHARGE command period	$t_{RP}$	18	–	18	–	15	–	20	–	ns	
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command	$t_{RRD}$	12	–	12	–	14	–	15	–	ns	
Transition time	$t_T$	0.3	1.2	0.3	1.2	0.3	1.2	0.3	1.2	ns	13
WRITE recovery time	$t_{WR}$	1 CLK + 6ns	–	1 CLK + 6ns	–	1 CLK + 7ns	–	1 CLK + 7.5ns	–	ns	14
		12	–	12	–	14	–	15	–		15
Exit SELF REFRESH-to-AC-TIVE command	$t_{XSR}$	70	–	67	–	67	–	75	–	ns	16

**Table 13: AC Functional Characteristics**

Notes 1–6 apply to all parameters and conditions

Parameter	Symbol	-6/-6A	-7E	-75	Unit	Notes	
Last data-in to burst STOP command	$t^{\text{BDL}}$	1	1	1	$t^{\text{CK}}$	17	
READ/WRITE command to READ/WRITE command	$t^{\text{CCD}}$	1	1	1	$t^{\text{CK}}$	17	
Last data-in to new READ/WRITE command	$t^{\text{CDL}}$	1	1	1	$t^{\text{CK}}$	17	
CKE to clock disable or power-down entry mode	$t^{\text{CKED}}$	1	1	1	$t^{\text{CK}}$	18	
Data-in to ACTIVE command	$t^{\text{DAL}}$	5	4	5	$t^{\text{CK}}$	19, 20	
Data-in to PRECHARGE command	$t^{\text{DPL}}$	2	2	2	$t^{\text{CK}}$	20, 21	
DQM to input data delay	$t^{\text{DQD}}$	0	0	0	$t^{\text{CK}}$	17	
DQM to data mask during WRITES	$t^{\text{DQM}}$	0	0	0	$t^{\text{CK}}$	17	
DQM to data High-Z during READS	$t^{\text{DQZ}}$	2	2	2	$t^{\text{CK}}$	17	
WRITE command to input data delay	$t^{\text{DWD}}$	0	0	0	$t^{\text{CK}}$	17	
LOAD MODE REGISTER command to ACTIVE or REFRESH command	$t^{\text{MRD}}$	2	2	2	$t^{\text{CK}}$	22	
CKE to clock enable or power-down exit setup mode	$t^{\text{PED}}$	1	1	1	$t^{\text{CK}}$	17	
Last data-in to PRECHARGE command	$t^{\text{RDL}}$	2	2	2	$t^{\text{CK}}$	20, 21	
Data-out High-Z from PRECHARGE command	CL = 3	$t^{\text{ROH}}(3)$	3	3	3	$t^{\text{CK}}$	17
	CL = 2	$t^{\text{ROH}}(2)$	2	2	2	$t^{\text{CK}}$	17
	CL = 1	$t^{\text{ROH}}(1)$	1	–	–	$t^{\text{CK}}$	17

- Notes:
- Minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured:  
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$  (commercial)  
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  (industrial)  
 $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$  (automotive)
  - An initial pause of 100 $\mu\text{s}$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ( $V_{\text{DD}}$  and  $V_{\text{DDQ}}$  must be powered up simultaneously.  $V_{\text{SS}}$  and  $V_{\text{SSQ}}$  must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the  $t^{\text{REF}}$  refresh requirement is exceeded.
  - In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{\text{IH}}$  and  $V_{\text{IL}}$  (or between  $V_{\text{IL}}$  and  $V_{\text{IH}}$ ) in a monotonic manner.
  - Outputs measured at 1.5V with equivalent load:



- AC operating and  $I_{\text{DD}}$  test conditions have  $V_{\text{IL}} = 0\text{V}$  and  $V_{\text{IH}} = 3.0\text{V}$  using a measurement reference level of 1.5V. If the input transition time is longer than 1ns, then the timing is measured from  $V_{\text{IL,max}}$  and  $V_{\text{IH,min}}$  and no longer from the 1.5V midpoint. CLK should always be 1.5V referenced to crossover. Refer to Micron technical note TN-48-09.
- The -6 speed grade does not support CL = 2.
- Not applicable for Revision G.