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Mobile SDRAM

MT48LC8M16LF, MT48V8M16LF, MT48LC4M32LF, MT48V4M32LF

Features

- Temperature-compensated self refresh (TCSR)
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge, and auto refresh modes
- Self refresh mode; standard and low power (not available on AT devices)
- Auto refresh
  - 64ms, 4,096-cycle refresh (15.6µs/row) (commercial and industrial)
  - 16ms, 4,096-cycle refresh (3.9µs/row) (automotive)
- LVTTL-compatible inputs and outputs
- Low voltage power supply
- Partial-array self refresh (PASR) power-saving mode

Table 1: Key Timing Parameters
CL = CAS (READ) latency

Speed Grade	Clock Frequency	Access Time			^tRCD	^tRP
		CL = 1	CL = 2	CL = 3		
-75M	133 MHz	–	–	5.4	19ns	19ns
-8	125 MHz	–	–	7ns	20ns	20ns
-10	100 MHz	–	–	7ns	20ns	20ns
-75M	100 MHz	–	6	–	19ns	19ns
-8	100 MHz	–	8ns	–	20ns	20ns
-10	83 MHz	–	8ns	–	20ns	20ns
-8	50 MHz	19ns	–	–	20ns	20ns
-10	40 MHz	22ns	–	–	20ns	20ns

Options

Options	Mark
• VDD/VDDQ	
– 3.3V/3.3V	LC
– 2.5V/2.5–1.8V	V
• Configurations	
– 8 Meg x 16 (2 Meg x 16 x 4 banks)	8M16
– 4 Meg x 32 (1 Meg x 32 x 4 banks)	4M32
• Package/ball out	
– 54-ball VFBGA (8mm x 8mm)[1]	F4
– 54-ball VFBGA (8mm x 8mm)[1] Pb-free	B4
– 90-ball VFBGA (8mm x 13mm)[2]	F5
– 90-ball VFBGA (8mm x 13mm)[2] Pb-free	B5
– 54-pin TSOP II (400 mil)	TG[3]
– 54-pin TSOP II (400 mil) Pb-free	P[3]
• Timing (cycle time)	
– 7.5ns @ CL = 3 (133 MHz)	-75M[3]
– 8ns @ CL = 3 (125 MHz)	-8
– 10ns @ CL = 3 (100 MHz)	-10[3]
• Temperature	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
– Automotive (–40°C to +105°C)	AT[3]
• Design revision	:G

Notes: 1. x16 only.
2. x32 only.
3. Contact Micron for availability.

Table 2: Configurations

	8 Meg x 16	4 Meg x 32
Configuration	2 Meg x 16 x 4 banks	1 Meg x 32 x 4 banks
Refresh count	4K	4K
Row addressing	4K (A0–A11)	4K (A0–A11)
Bank addressing	4 (BA0, BA1)	4 (BA0, BA1)
Column addressing	512 (A0–A8)	256 (A0–A7)

Part Number Example:
MT48V8M16LFB4-8:G

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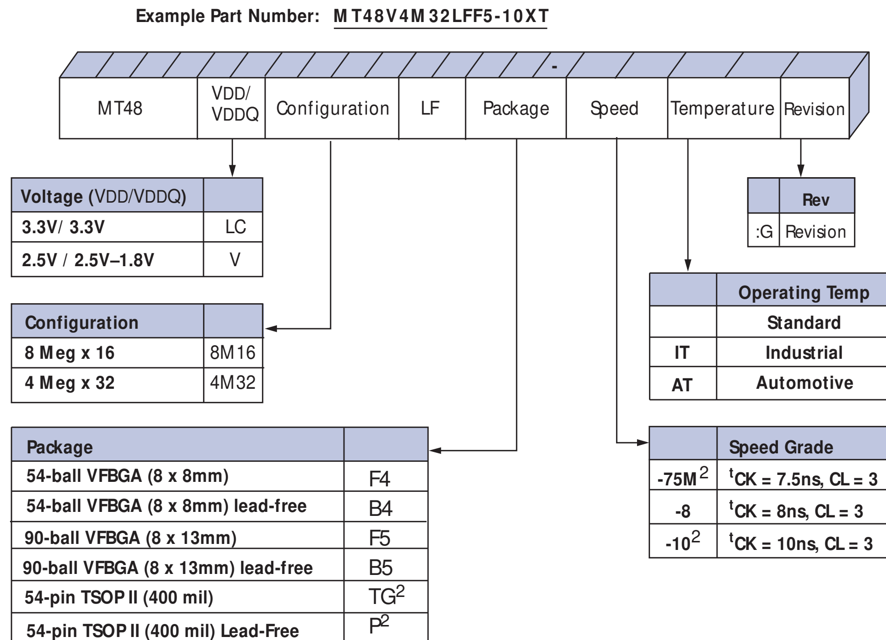
Figure 1: 128Mb SDRAM Part Numbers



Notes: 1. Not all speeds and configurations are available.
2. Contact Micron for availability.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's new FBGA Part Marking Decoder makes it easier to understand that part marking. Visit the Web site at www.micron.com/decoder.

General Description

The Micron® 128Mb SDRAM device is a high-speed CMOS, dynamic random access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits. Each of the x32's 33,554,432-bit banks is organized as 4,096 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

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The 128Mb SDRAM device uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also enables the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 128Mb SDRAM device is designed to operate in 3.3V or 2.5V low-power memory systems. The 2.5V version is compatible with 1.8V I/O interface. An auto refresh mode is provided along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Automotive Temperature

The automotive temperature (AT) option adheres to the following specifications:

- 16ms refresh rate
- Self refresh not supported
- Ambient and case temperature cannot be less than –40°C or greater than +105°C

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Figure 2: Functional Block Diagram 8 Meg x 16 SDRAM

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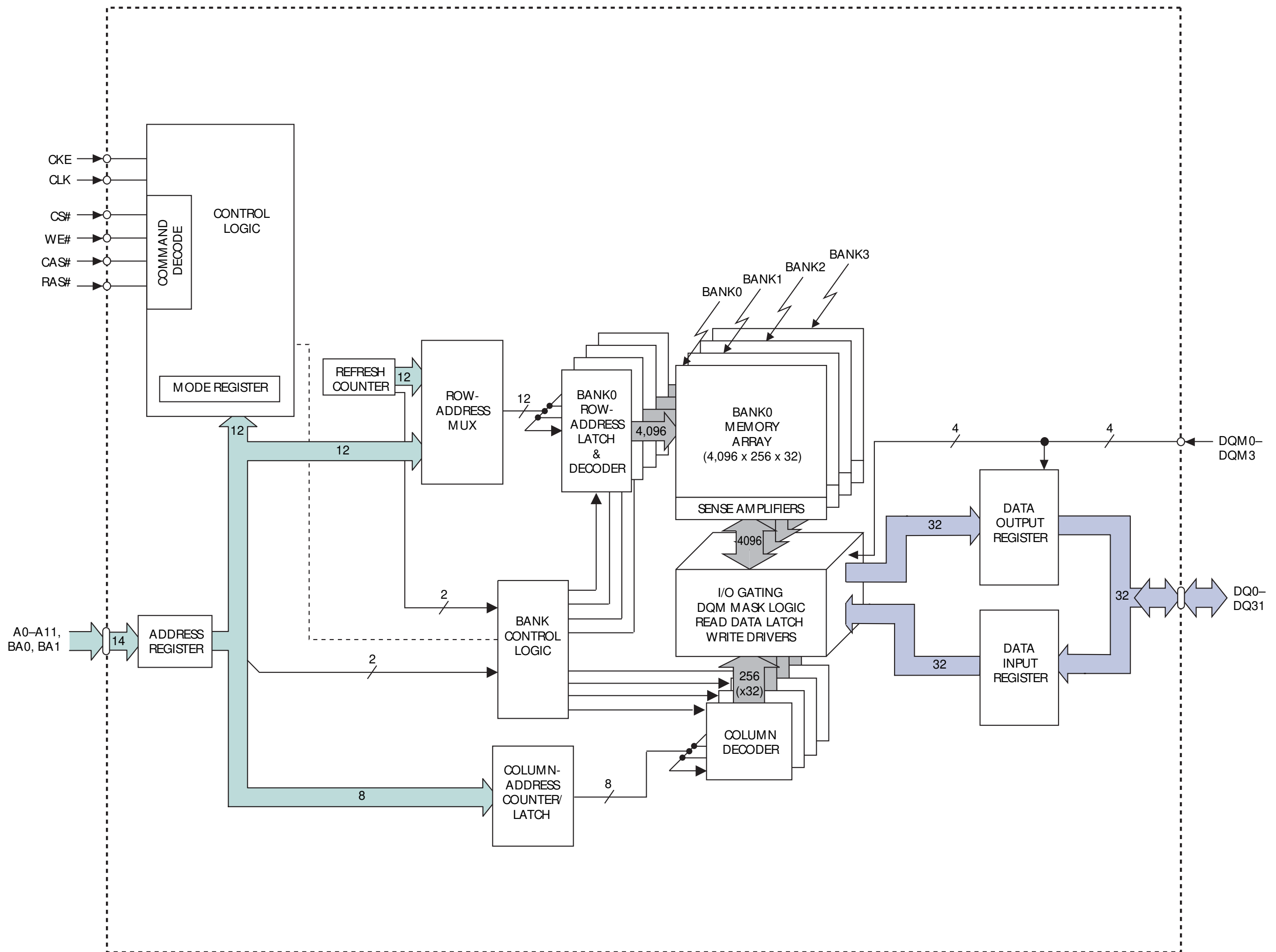
Figure 3: Functional Block Diagram 4 Meg x 32 SDRAM



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Pin/Ball Assignments and Descriptions

Figure 4: 90-Ball FBGA Pin Assignments (Top View)

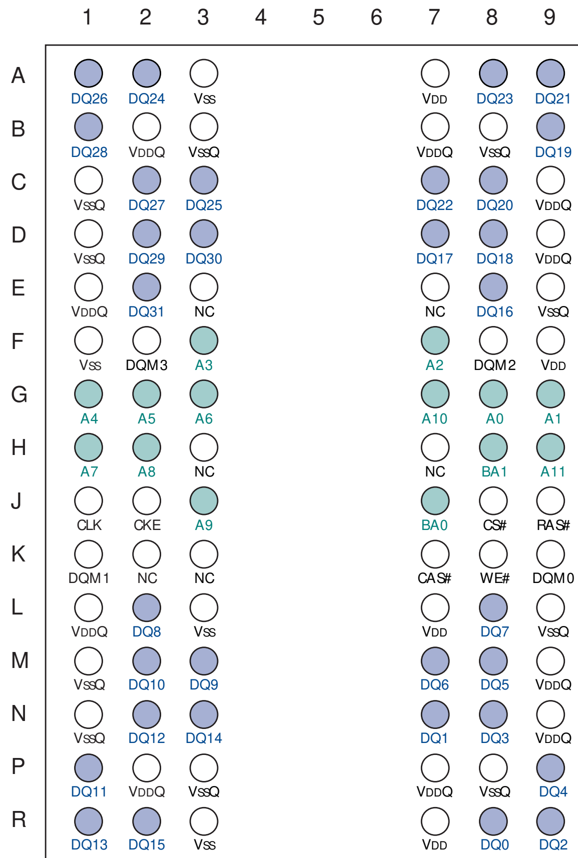

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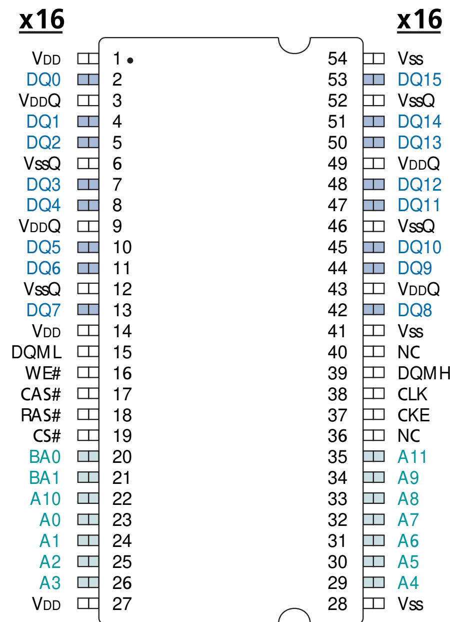
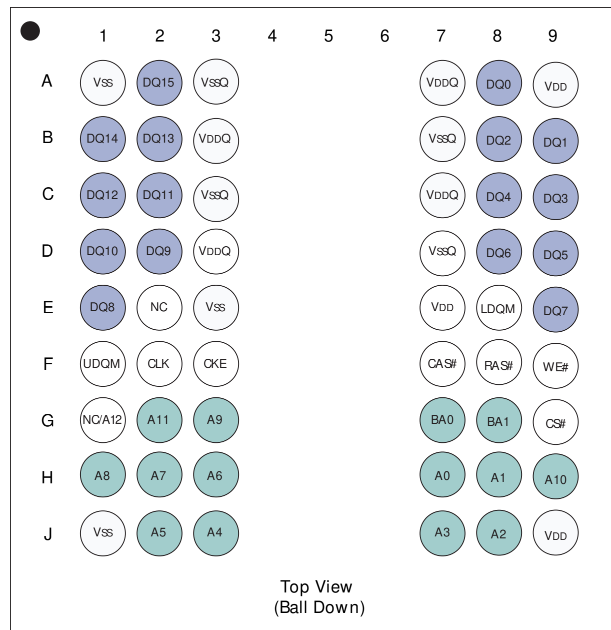
Figure 5: 54-Pin TSOP Pin Assignments (Top View)



Notes: 1. The # symbol indicates signal is active LOW.

Figure 6: 54-Ball VFBGA Pin Assignments (Top View)



Top View
(Ball Down)

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Table 3: Ball Descriptions: 54-Ball VFBGA

54-Ball VFBGA	Symbol	Type	Description
F2	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
G9	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue and DQM will retain its DQ mask capability while CS# remains HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F7, F8, F9	CAS#, RAS#, WE#	Input	Command inputs: CAS#, RAS#, and WE# (along with CS#) define the command being entered.
E8, F1	LDQM, UDQM	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (2-clock latency) during a READ cycle. LDQM corresponds to DQ0–DQ7, and UDQM corresponds to DQ8–DQ15. LDQM and UDQM are considered same state when referenced as DQM.
G7, G8	BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. These pins also provide the op-code during a LOAD MODE REGISTER command.
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2	A0–A6 A7–A11	Input	Address inputs: A0–A11 are sampled during the ACTIVE command (row-address A0–A11) and READ/WRITE command (column-address A0–A8; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	DQ0–DQ5 DQ6–DQ11 DQ12–DQ15	I/O	Data input/output: Data bus.
E2, G1	NC	–	No connect: These pins should be left unconnected. G1 is a no connect for this part but may be used as A12 in future designs.
A7, B3, C7, D3	VDDQ	Supply	DQ power: Isolated DQ power on the die to improve noise immunity.
A3, B7, C3, D7	VSSQ	Supply	DQ ground: Isolated DQ power on the die to improve noise immunity.
A9, E7, J9	VDD	Supply	Power supply: Voltage dependant on option.
A1, E3, J1	VDD	Supply	Ground.

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Table 4: Ball Descriptions: 90-Ball VFBGA

90-Ball FBGA	Symbol	Type	Description
J1	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
J2	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
J8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue and DQM will retain its DQ mask capability while CS# remains HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
J9, K7, K8	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
K9, K1, F8, F2	DQM0–3	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (2-clock latency) during a READ cycle. DQM0 corresponds to DQ0–DQ7, DQM1 corresponds to DQ8–DQ15, DQM2 corresponds to DQ16–DQ23, and DQM3 corresponds to DQ24–DQ31. DQM0–3 are considered same state when referenced as DQM.
J7, H8	BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. These pins also provide the op-code during a LOAD MODE REGISTER command.
G8, G9, F7, F3, G1, G2, G3, H1, H2, J3, G7, H9	A0–A5 A6–A11	Input	Address inputs: A0–A11 are sampled during the ACTIVE command (row-address A0–A11) and READ/WRITE command (column-address A0–A7; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
R8, N7, R9, N8, P9, M8, M7, L8, L2, M3, M2, P1, N2, R1, N3, R2, E8, D7, D8, B9, C8, A9, C7, A8, A2, C3, A1, C2, B1, D2, D3, E2	DQ0–DQ5 DQ6–DQ11 DQ12–DQ17 DQ18–DQ23 DQ24–DQ29 DQ30–DQ31	I/O	Data input/output: Data bus.
E3, E7, H3, H7, K2, K3	NC	–	No connect: These pins should be left unconnected. H3 is a no connect for this part, but may be used as A12 in future designs.
B2, B7, C9, D9, E1, L1, M9, N9, P2, P7	V_{DDQ}	Supply	DQ power: Isolated DQ power on the die to improve noise immunity.
B8, B3, C1, D1, E9, L9, M1, N1, P3, P8	V_{SSQ}	Supply	DQ ground: Isolated DQ power on the die to improve noise immunity.
A7, F9, L7, R7	V_{DD}	Supply	Power supply: Voltage dependant on option.
A3, F1, L3, R3	V_{SS}	Supply	Ground.

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Table 5: Pin Descriptions: 54-Pin TSOP (x16 Only)

54-Pin TSOP	Symbol	Type	Description
38	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
19	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue and DQM will retain its DQ mask capability while CS# remains HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
16, 17, 18	WE#, CAS#, RAS#	Input	Command inputs: WE#, CAS#, and RAS# (along with CS#) define the command being entered.
15, 39	DQML, DQMH	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (2-clock latency) during a READ cycle. DQM0 corresponds to DQ0–DQ7, DQM1 corresponds to DQ8–DQ15, DQM2 corresponds to DQ16–DQ23, and DQM3 corresponds to DQ24–DQ31. LDQM corresponds to DQ0–DQ7, and UDQM corresponds to DQ8–DQ15. LDQM and UDQM are considered same state when referenced as DQM.
20, 21	BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. These pins also provide the op-code during a LOAD MODE REGISTER command.
23, 24, 25, 29, 30, 31, 32, 33, 34, 22, 35	A0–A5 A6–A11	Input	Address inputs: A0–A11 are sampled during the ACTIVE command (row-address A0–A11) and READ/WRITE command (column-address A0–A7; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 42, 49, 45, 47, 48, 50, 51	DQ0–DQ7 DQ8–DQ15	I/O	Data input/output: Data bus (x16 only).
36, 40	NC	–	No connect: These pins should be left unconnected. Pin 36 is a no connect for this part, but may be used as A12 in future designs.
3, 9, 43, 49	VDDQ	Supply	DQ power: Isolated DQ power on the die to improve noise immunity.
6, 12, 46, 52	VSSQ	Supply	DQ ground: Isolated DQ power on the die to improve noise immunity.
1, 14, 27	VDD	Supply	Power supply: Voltage dependant on option.
28, 41, 54	VSS	Supply	Ground.

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Functional Description

In general, the 128Mb SDRAMs (2 Meg x 16 x 4 banks and 1 Meg x 32 x 4 banks) are quad-bank DRAMs that operate at 3.3V or 2.5V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits. Each of the x32's 33,554,432-bit banks is organized as 4,096 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0–A11 select the row). The address bits (x16: A0–A8; x32: A0–A7) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. After power is applied to VDD and VDDQ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands must be applied.

After the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, at least two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it must be loaded prior to applying any operational command. If desired, the two AUTO REFRESH commands can be issued after the LOAD MODE REGISTER (LMR) command.

The recommended power-up sequence for SDRAMs:

1. Simultaneously apply power to VDD and VDDQ.
2. Assert and hold CKE at a LVTTL logic LOW.
3. Provide stable CLOCK signal. Stable clock is defined as a signal cycling within timing constraints specified for the clock pin.
4. Wait at least 100µs prior to issuing any command other than a COMMAND INHIBIT or NOP.
5. Starting at some point during this 100µs period, bring CKE HIGH. Continuing at least through the end of this period, one or more COMMAND INHIBIT or NOP commands must be applied.
6. Perform a PRECHARGE ALL command.

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7. Wait at least ^{t}RP time; during this time, NOPs or DESELECT commands must be given. All banks will complete their precharge, thereby placing the device in the all banks idle state.
8. Issue an AUTO REFRESH command.
9. Wait at least ^{t}RFC time, during which only NOPs or COMMAND INHIBIT commands are allowed.
10. Issue an AUTO REFRESH command.
11. Wait at least ^{t}RFC time, during which only NOPs or COMMAND INHIBIT commands are allowed.
12. The SDRAM is now ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded with desired bit values prior to applying any operational command. Using the LMR command, program the mode register. The mode register is programmed via the MODE REGISTER SET command with BA1 = 0, BA0 = 0 and retains the stored information until it is programmed again or the device loses power. Not programming the mode register upon initialization will result in default settings, which may not be desired. Outputs are guaranteed High-Z after the LMR command is issued. Outputs should be High-Z already before the LMR command is issued.
13. Wait at least ^{t}MRD time, during which only NOP or DESELECT commands are allowed.
14. Using the LMR command, program the extended mode register. The low-power extended mode register is programmed via the MODE REGISTER SET command with BA1 = 1, BA0 = 0 and retains the stored information until it is programmed again or the device loses power. Not programming the extended mode register upon initialization will result in default settings for the low-power features. The extended mode will default with the temperature sensor enabled, full drive strength, and full array refresh.
15. Wait at least ^{t}MRD time, during which only NOP or DESELECT commands are allowed.

At this point, the DRAM is ready for any valid command.

Note: If desired, more than two AUTO REFRESH commands can be issued in the sequence. After steps 9 and 10 are complete, repeat them until the desired number of AUTO REFRESH + ^{t}RFC loops is achieved.

Register Definition

Mode Register

To achieve low power consumption, there are two mode registers in the Mobile component: mode register and extended mode register. Mode register is discussed in this section. Extended mode register is discussed on page 21. The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of BL, a burst type, CL, an operating mode, and a write burst mode, as shown in Figure 7 on page 18. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify BL, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify CL, M7 and M8 specify the operating mode, M9 specify the write burst mode (single or programmed burst length), M10 and M11 are reserved and must be set to zero. To address the mode register, M12 and M13 must be set to zero.

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The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented, with BL being programmable, as shown in Figure 8 on page 20. BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential mode. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths. If a full page burst is not terminated at the end of the page, it could wrap to column zero and continue.

Reserved states cannot be used because unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A8 (x16) or A1–A7 (x32) when BL = 2; by A2–A8 (x16) or A2–A7 (x32) when BL = 4; and by A3–A8 (x16) or A3–A7 (x32) when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed either to be sequential or interleaved; this is referred to as the burst type and is selected via bit M3. Note only a sequential burst is allowed for full page bursts.

The ordering of accesses within a burst is determined by BL, the burst type, and the starting column address, as shown in Table 6 on page 19.

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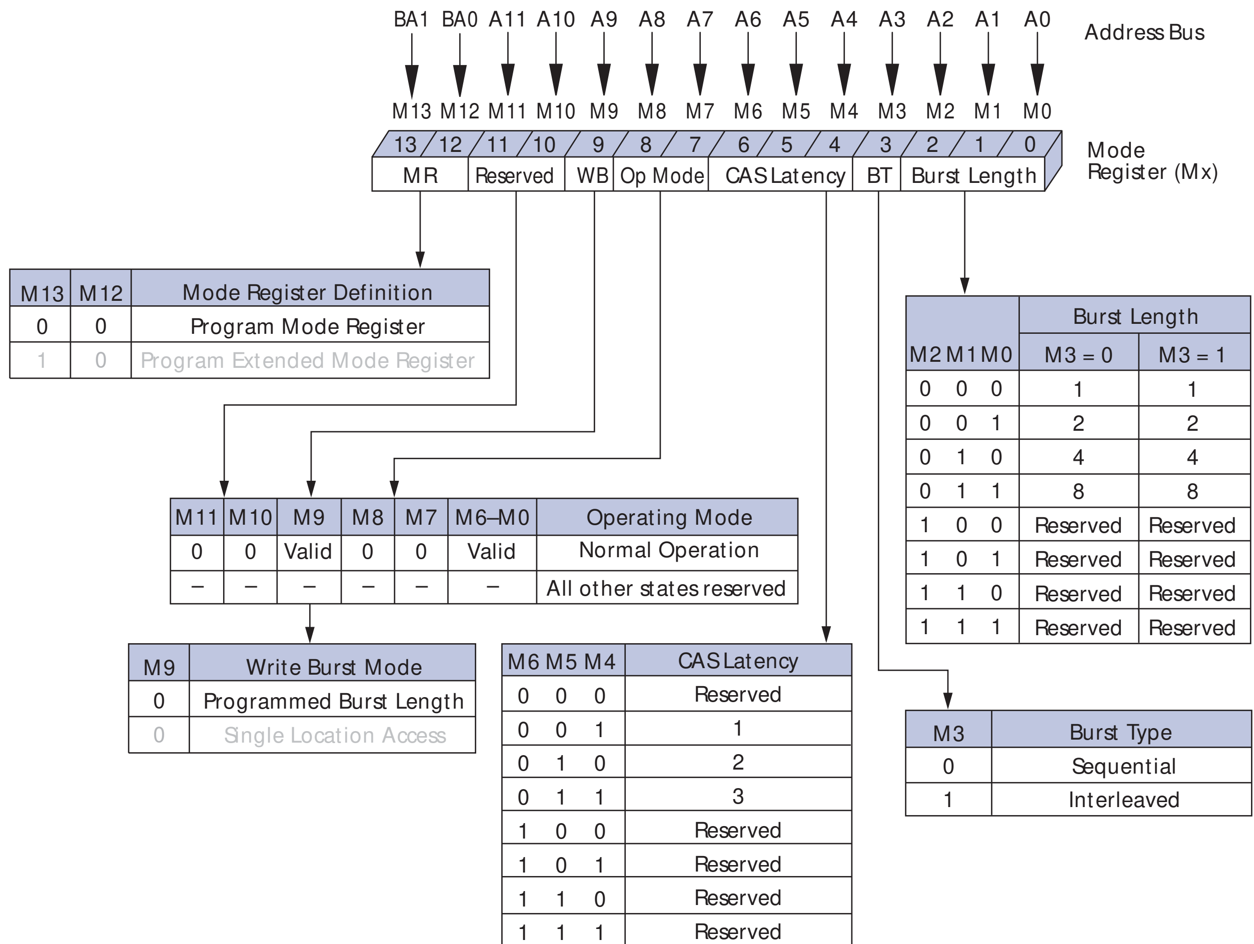
Figure 7: Mode Register Definition



M13	M12	Mode Register Definition
0	0	Program Mode Register
1	0	Program Extended Mode Register

M11	M10	M9	M8	M7	M6–M0	Operating Mode
0	0	Valid	0	0	Valid	Normal Operation
–	–	–	–	–	–	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
0	Single Location Access

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

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Table 6: Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			**A0**		
			0	0-1	0-1
			1	1-0	1-0
4		**A1**	**A0**		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	**A2**	**A1**	**A0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full page (y)	n = A0–A8 for x16, A0–A7 for x32 (location 0–y)			Cn, Cn + 1, Cn + 2, Cn + 3, Cn + 4..., ...Cn - 1, Cn...	Not supported

NOTE:

Notes:
1. For full-page accesses: y = 512 (x16), y = 256 (x32).
2. For BL = 2, A1–A8 (x16) or A1–A7 (x32) select the block-of-two burst; A0 selects the starting column within the block.
3. For BL = 4, A2–A8 (x16) or A2–A7 (x32) select the block-of-four burst; A0–A1 select the starting column within the block.
4. For BL = 8, A3–A8 (x16) or A3–A7 (x32) select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected, and A0–A8 (x16) or A0–A7 (x32) select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For BL = 1, A0–A8 (x16) or A0–A7 (x32) select the unique column to be accessed, and mode register bit M3 is ignored.

CAS Latency (CL)

CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 1, 2, or 3 clocks.

If a READ command is registered at clock edge n and the latency is m clocks, the data will be available by clock edge $n + m$. The DQ will start driving as a result of the clock edge one cycle earlier ($n + m - 1$), and provided that the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming that the clock cycle time is such that all relevant access times are met, if a read command is registered at T0 and the

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latency is programmed to 2 clocks, the DQ will start driving after T1, and the data will be valid by T2, as shown in Figure 8. Table 7 indicates the operating frequencies at which each CL setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 8: CAS Latency

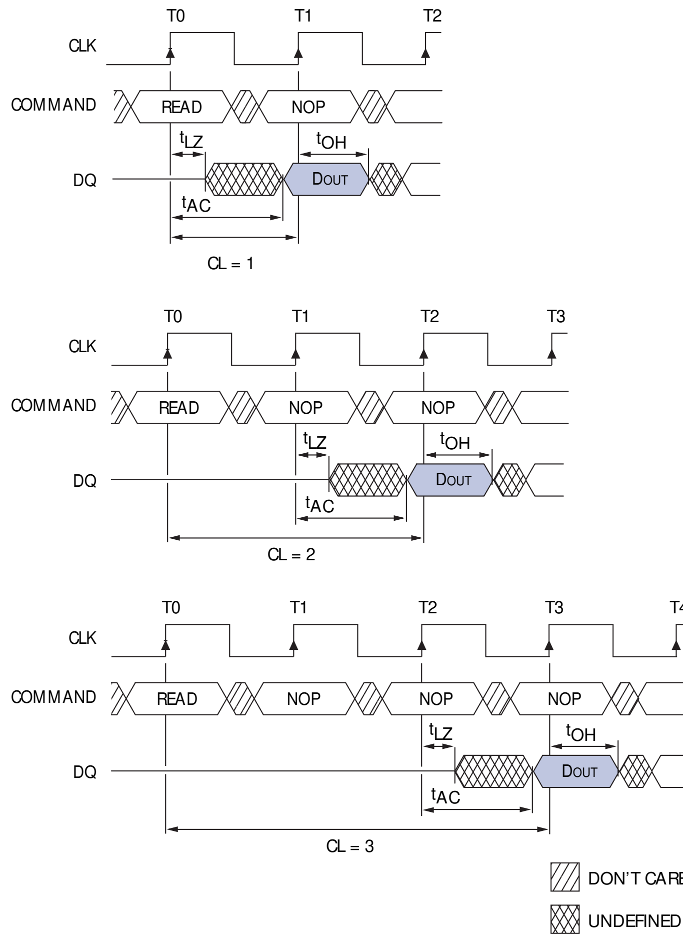

Table 7: CAS Latency

Speed	Allowable Operating Frequency (MHz)		
	CL = 1	CL = 2	CL = 3
-75M	–	≤ 100	≤ 133
-8	≤ 50	≤ 100	≤ 125
-10	≤ 40	≤ 83	≤ 100

Write Burst Mode

When M9 = 0, BL programmed into M0–M2 applies to both READ and WRITE burst. If M9 = 1, all WRITE bursts will only be single location access regardless of the BL setting in the mode register. READ burst lengths are unaffected by the state of M9.

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Operating Mode

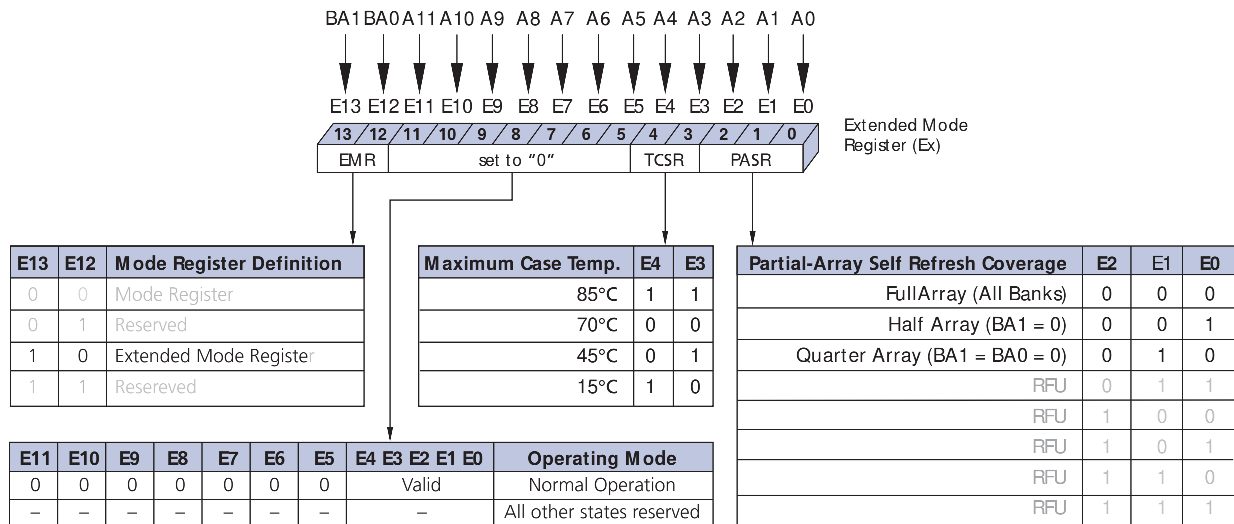
The normal operating mode is selected by setting M7, M8, M10, and M11 to zero; all the other combinations of values for M7, M8, M10, and M11 are reserved for future use and/ or test modes.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls the functions beyond those controlled by the mode register. These additional functions are special features of the Mobile device. They include TCSR and PASR.

Figure 9: Extended Mode Register



E13	E12	Mode Register Definition
0	0	Mode Register
0	1	Reserved
1	0	Extended Mode Register
1	1	Resereved

Maximum Case Temp.	E4	E3
85°C	1	1
70°C	0	0
45°C	0	1
15°C	1	0

Partial-Array Self Refresh Coverage	E2	E1	E0
FullArray (All Banks)	0	0	0
Half Array (BA1 = 0)	0	0	1
Quarter Array (BA1 = BA0 = 0)	0	1	0
RFU	0	1	1
RFU	1	0	0
RFU	1	0	1
RFU	1	1	0
RFU	1	1	1

E11	E10	E9	E8	E7	E6	E5	E4 E3 E2 E1 E0	Operating Mode
0	0	0	0	0	0	0	Valid	Normal Operation
–	–	–	–	–	–	–	–	All other states reserved

Notes:
1. E13 and E12 (BA1 and BA0) must be "1, 0" to select the extended mode register (vs. the base mode register).
2. RFU: reserved for future use.

The extended mode register is programmed via the MODE REGISTER SET command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

The extended mode register must be programmed with E5 through E11 set to "0." The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. The extended mode register must be programmed to ensure proper operation.

Temperature-Compensated Self Refresh (TCSR)

TCSR allows the controller to program the refresh interval during self refresh mode, according to the case temperature of the Mobile device. This allows great power savings during self refresh during most operating temperature ranges. Only during extreme temperatures would the controller have to select a higher TCSR level that will guarantee data during self refresh.

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Every cell in the DRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. Historically, during self refresh, the refresh rate has been set to accommodate the worst case, or highest temperature range, expected.

Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high because the refresh rate was set to accommodate the higher temperatures. Setting E4 and E3 allows the DRAM to accommodate more specific temperature regions during self refresh. There are four temperature settings, which will vary the self refresh current according to the selected temperature. This selectable refresh rate will save power when the DRAM is operating at normal temperatures.

Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the PASR feature allows the controller to select the amount of memory that will be refreshed during self refresh. The refresh options are all banks (banks 0, 1, 2, and 3); two banks (banks 0 and 1); and one bank (bank 0). WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during self refresh. It's important to note that data in banks 2 and 3 will be lost when the two-bank option is used. Data will be lost in banks 1, 2, and 3 when the one-bank option is used.

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Commands

Table 8 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

Table 8: Truth Table – Commands and DQM Operation
Note 1 applies to entire table

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	Addr	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/row	X	2
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/col	X	3
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/col	Valid	3
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	4
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	5, 6
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	7
Write enable/output enable	–	–	–	–	L	–	Active	8
Write inhibit/output High-Z	–	–	–	–	H	–	High-Z	8

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0–A11 provide row address, and BA0, BA1 determine which bank is made active.
3. A0–A8 (x16) or A0–A7 (x32) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
4. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are "Don't Care."
5. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
6. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
7. A0–A10 define the op-code written to the mode register. BA0–BA1 either select mode register or the extended mode register (BA0 = BA1 = 0 select the mode register, BA1 = 1, BA0 = 0 selects the extended mode register, all other combinations of BA0-BA1 are reserved).
8. Activates or deactivates the DQ during WRITEs (0-clock delay) and READs (2-clock delay). For x16, LDQM controls DQ0–DQ7, and UDQM controls DQ8–DQ15. For x32, DQM0 controls DQ0–DQ7, DQM1 controls DQ8–DQ15, DQM2 controls DQ16–23, and DQM3 controls DQ24–DQ31.

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected SDRAM to perform a NOP (RAS#, CAS#, and WE# are HIGH, and CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

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LOAD MODE REGISTER

The mode register is loaded via inputs A0–A11. Refer to "Mode Register Definition" on page 18. The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 (x16) or A0–A7 (x32) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 (x16) or A0–A7 (x32) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is

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automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode where auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual read or write command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in "Operation" on page 26.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet. The BURST TERMINATE command does not precharge the row; the row will remain open until a PRECHARGE command is issued.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP has been met after the PRECHARGE command as shown in the operation section.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. Regardless of device width, the 128Mb SDRAM requires 4,096 AUTO REFRESH cycles every 64ms (commercial and industrial) or 16ms (automotive). Providing a distributed AUTO REFRESH command every 15.625µs (commercial and industrial) or 3.906µs (automotive) will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RFC), once every 64ms (commercial and industrial) or 16ms (automotive).

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain LOW.

After self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. After CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of 2 clocks, regardless of clock frequency) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

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