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# CIO RLD RAM<sup>®</sup> 2

MT49H32M9 – 32 Meg x 9 x 8 Banks

MT49H16M18 – 16 Meg x 18 x 8 Banks

MT49H8M36 – 8 Meg x 36 x 8 Banks

## Features

- 533 MHz DDR operation (1.067 Gb/s/pin data rate)
- 38.4 Gb/s peak bandwidth (x36 at 533 MHz clock frequency)
- Organization
  - 32 Meg x 9, 16 Meg x 18, and 8 Meg x 36
- 8 internal banks for concurrent operation and maximum bandwidth
- Reduced cycle time (15ns at 533 MHz)
- Nonmultiplexed addresses (address multiplexing option available)
- SRAM-type interface
- Programmable READ latency (RL), row cycle time, and burst sequence length
- Balanced READ and WRITE latencies in order to optimize data bus utilization
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Differential input data clocks (DKx, DKx#)
- On-die DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32ms refresh (8K refresh for each bank; 64K refresh command must be issued in total each 32ms)
- 144-ball  $\mu$ BGA package
- HSTL I/O (1.5V or 1.8V nominal)
- 25–60 $\Omega$  matched impedance outputs
- 2.5V  $V_{EXT}$ , 1.8V  $V_{DD}$ , 1.5V or 1.8V  $V_{DDQ}$  I/O
- On-die termination (ODT)  $R_{TT}$

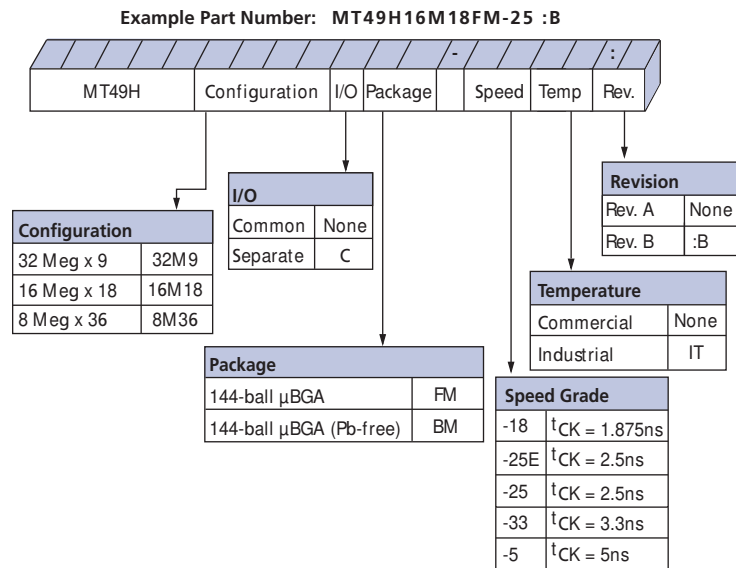
## Options<sup>1</sup>

- Clock cycle timing
  - 1.875ns @  $t_{RC} = 15ns$  -18
  - 2.5ns @  $t_{RC} = 15ns$  -25E
  - 2.5ns @  $t_{RC} = 20ns$  -25
  - 3.3ns @  $t_{RC} = 20ns$  -33
  - 5.0ns @  $t_{RC} = 20ns$  -5
- Configuration
  - 32 Meg x 9 32M9
  - 16 Meg x 18 16M18
  - 8 Meg x 36 8M36
- Operating temperature
  - Commercial (0° to +95°C) None
  - Industrial ( $T_C = -40^\circ C$  to +95°C;  $T_A = -40^\circ C$  to +85°C) IT
- Package
  - 144-ball  $\mu$ BGA FM
  - 144-ball  $\mu$ BGA (Pb-free) BM
- Revision :B

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on [www.micron.com](http://www.micron.com) for available offerings.

## Marking

Figure 1: 288Mb RLD RAM 2 CIO Part Numbers



## BGA Part Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. Micron's BGA Part Marking Decoder is available on Micron's Web site at [micron.com](http://micron.com).



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## General Description

The Micron<sup>®</sup> reduced latency DRAM (RLDRAM<sup>®</sup>) 2 is a high-speed memory device designed for high bandwidth data storage—telecommunications, networking, and cache applications, etc. The chip's 8-bank architecture is optimized for sustainable high speed operation.

The DDR I/O interface transfers two data words per clock cycle at the I/O balls. Output data is referenced to the free-running output data clock.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock(s).

Read and write accesses to the RLD RAM are burst-oriented. The burst length (BL) is programmable from 2, 4, or 8 by setting the mode register.

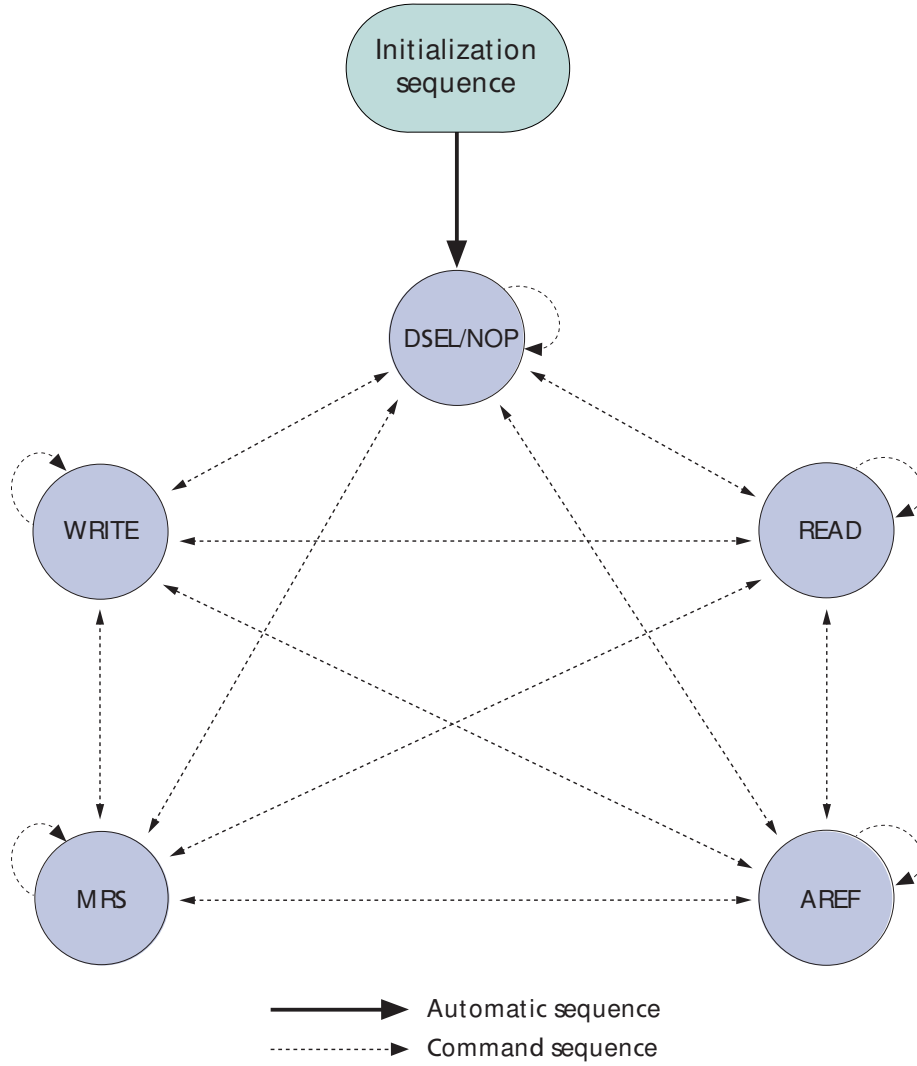
The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

Bank-scheduled refresh is supported with the row address generated internally.

The  $\mu$ BGA 144-ball package is used to enable ultra high-speed data transfer rates and a simple upgrade path from early generation devices.

## State Diagram

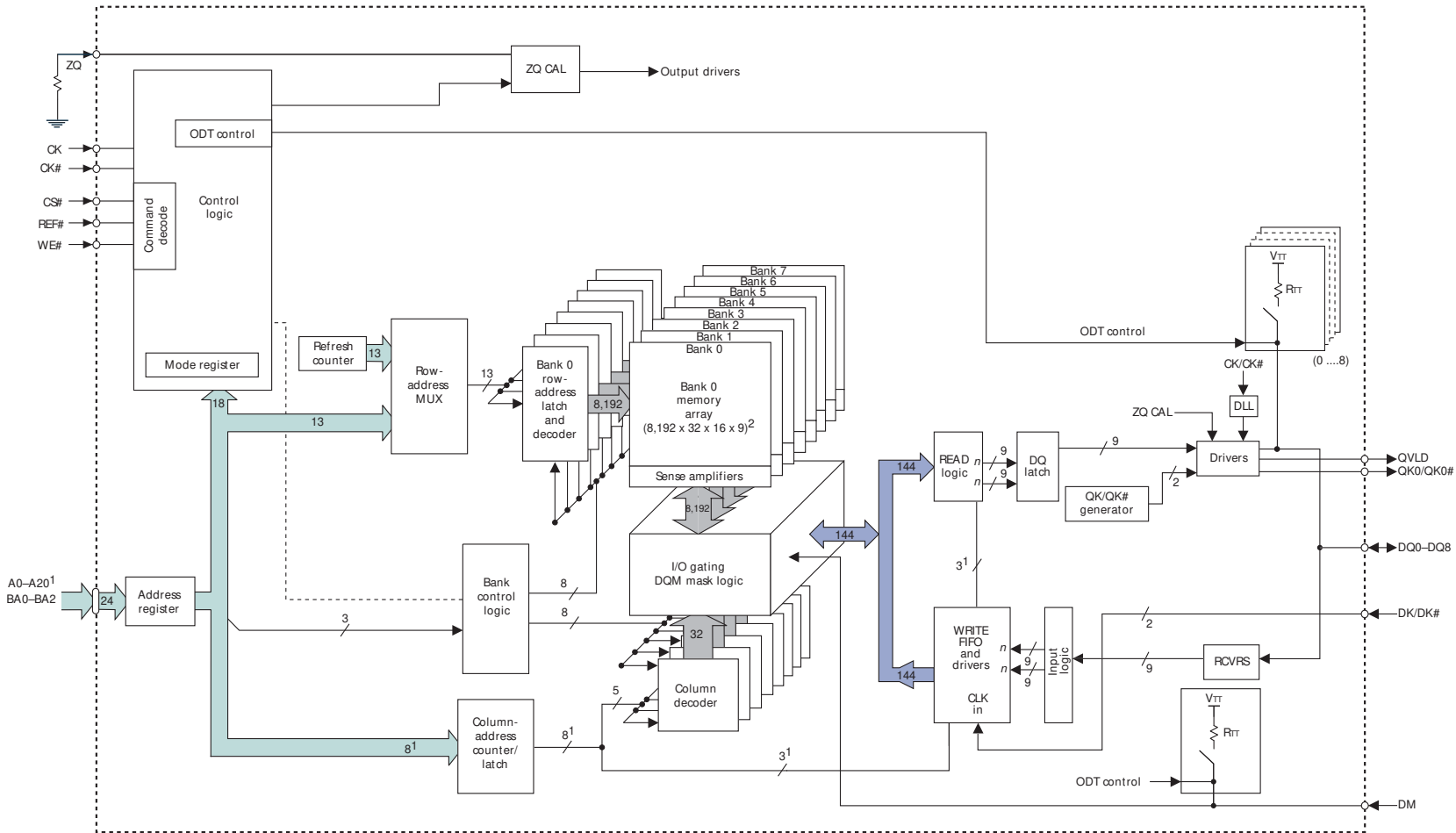
Figure 2: Simplified State Diagram





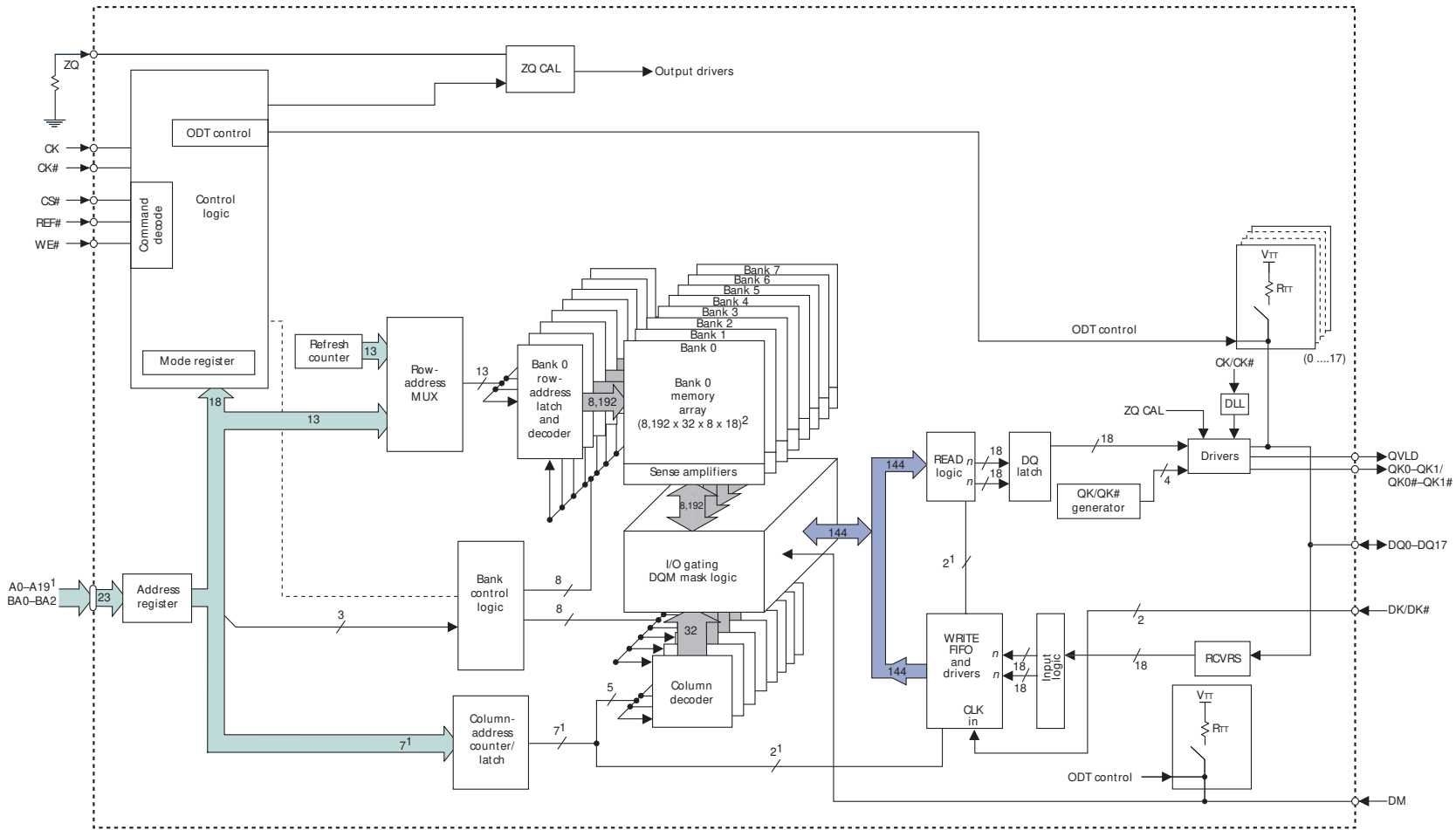
# Functional Block Diagrams

Figure 3: 32 Meg x 9 Functional Block Diagram



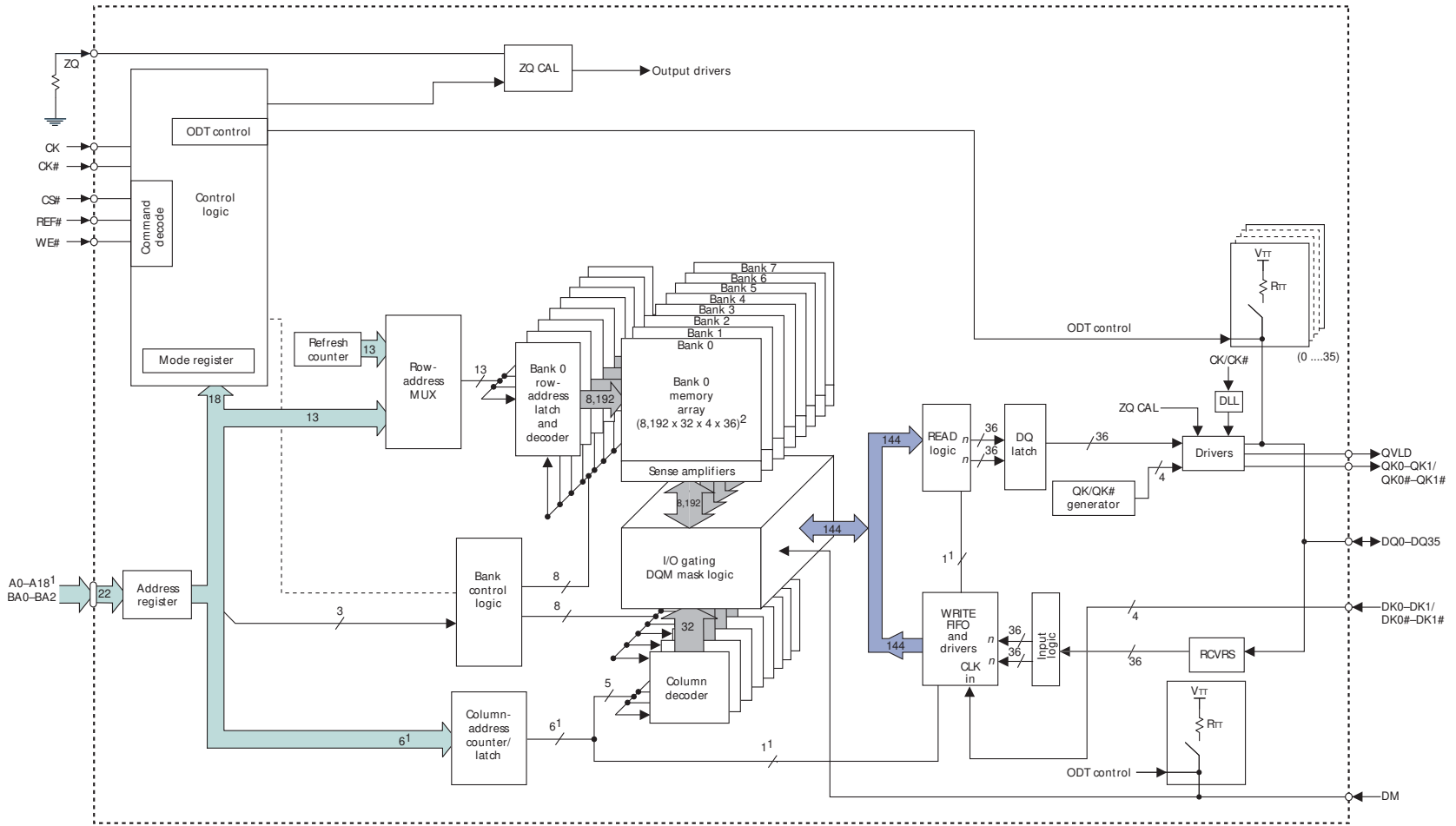
- Notes:
1. Examples for BL = 2; column address will be reduced with an increase in burst length.
  2. The "16" = (length of burst) x 2<sup>n</sup> (number of column addresses to WRITE FIFO and READ logic).

**Figure 4: 16 Meg x 18 Functional Block Diagram**



- Notes:
1. Examples for BL = 2; column address will be reduced with an increase in burst length.
  2. The "8" = (length of burst) x 2<sup>n</sup>(number of column addresses to WRITE FIFO and READ logic).

Figure 5: 8 Meg x 36 Functional Block Diagram



- Notes:
1. Examples for BL = 2; column address will be reduced with an increase in burst length.
  2. The "4" = (length of burst) x 2<sup>n</sup> (number of column addresses to WRITE FIFO and READ logic).



## Ball Assignments and Descriptions

Table 1: 32 Meg x 9 Ball Assignments (Top View) 144-Ball  $\mu$ BGA

	1	2	3	4	5	6	7	8	9	10	11	12
<b>A</b>	$V_{REF}$	$V_{SS}$	$V_{EXT}$	$V_{SS}$					$V_{SS}$	$V_{EXT}$	TMS	TCK
<b>B</b>	$V_{DD}$	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{SSQ}$					$V_{SSQ}$	DQ0	DNU <sup>4</sup>	$V_{DD}$
<b>C</b>	$V_{TT}$	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{DDQ}$					$V_{DDQ}$	DQ1	DNU <sup>4</sup>	$V_{TT}$
<b>D</b>	A22 <sup>1</sup>	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{SSQ}$					$V_{SSQ}$	QK0#	QK0	$V_{SS}$
<b>E</b>	A21 <sup>2</sup>	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{DDQ}$					$V_{DDQ}$	DQ2	DNU <sup>4</sup>	A20
<b>F</b>	A5	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{SSQ}$					$V_{SSQ}$	DQ3	DNU <sup>4</sup>	QVLD
<b>G</b>	A8	A6	A7	$V_{DD}$					$V_{DD}$	A2	A1	A0
<b>H</b>	B2	A9	$V_{SS}$	$V_{SS}$					$V_{SS}$	$V_{SS}$	A4	A3
<b>J</b>	NF <sup>3</sup>	NF <sup>3</sup>	$V_{DD}$	$V_{DD}$					$V_{DD}$	$V_{DD}$	B0	CK
<b>K</b>	DK	DK#	$V_{DD}$	$V_{DD}$					$V_{DD}$	$V_{DD}$	B1	CK#
<b>L</b>	REF#	CS#	$V_{SS}$	$V_{SS}$					$V_{SS}$	$V_{SS}$	A14	A13
<b>M</b>	WE#	A16	A17	$V_{DD}$					$V_{DD}$	A12	A11	A10
<b>N</b>	A18	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{SSQ}$					$V_{SSQ}$	DQ4	DNU <sup>4</sup>	A19
<b>P</b>	A15	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{DDQ}$					$V_{DDQ}$	DQ5	DNU <sup>4</sup>	DM
<b>R</b>	$V_{SS}$	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{SSQ}$					$V_{SSQ}$	DQ6	DNU <sup>4</sup>	$V_{SS}$
<b>T</b>	$V_{TT}$	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{DDQ}$					$V_{DDQ}$	DQ7	DNU <sup>4</sup>	$V_{TT}$
<b>U</b>	$V_{DD}$	DNU <sup>4</sup>	DNU <sup>4</sup>	$V_{SSQ}$					$V_{SSQ}$	DQ8	DNU <sup>4</sup>	$V_{DD}$
<b>V</b>	$V_{REF}$	ZQ	$V_{EXT}$	$V_{SS}$					$V_{SS}$	$V_{EXT}$	TDO	TDI

- Notes:
1. Reserved for future use. This signal is not connected.
  2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal.
  3. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to GND.
  4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND. Note that if ODT is enabled on Rev. A die, these pins will be connected to  $V_{TT}$ . The DNU pins are High-Z on Rev. B die when ODT is enabled.



Table 2: 16 Meg x 18 Ball Assignments (Top View) 144-Ball  $\mu$ BGA

	1	2	3	4	5	6	7	8	9	10	11	12
<b>A</b>	$V_{REF}$	$V_{SS}$	$V_{EXT}$	$V_{SS}$					$V_{SS}$	$V_{EXT}$	TMS	TCK
<b>B</b>	$V_{DD}$	DNU <sup>4</sup>	DQ4	$V_{SSQ}$					$V_{SSQ}$	DQ0	DNU <sup>4</sup>	$V_{DD}$
<b>C</b>	$V_{TT}$	DNU <sup>4</sup>	DQ5	$V_{DDQ}$					$V_{DDQ}$	DQ1	DNU <sup>4</sup>	$V_{TT}$
<b>D</b>	A22 <sup>1</sup>	DNU <sup>4</sup>	DQ6	$V_{SSQ}$					$V_{SSQ}$	QK0#	QK0	$V_{SS}$
<b>E</b>	A21 <sup>2</sup>	DNU <sup>4</sup>	DQ7	$V_{DDQ}$					$V_{DDQ}$	DQ2	DNU <sup>4</sup>	A20 <sup>2</sup>
<b>F</b>	A5	DNU <sup>4</sup>	DQ8	$V_{SSQ}$					$V_{SSQ}$	DQ3	DNU <sup>4</sup>	QVLD
<b>G</b>	A8	A6	A7	$V_{DD}$					$V_{DD}$	A2	A1	A0
<b>H</b>	B2	A9	$V_{SS}$	$V_{SS}$					$V_{SS}$	$V_{SS}$	A4	A3
<b>J</b>	NF <sup>3</sup>	NF <sup>3</sup>	$V_{DD}$	$V_{DD}$					$V_{DD}$	$V_{DD}$	B0	CK
<b>K</b>	DK	DK#	$V_{DD}$	$V_{DD}$					$V_{DD}$	$V_{DD}$	B1	CK#
<b>L</b>	REF#	CS#	$V_{SS}$	$V_{SS}$					$V_{SS}$	$V_{SS}$	A14	A13
<b>M</b>	WE#	A16	A17	$V_{DD}$					$V_{DD}$	A12	A11	A10
<b>N</b>	A18	DNU <sup>4</sup>	DQ14	$V_{SSQ}$					$V_{SSQ}$	DQ9	DNU <sup>4</sup>	A19
<b>P</b>	A15	DNU <sup>4</sup>	DQ15	$V_{DDQ}$					$V_{DDQ}$	DQ10	DNU <sup>4</sup>	DM
<b>R</b>	$V_{SS}$	QK1	QK1#	$V_{SSQ}$					$V_{SSQ}$	DQ11	DNU <sup>4</sup>	$V_{SS}$
<b>T</b>	$V_{TT}$	DNU <sup>4</sup>	DQ16	$V_{DDQ}$					$V_{DDQ}$	DQ12	DNU <sup>4</sup>	$V_{TT}$
<b>U</b>	$V_{DD}$	DNU <sup>4</sup>	DQ17	$V_{SSQ}$					$V_{SSQ}$	DQ13	DNU <sup>4</sup>	$V_{DD}$
<b>V</b>	$V_{REF}$	ZQ	$V_{EXT}$	$V_{SS}$					$V_{SS}$	$V_{EXT}$	TDO	TDI

- Notes:
1. Reserved for future use. This may optionally be connected to GND.
  2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.
  3. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to GND.
  4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND. Note that if ODT is enabled on Rev. A die, these pins will be connected to  $V_{TT}$ . The DNU pins are High-Z on Rev. B die when ODT is enabled.



Table 3: 8 Meg x 36 Ball Assignments (Top View) 144-Ball  $\mu$ BGA

	1	2	3	4	5	6	7	8	9	10	11	12
<b>A</b>	$V_{REF}$	$V_{SS}$	$V_{EXT}$	$V_{SS}$					$V_{SS}$	$V_{EXT}$	TMS	TCK
<b>B</b>	$V_{DD}$	DQ8	DQ9	$V_{SSQ}$					$V_{SSQ}$	DQ1	DQ0	$V_{DD}$
<b>C</b>	$V_{TT}$	DQ10	DQ11	$V_{DDQ}$					$V_{DDQ}$	DQ3	DQ2	$V_{TT}$
<b>D</b>	A22	DQ12	DQ13	$V_{SSQ}$					$V_{SSQ}$	QK0#	QK0	$V_{SS}$
<b>E</b>	A21 <sup>2</sup>	DQ14	DQ15	$V_{DDQ}$					$V_{DDQ}$	DQ5	DQ4	A20 <sup>2</sup>
<b>F</b>	A5	DQ16	DQ17	$V_{SSQ}$					$V_{SSQ}$	DQ7	DQ6	QVLD
<b>G</b>	A8	A6	A7	$V_{DD}$					$V_{DD}$	A2	A1	A0
<b>H</b>	B2	A9	$V_{SS}$	$V_{SS}$					$V_{SS}$	$V_{SS}$	A4	A3
<b>J</b>	DK0	DK0#	$V_{DD}$	$V_{DD}$					$V_{DD}$	$V_{DD}$	B0	CK
<b>K</b>	DK1	DK1#	$V_{DD}$	$V_{DD}$					$V_{DD}$	$V_{DD}$	B1	CK#
<b>L</b>	REF#	CS#	$V_{SS}$	$V_{SS}$					$V_{SS}$	$V_{SS}$	A14	A13
<b>M</b>	WE#	A16	A17	$V_{DD}$					$V_{DD}$	A12	A11	A10
<b>N</b>	A18	DQ24	DQ25	$V_{SSQ}$					$V_{SSQ}$	DQ35	DQ34	A19 <sup>2</sup>
<b>P</b>	A15	DQ22	DQ23	$V_{DDQ}$					$V_{DDQ}$	DQ33	DQ32	DM
<b>R</b>	$V_{SS}$	QK1	QK1#	$V_{SSQ}$					$V_{SSQ}$	DQ31	DQ30	$V_{SS}$
<b>T</b>	$V_{TT}$	DQ20	DQ21	$V_{DDQ}$					$V_{DDQ}$	DQ29	DQ28	$V_{TT}$
<b>U</b>	$V_{DD}$	DQ18	DQ19	$V_{SSQ}$					$V_{SSQ}$	DQ27	DQ26	$V_{DD}$
<b>V</b>	$V_{REF}$	ZQ	$V_{EXT}$	$V_{SS}$					$V_{SS}$	$V_{EXT}$	TDO	TDI

- Notes:
1. Reserved for future use. This may optionally be connected to GND.
  2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.

**Table 4: Ball Descriptions**

Symbol	Type	Description
A0–A20	Input	<b>Address inputs:</b> A0–A20 define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK.
BA0–BA2	Input	<b>Bank address inputs:</b> Select to which internal bank a command is being applied.
CK, CK#	Input	<b>Input clock:</b> CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	<b>Chip select:</b> CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
DK, DK#	Input	<b>Input data clock:</b> DK and DK# are the differential input data clocks. All input data is referenced to both edges of DK. DK# is ideally 180 degrees out of phase with DK. For the x36 device, DQ0–DQ17 are referenced to DK0 and DK0# and DQ18–DQ35 are referenced to DK1 and DK1#. For the x9 and x18 devices, all DQs are referenced to DK and DK#. All DKx and DKx# pins must always be supplied to the device.
DM	Input	<b>Input data mask:</b> The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM is sampled on both edges of DK (DK1 for the x36 configuration). Tie signal to ground if not used.
TCK	Input	<b>IEEE 1149.1 clock input:</b> This ball must be tied to V <sub>SS</sub> if the JTAG function is not used.
TMS, TDI	Input	<b>IEEE 1149.1 test inputs:</b> These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	<b>Command inputs:</b> Sampled at the positive edge of CK, WE# and REF# define (together with CS#) the command to be executed.
DQ0–DQ35	I/O	<b>Data input:</b> The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QKx. During WRITE commands, the data is sampled at both edges of DK.
ZQ	Reference	<b>External impedance (25–60Ω):</b> This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 × RQ, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode. Connecting ZQ to V <sub>DD</sub> invokes the maximum impedance mode. Refer to the Mode Register Definition in Nonmultiplexed Address Mode figure to activate this function.
QKx, QKx#	Output	<b>Output data clocks:</b> QKx and QKx# are opposite polarity, output data clocks. They are free-running, and during READs, are edge-aligned with data output from the RLDRAM. QKx# is ideally 180 degrees out of phase with QKx. For the x36 device, QK0 and QK0# are aligned with DQ0–DQ17, and QK1 and QK1# are aligned with DQ18–DQ35. For the x18 device, QK0 and QK0# are aligned with DQ0–DQ8, while QK1 and QK1# are aligned with Q9–Q17. For the x9 device, all DQs are aligned with QK0 and QK0#.
QVLD	Output	<b>Data valid:</b> The QVLD pin indicates valid output data. QVLD is edge-aligned with QKx and QKx#.
TDO	Output	<b>IEEE 1149.1 test output:</b> JTAG output. This ball may be left as no connect if the JTAG function is not used.
V <sub>DD</sub>	Supply	<b>Power supply:</b> Nominally, 1.8V. See Table 8 on page 20 for range.
V <sub>DDQ</sub>	Supply	<b>DQ power supply:</b> Nominally, 1.5V or 1.8V. Isolated on the device for improved noise immunity. See Table 8 on page 20 for range.
V <sub>EXT</sub>	Supply	<b>Power supply:</b> Nominally, 2.5V. See Table 8 on page 20 for range.
V <sub>REF</sub>	Supply	<b>Input reference voltage:</b> Nominally V <sub>DDQ</sub> /2. Provides a reference voltage for the input buffers.
V <sub>SS</sub>	Supply	Ground.
V <sub>SSQ</sub>	Supply	<b>DQ ground:</b> Isolated on the device for improved noise immunity.
V <sub>TT</sub>	Supply	<b>Power supply:</b> Isolated termination supply. Nominally, V <sub>DDQ</sub> /2. See Table 8 on page 20 for range.
A21	–	<b>Reserved for future use:</b> This signal is internally connected and can be treated as an address input.
A22	–	<b>Reserved for future use:</b> This signal is not connected and can be connected to ground.



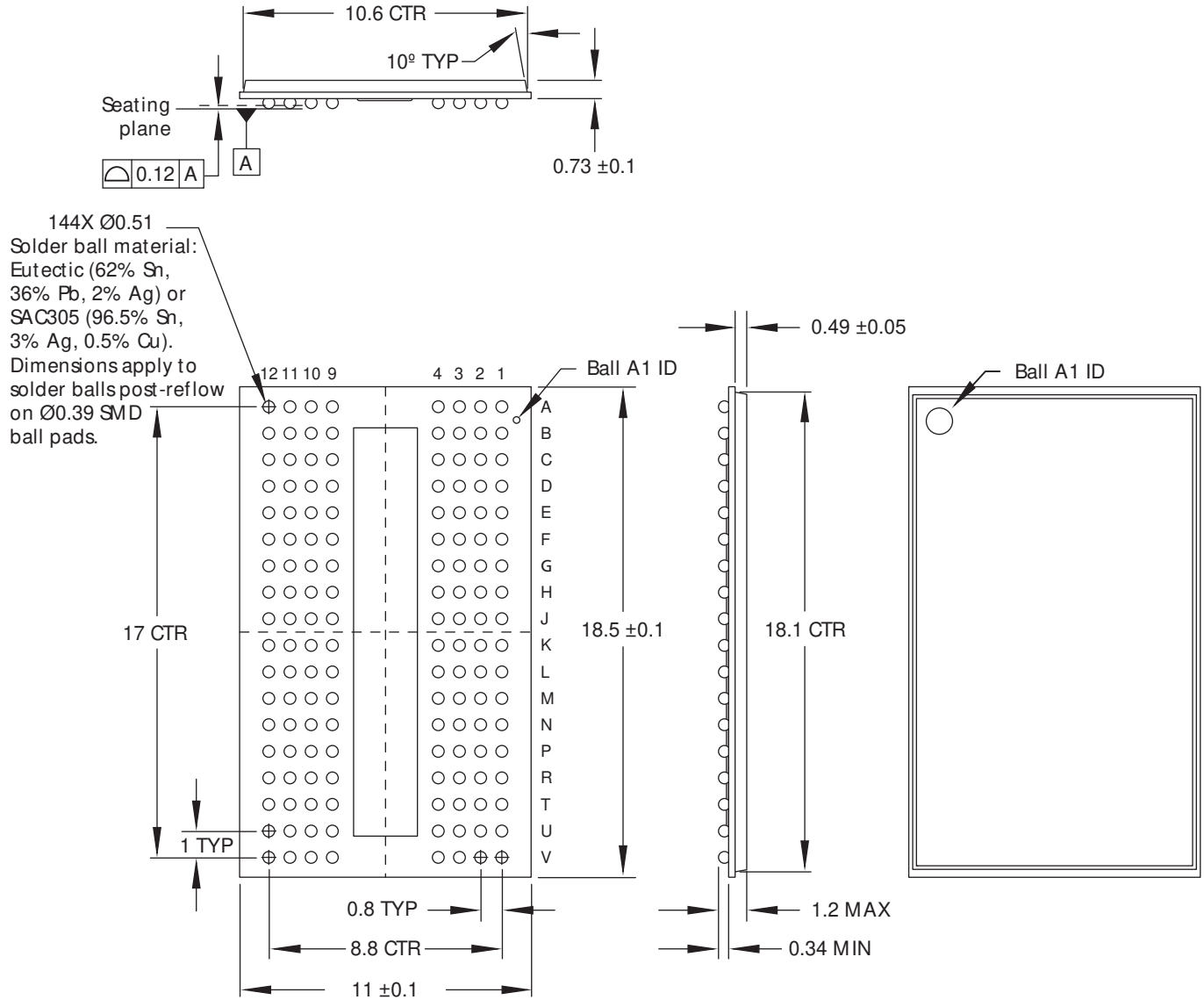
Table 4: Ball Descriptions (continued)

Symbol	Type	Description
DNU	–	<b>Do not use:</b> These balls may be connected to ground. Note that if ODT is enabled on Rev. A die, these pins will be connected to $V_{TT}$ . The DNU pins are High-Z on Rev. B die when ODT is enabled.
NF	–	<b>No function:</b> These balls can be connected to ground.



## Package Dimensions

Figure 6: 144-Ball  $\mu$ BGA



Notes: 1. All dimensions are in millimeters.



## Electrical Specifications – $I_{DD}$

**Table 5:  $I_{DD}$  Operating Conditions and Maximum Limits – Rev. A**

Notes appear on page 19

Description	Condition	Symbol	-25	-33	-5	Units
Standby current	tCK = idle; All banks idle; No inputs toggling	$I_{SB1}(V_{DD})$ x9/x18	48	48	48	mA
		$I_{SB1}(V_{DD})$ x36	48	48	48	
		$I_{SB1}(V_{EXT})$	26	26	26	
Active standby current	CS# = 1; No commands; Bank address incremented and half address/data change once every 4 clock cycles	$I_{SB2}(V_{DD})$ x9/x18	288	233	189	mA
		$I_{SB2}(V_{DD})$ x36	288	233	189	
		$I_{SB2}(V_{EXT})$	26	26	26	
Operational current	BL = 2; Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by write sequence; continuous data during WRITE commands	$I_{DD1}(V_{DD})$ x9/x18	348	305	255	mA
		$I_{DD1}(V_{DD})$ x36	374	343	292	
		$I_{DD1}(V_{EXT})$	41	36	36	
Operational current	BL = 4; Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by write sequence; Continuous data during WRITE commands	$I_{DD2}(V_{DD})$ x9/x18	362	319	269	mA
		$I_{DD2}(V_{DD})$ x36	418	389	339	
		$I_{DD2}(V_{EXT})$	48	42	42	
Operational current	BL = 8; Sequential bank access; Bank transitions once every tRC; half address transitions once every tRC; Read followed by write sequence; continuous data during WRITE commands	$I_{DD3}(V_{DD})$ x9/x18	408	368	286	mA
		$I_{DD3}(V_{DD})$ x36	n/a	n/a	n/a	
		$I_{DD3}(V_{EXT})$	55	48	48	
Burst refresh current	Eight-bank cyclic refresh; Continuous address/data; Command bus remains in refresh for all eight banks	$I_{REF1}(V_{DD})$ x9/x18	785	615	430	mA
		$I_{REF1}(V_{DD})$ x36	785	615	430	
		$I_{REF1}(V_{EXT})$	133	111	105	
Distributed refresh current	Single-bank refresh; Sequential bank access; Half address transitions once every tRC, continuous data	$I_{REF2}(V_{DD})$ x9/x18	325	267	221	mA
		$I_{REF2}(V_{DD})$ x36	326	281	227	
		$I_{REF2}(V_{EXT})$	48	42	42	
Operating burst write current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; measurement is taken during continuous WRITE	$I_{DD2W}(V_{DD})$ x9/x18	970	819	597	mA
		$I_{DD2W}(V_{DD})$ x36	990	914	676	
		$I_{DD2W}(V_{EXT})$	100	90	69	
Operating burst write current example	BL = 4; Cyclic bank access; Half of address bits change every 2 clock cycles; Continuous data; Measurement is taken during continuous WRITE	$I_{DD4W}(V_{DD})$ x9/x18	779	609	439	mA
		$I_{DD4W}(V_{DD})$ x36	882	790	567	
		$I_{DD4W}(V_{EXT})$	88	77	63	
Operating burst write current example	BL = 8; Cyclic bank access; Half of address bits change every 4 clock cycles; continuous data; Measurement is taken during continuous WRITE	$I_{DD8W}(V_{DD})$ x9/x18	668	525	364	mA
		$I_{DD8W}(V_{DD})$ x36	n/a	n/a	n/a	
		$I_{DD8W}(V_{EXT})$	60	51	40	
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Measurement is taken during continuous READ	$I_{DD2R}(V_{DD})$ x9/x18	860	735	525	mA
		$I_{DD2R}(V_{DD})$ x36	880	795	565	
		$I_{DD2R}(V_{EXT})$	100	90	69	
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every 2 clock cycles; Measurement is taken during continuous READ	$I_{DD4R}(V_{DD})$ x9/x18	680	525	380	mA
		$I_{DD4R}(V_{DD})$ x36	730	660	455	
		$I_{DD4R}(V_{EXT})$	88	77	63	



**Table 5:  $I_{DD}$  Operating Conditions and Maximum Limits – Rev. A**

Notes appear on page 19

Description	Condition	Symbol	-25	-33	-5	Units
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every 4 clock cycles; Measurement is taken during continuous READ	$I_{DD8R}(V_{DD})$ x9/x18	570	450	310	mA
		$I_{DD8R}(V_{DD})$ x36	n/a	n/a	n/a	
		$I_{DD8R}(V_{EXT})$	60	51	40	

**Table 6:  $I_{DD}$  Operating Conditions and Maximum Limits – Rev. B**

Notes appear on page 19

Description	Condition	Symbol	-18	-25E	-25	-33	Units
Standby current	$t_{CK}$ = idle; All banks idle; No inputs toggling	$I_{SB1}(V_{DD})$ x9/x18	55	55	55	55	mA
		$I_{SB1}(V_{DD})$ x36	55	55	55	55	
		$I_{SB1}(V_{EXT})$	5	5	5	5	
Active standby current	CS# = 1; No commands; Bank address incremented and half address/data change once every 4 clock cycles	$I_{SB2}(V_{DD})$ x9/x18	250	215	215	190	mA
		$I_{SB2}(V_{DD})$ x36	250	215	215	190	
		$I_{SB2}(V_{EXT})$	5	5	5	5	
Operational current	BL = 2; Sequential bank access; Bank transitions once every $t_{RC}$ ; Half address transitions once every $t_{RC}$ ; Read followed by write sequence; continuous data during WRITE commands	$I_{DD1}(V_{DD})$ x9/x18	310	285	260	225	mA
		$I_{DD1}(V_{DD})$ x36	320	295	270	230	
		$I_{DD1}(V_{EXT})$	10	10	10	10	
Operational current	BL = 4; Sequential bank access; Bank transitions once every $t_{RC}$ ; Half address transitions once every $t_{RC}$ ; Read followed by write sequence; Continuous data during WRITE commands	$I_{DD2}(V_{DD})$ x9/x18	315	290	260	220	mA
		$I_{DD2}(V_{DD})$ x36	330	305	275	230	
		$I_{DD2}(V_{EXT})$	10	10	10	10	
Operational current	BL = 8; Sequential bank access; Bank transitions once every $t_{RC}$ ; half address transitions once every $t_{RC}$ ; Read followed by write sequence; continuous data during WRITE commands	$I_{DD3}(V_{DD})$ x9/x18	330	305	275	230	mA
		$I_{DD3}(V_{DD})$ x36	390	365	320	265	
		$I_{DD3}(V_{EXT})$	15	15	15	15	
Burst refresh current	Eight-bank cyclic refresh; Continuous address/data; Command bus remains in refresh for all eight banks	$I_{REF1}(V_{DD})$ x9/x18	660	540	530	430	mA
		$I_{REF1}(V_{DD})$ x36	670	545	535	435	
		$I_{REF1}(V_{EXT})$	45	30	30	25	
Distributed refresh current	Single-bank refresh; Sequential bank access; Half address transitions once every $t_{RC}$ , continuous data	$I_{REF2}(V_{DD})$ x9/x18	295	265	250	215	mA
		$I_{REF2}(V_{DD})$ x36	295	265	250	215	
		$I_{REF2}(V_{EXT})$	10	10	10	10	
Operating burst write current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; measurement is taken during continuous WRITE	$I_{DD2W}(V_{DD})$ x9/x18	830	655	655	530	mA
		$I_{DD2W}(V_{DD})$ x36	885	700	700	565	
		$I_{DD2W}(V_{EXT})$	40	35	35	30	
Operating burst write current example	BL = 4; Cyclic bank access; Half of address bits change every 2 clock cycles; Continuous data; Measurement is taken during continuous WRITE	$I_{DD4W}(V_{DD})$ x9/x18	580	465	465	385	mA
		$I_{DD4W}(V_{DD})$ x36	635	510	510	420	
		$I_{DD4W}(V_{EXT})$	25	20	20	20	
Operating burst write current example	BL = 8; Cyclic bank access; Half of address bits change every 4 clock cycles; continuous data; Measurement is taken during continuous WRITE	$I_{DD8W}(V_{DD})$ x9/x18	445	370	370	305	mA
		$I_{DD8W}(V_{DD})$ x36	560	455	455	375	
		$I_{DD8W}(V_{EXT})$	25	20	20	20	

**Table 6:  $I_{DD}$  Operating Conditions and Maximum Limits – Rev. B (continued)**

Notes appear on page 19

Description	Condition	Symbol	-18	-25E	-25	-33	Units
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Measurement is taken during continuous READ	$I_{DD2R}(V_{DD})$ x9/x18	805	640	640	515	mA
		$I_{DD2R}(V_{DD})$ x36	850	675	675	540	
		$I_{DD2R}(V_{EXT})$	40	35	35	30	
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every 2 clock cycles; Measurement is taken during continuous READ	$I_{DD4R}(V_{DD})$ x9/x18	545	440	440	365	mA
		$I_{DD4R}(V_{DD})$ x36	590	475	475	390	
		$I_{DD4R}(V_{EXT})$	25	20	20	20	
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every 4 clock cycles; Measurement is taken during continuous READ	$I_{DD8R}(V_{DD})$ x9/x18	410	335	335	280	mA
		$I_{DD8R}(V_{DD})$ x36	525	425	425	350	
		$I_{DD8R}(V_{EXT})$	25	20	20	20	

- Notes:
- $I_{DD}$  specifications are tested after the device is properly initialized.  $+0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.7\text{V} \leq V_{DD} \leq +1.9\text{V}$ ,  $+2.38\text{V} \leq V_{EXT} \leq +2.63\text{V}$ ,  $+1.4\text{V} \leq V_{DDQ} \leq V_{DD}$ ,  $V_{REF} = V_{DDQ}/2$ .
  - $t_{CK} = t_{DK} = \text{MIN}$ ,  $t_{RC} = \text{MIN}$ .
  - Input slew rate is specified in Table 9 on page 21.
  - Definitions for  $I_{DD}$  conditions:
    - LOW is defined as  $V_{IN} \leq V_{IL(AC)}$  MAX.
    - HIGH is defined as  $V_{IN} \geq V_{IH(AC)}$  MIN.
    - Stable is defined as inputs remaining at a HIGH or LOW level.
    - Floating is defined as inputs at  $V_{REF} = V_{DDQ}/2$ .
    - Continuous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
    - Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
    - Sequential bank access is defined as the bank address incrementing by one every  $t_{RC}$ .
    - Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
  - CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
  - $I_{DD}$  parameters are specified with ODT disabled.
  - Tests for AC timing,  $I_{DD}$ , and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
  - $I_{DD}$  tests may use a  $V_{IL}$ -to- $V_{IH}$  swing of up to 1.5V in the test environment, but input timing is still referenced to  $V_{REF}$  (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between  $V_{IL(AC)}$  and  $V_{IH(AC)}$ .

## Electrical Specifications – AC and DC

### Absolute Maximum Ratings

Stresses greater than those listed in Table 7 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 7: Absolute Maximum Ratings**

Parameter	Min	Max	Units
I/O voltage	-0.3	$V_{DDQ} + 0.3$	V
Voltage on $V_{EXT}$ supply relative to $V_{SS}$	-0.3	+2.8	V
Voltage on $V_{DD}$ supply relative to $V_{SS}$	-0.3	+2.1	V
Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	-0.3	+2.1	V

### AC and DC Operating Conditions

**Table 8: DC Electrical Characteristics and Operating Conditions**

Note 1 applies to the entire table; Unless otherwise noted:  $+0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.7\text{V} \leq V_{DD} \leq +1.9\text{V}$

Description	Conditions	Symbol	Min	Max	Units	Notes
Supply voltage	–	$V_{EXT}$	2.38	2.63	V	
Supply voltage	–	$V_{DD}$	1.7	1.9	V	2
Isolated output buffer supply	–	$V_{DDQ}$	1.4	$V_{DD}$	V	2, 3
Reference voltage	–	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	4, 5, 6
Termination voltage	–	$V_{TT}$	$0.95 \times V_{REF}$	$1.05 \times V_{REF}$	V	7, 8
Input high (logic 1) voltage	–	$V_{IH}$	$V_{REF} + 0.1$	$V_{DDQ} + 0.3$	V	2
Input low (logic 0) voltage	–	$V_{IL}$	$V_{SSQ} - 0.3$	$V_{REF} - 0.1$	V	2
Output high current	$V_{OH} = V_{DDQ}/2$	$I_{OH}$	$(V_{DDQ}/2)/(1.15 \times RQ/5)$	$(V_{DDQ}/2)/(0.85 \times RQ/5)$	A	9, 10, 11
Output low current	$V_{OL} = V_{DDQ}/2$	$I_{OL}$	$(V_{DDQ}/2)/(1.15 \times RQ/5)$	$(V_{DDQ}/2)/(0.85 \times RQ/5)$	A	9, 10, 11
Clock input leakage current	$0\text{V} \leq V_{IN} \leq V_{DD}$	$I_{LC}$	-5	5	$\mu\text{A}$	
Input leakage current	$0\text{V} \leq V_{IN} \leq V_{DD}$	$I_{LI}$	-5	5	$\mu\text{A}$	
Output leakage current	$0\text{V} \leq V_{IN} \leq V_{DDQ}$	$I_{LO}$	-5	5	$\mu\text{A}$	
Reference voltage current	–	$I_{REF}$	-5	5	$\mu\text{A}$	

- Notes:
- All voltages referenced to  $V_{SS}$  (GND).
  - Overshoot:  $V_{IH(AC)} \leq V_{DD} + 0.7\text{V}$  for  $t \leq t_{CK}/2$ . Undershoot:  $V_{IL(AC)} \geq -0.5\text{V}$  for  $t \leq t_{CK}/2$ . During normal operation,  $V_{DDQ}$  must not exceed  $V_{DD}$ . Control input signals may not have pulse widths less than  $t_{CK}/2$  or operate at frequencies exceeding  $t_{CK}$  (MAX).
  - $V_{DDQ}$  can be set to a nominal  $1.5\text{V} \pm 0.1\text{V}$  or  $1.8\text{V} \pm 0.1\text{V}$  supply.
  - Typically the value of  $V_{REF}$  is expected to be  $0.5 \times V_{DDQ}$  of the transmitting device.  $V_{REF}$  is expected to track variations in  $V_{DDQ}$ .
  - Peak-to-peak AC noise on  $V_{REF}$  must not exceed  $\pm 2\% V_{REF(DC)}$ .
  - $V_{REF}$  is expected to equal  $V_{DDQ}/2$  of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on  $V_{REF}$  may not exceed  $\pm 2\%$  of the DC value. Thus, from  $V_{DDQ}/2$ ,  $V_{REF}$  is allowed  $\pm 2\% V_{DDQ}/2$  for DC error and an additional  $\pm 2\% V_{DDQ}/2$  for AC noise. This measurement is to be taken at the nearest  $V_{REF}$  bypass capacitor.

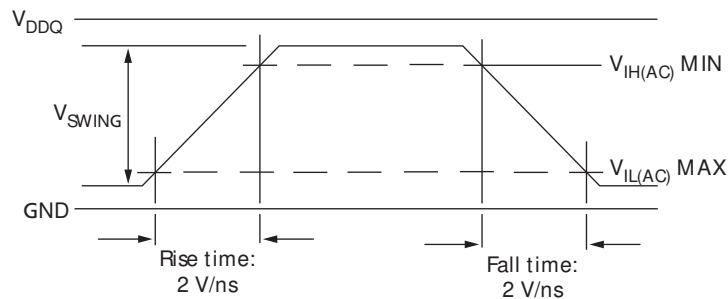
7.  $V_{TT}$  is expected to be set equal to  $V_{REF}$  and must track variations in the DC level of  $V_{REF}$ .
8. On-die termination may be selected using mode register bit 9 (see the Mode Register Definition in Nonmultiplexed Address Mode figure). A resistance  $R_{TT}$  from each data input signal to the nearest  $V_{TT}$  can be enabled.  
 $R_{TT} = 125\text{--}185\Omega$  at  $95^\circ\text{C } T_C$ .
9.  $I_{OH}$  and  $I_{OL}$  are defined as absolute values and are measured at  $V_{DDQ}/2$ .  $I_{OH}$  flows from the device,  $I_{OL}$  flows into the device.
10. If MRSbit A8 is 0, use  $R_Q = 250\Omega$  in the equation in lieu of presence of an external impedance matched resistor.
11. For  $V_{OL}$  and  $V_{OH}$ , refer to the RLDRAM 2 HSPICE or IBIS driver models.

**Table 9: Input AC Logic Levels**

Notes 1–3 apply to entire table; Unless otherwise noted:  $+0^\circ\text{C} \leq T_C \leq +95^\circ\text{C}$ ;  $+1.7\text{V} \leq V_{DD} \leq +1.9\text{V}$

Description	Symbol	Min	Max	Units
Input high (logic 1) voltage	$V_{IH}$	$V_{REF} + 0.2$	–	V
Input low (logic 0) voltage	$V_{IL}$	–	$V_{REF} - 0.2$	V

- Notes:
1. All voltages referenced to  $V_{SS}$  (GND).
  2. The AC and DC input level specifications are as defined in the HSTL standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
  3. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between  $V_{IL(AC)}$  and  $V_{IH(AC)}$ . See illustration below:



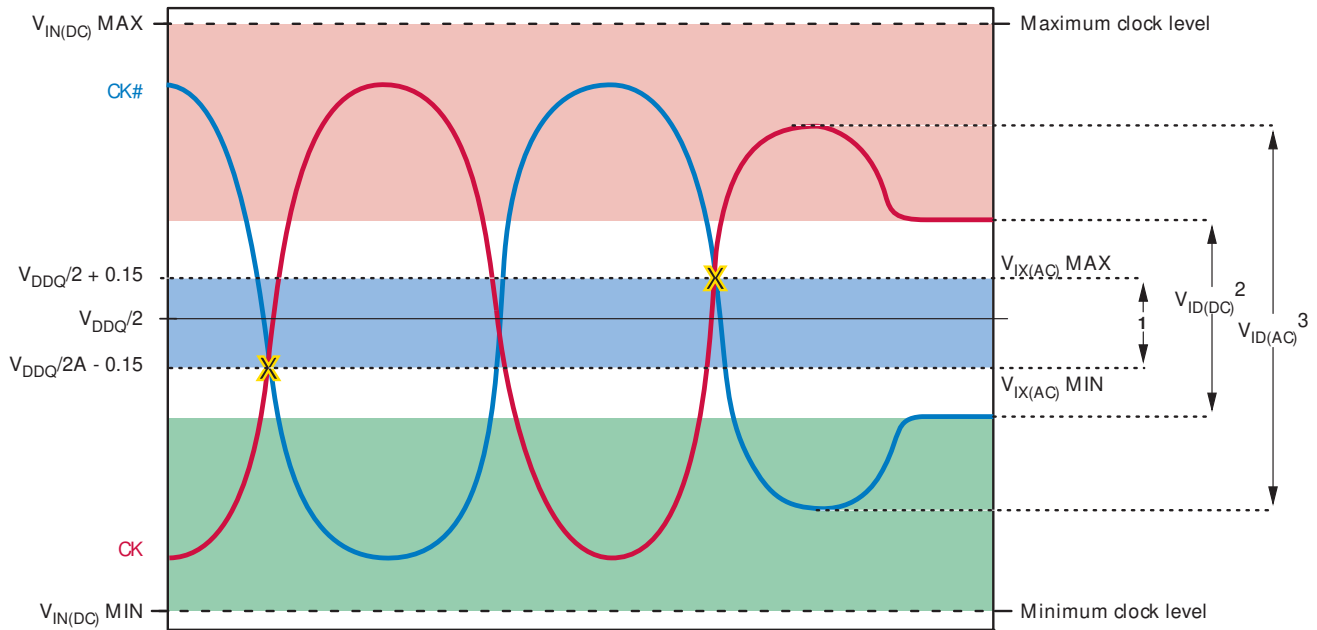
**Table 10: Differential Input Clock Operating Conditions**

Notes 1–4 apply to the entire table; Unless otherwise noted:  $+0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ ;  $+1.7\text{V} \leq V_{DD} \leq +1.9\text{V}$

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input voltage level: CK and CK#	$V_{IN(DC)}$	-0.3	$V_{DDQ} + 0.3$	V	
Clock input differential voltage: CK and CK#	$V_{ID(DC)}$	0.2	$V_{DDQ} + 0.6$	V	5
Clock input differential voltage: CK and CK#	$V_{ID(AC)}$	0.4	$V_{DDQ} + 0.6$	V	5
Clock input crossing point voltage: CK and CK#	$V_{IX(AC)}$	$V_{DDQ}/2 - 0.15$	$V_{DDQ}/2 + 0.15$	V	6

- Notes:
1. DKx and DKx# have the same requirements as CK and CK#.
  2. All voltages referenced to  $V_{SS}$  (GND).
  3. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is  $V_{REF}$ .
  4. CK and CK# input slew rate must be  $\geq 2$  V/ns ( $\geq 4$  V/ns if measured differentially).
  5.  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on CK#.
  6. The value of  $V_{IX}$  is expected to equal  $V_{DDQ}/2$  of the transmitting device and must track variations in the DC level of the same.

**Figure 7: Clock Input**



- Notes:
1. CK and CK# must cross within this region.
  2. CK and CK# must meet at least  $V_{ID(DC)}$  MIN when static and centered around  $V_{DDQ}/2$ .
  3. Minimum peak-to-peak swing.
  4. It is a violation to tristate CK and CK# after the part is initialized.

## Input Slew Rate Derating

Table 11 on page 24 and Table 12 on page 25 define the address, command, and data setup and hold derating values. These values are added to the default  $t_{AS}/t_{CS}/t_{DS}$  and  $t_{AH}/t_{CH}/t_{DH}$  specifications when the slew rate of any of these input signals is less than the  $2 V/ns$  the nominal setup and hold specifications are based upon.

To determine the setup and hold time needed for a given slew rate, add the  $t_{AS}/t_{CS}$  default specification to the “ $t_{AS}/t_{CS} V_{REF}$  to CK/CK# Crossing” and the  $t_{AH}/t_{CH}$  default specification to the “ $t_{AH}/t_{CH}$  CK/CK# Crossing to  $V_{REF}$ ” derated values on Table 11. The derated data setup and hold values can be determined in a like manner using the “ $t_{DS} V_{REF}$  to CK/CK# Crossing” and “ $t_{DH}$  to CK/CK# Crossing to  $V_{REF}$ ” values on Table 12. The derating values on Table 11 and Table 12 apply to all speed grades.

The setup times on Table 11 and Table 12 represent a rising signal. In this case, the time from which the rising signal crosses  $V_{IH(AC)}$  MIN to the CK/CK# cross point is static and must be maintained across all slew rates. The derated setup timing represents the point at which the rising signal crosses  $V_{REF(DC)}$  to the CK/CK# cross point. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between  $V_{IH(AC)}$  MIN and the CK/CK# cross point. The setup values in Table 11 and Table 12 are also valid for falling signals (with respect to  $V_{IL[AC]}$  MAX and the CK/CK# cross point).

The hold times in Table 11 and Table 12 represent falling signals. In this case, the time from the CK/CK# cross point to when the signal crosses  $V_{IH(DC)}$  MIN is static and must be maintained across all slew rates. The derated hold timing represents the delta between the CK/CK# cross point to when the falling signal crosses  $V_{REF(DC)}$ . This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between the CK/CK# cross point and  $V_{IH(DC)}$ . The hold values in Table 11 and Table 12 are also valid for rising signals (with respect to  $V_{IL[DC]}$  MAX and the CK and CK# cross point).

**Note:** The above descriptions also pertain to data setup and hold derating when CK/CK# are replaced with DK/DK#.





Table 11: Address and Command Setup and Hold Derating Values

Command/ Address Slew Rate (V/ns)	$t_{AS}^{\dagger}/t_{CS}^{\dagger} V_{REF}$ to CK/CK# Crossing	$t_{AS}^{\dagger}/t_{CS}^{\dagger} V_{IH(AC)}$ MIN to CK/CK# Crossing	$t_{AH}^{\dagger}/t_{CH}^{\dagger}$ CK/CK# Crossing to $V_{REF}$	$t_{AH}^{\dagger}/t_{CH}^{\dagger}$ CK/CK# Crossing to $V_{IH(DC)}$ MIN	Units
CK, CK# Differential Sew Rate: 2.0 V/ns					
2.0	0	-100	0	-50	ps
1.9	5	-100	3	-50	ps
1.8	11	-100	6	-50	ps
1.7	18	-100	9	-50	ps
1.6	25	-100	13	-50	ps
1.5	33	-100	17	-50	ps
1.4	43	-100	22	-50	ps
1.3	54	-100	27	-50	ps
1.2	67	-100	34	-50	ps
1.1	82	-100	41	-50	ps
1.0	100	-100	50	-50	ps
CK, CK# Differential Sew Rate: 1.5 V/ns					
2.0	30	-70	30	-20	ps
1.9	35	-70	33	-20	ps
1.8	41	-70	36	-20	ps
1.7	48	-70	39	-20	ps
1.6	55	-70	43	-20	ps
1.5	63	-70	47	-20	ps
1.4	73	-70	52	-20	ps
1.3	84	-70	57	-20	ps
1.2	97	-70	64	-20	ps
1.1	112	-70	71	-20	ps
1.0	130	-70	80	-20	ps
CK, CK# Differential Sew Rate: 1.0 V/ns					
2.0	60	-40	60	10	ps
1.9	65	-40	63	10	ps
1.8	71	-40	66	10	ps
1.7	78	-40	69	10	ps
1.6	85	-40	73	10	ps
1.5	93	-40	77	10	ps
1.4	103	-40	82	10	ps
1.3	114	-40	87	10	ps
1.2	127	-40	94	10	ps
1.1	142	-40	101	10	ps
1.0	160	-40	110	10	ps



Table 12: Data Setup and Hold Derating Values

Data Slew Rate (V/ns)	$t_{DS} V_{REF}$ to CK/CK# Crossing	$t_{DS} V_{IH(AC)} MIN$ to CK/CK# Crossing	$t_{DH} CK/CK#$ Crossing to $V_{REF}$	$t_{DH} CK/CK#$ Crossing to $V_{IH(DC)} MIN$	Units
DK, DK# Differential Slew Rate: 2.0 V/ns					
2.0	0	-100	0	-50	ps
1.9	5	-100	3	-50	ps
1.8	11	-100	6	-50	ps
1.7	18	-100	9	-50	ps
1.6	25	-100	13	-50	ps
1.5	33	-100	17	-50	ps
1.4	43	-100	22	-50	ps
1.3	54	-100	27	-50	ps
1.2	67	-100	34	-50	ps
1.1	82	-100	41	-50	ps
1.0	100	-100	50	-50	ps
DK, DK# Differential Slew Rate: 1.5 V/ns					
2.0	30	-70	30	-20	ps
1.9	35	-70	33	-20	ps
1.8	41	-70	36	-20	ps
1.7	48	-70	39	-20	ps
1.6	55	-70	43	-20	ps
1.5	63	-70	47	-20	ps
1.4	73	-70	52	-20	ps
1.3	84	-70	57	-20	ps
1.2	97	-70	64	-20	ps
1.1	112	-70	71	-20	ps
1.0	130	-70	80	-20	ps
DK, DK# Differential Slew Rate: 1.0 V/ns					
2.0	60	-40	60	10	ps
1.9	65	-40	63	10	ps
1.8	71	-40	66	10	ps
1.7	78	-40	69	10	ps
1.6	85	-40	73	10	ps
1.5	93	-40	77	10	ps
1.4	103	-40	82	10	ps
1.3	114	-40	87	10	ps
1.2	127	-40	94	10	ps
1.1	142	-40	101	10	ps
1.0	160	-40	110	10	ps