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SIO RLDRAM 2

MT49H16M18C – 16 Meg x 18 x 8 banks

Features

- 533 MHz DDR operation (1.067 Gb/s/pin data rate)
- 38.4 Gb/s peak bandwidth (x36 at 533 MHz clock frequency)
- Organization
  - 16 Meg x 18 separate I/O
  - 8 banks
- Cyclic bank switching for maximum bandwidth
- Reduced cycle time (15ns at 533 MHz)
- Nonmultiplexed addresses (address multiplexing option available)
- SRAM-type interface
- Programmable READ latency (RL), row cycle time, and burst sequence length
- Balanced READ and WRITE latencies in order to optimize data bus utilization
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Differential input data clocks (DK*x*, DK*x*#)
- On-die DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32ms refresh (8K refresh for each bank; 64K refresh command must be issued in total each 32ms)
- HSTL I/O (1.5V or 1.8V nominal)
- 25–60Ω matched impedance outputs
- 2.5V V_{EXT}, 1.8V V_{DD}, 1.5V or 1.8V V_{DDQ} I/O
- On-die termination (ODT) R_{TT}

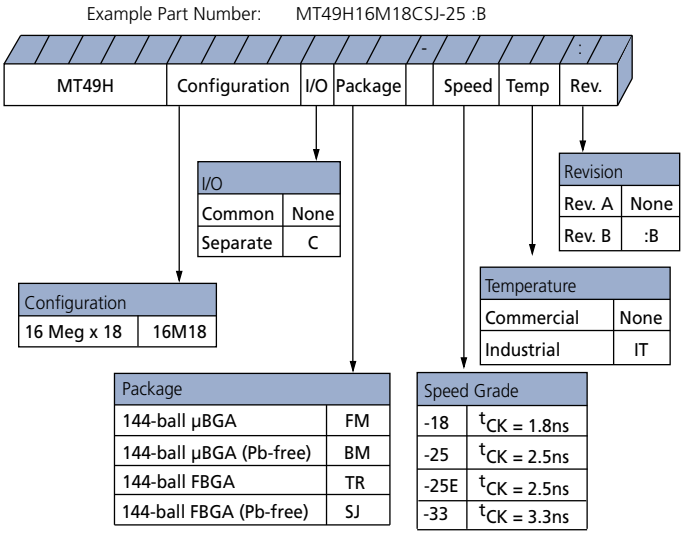
Options [1]	Marking
• Clock cycle timing	
– 1.875ns @ ^{t}RC = 15ns	-18
– 2.5ns @ ^{t}RC = 15ns	-25E
– 2.5ns @ ^{t}RC = 20ns	-25
– 3.3ns @ ^{t}RC = 20ns	-33
• Configuration	
– 16 Meg x 18	16M18
• Operating temperature range	
– Commercial (0° to +95°C)	None
– Industrial (T_C = –40°C to +95°C; T_A = –40°C to +85°C)	IT
• Package	
– 144-ball µBGA	FM
– 144-ball µBGA (Pb-free)	BM
– 144-ball FBGA	TR
– 144-ball FBGA (Pb-free)	SJ
• Revision	:B

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on micron.com for available offerings.

BGA Part Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. Micron's BGA Part Marking Decoder is available on Micron's Web site at micron.com.

Figure 1: 288Mb RLDRAM 2 SIO Part Numbers



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General Description

The Micron® reduced latency DRAM (RLDRAM®) 2 is a high-speed memory device designed for high bandwidth data storage—telecommunications, networking, and cache applications, etc. The chip's 8-bank architecture is optimized for sustainable high-speed operation.

The DDR separate I/O interface transfers two data words per clock cycle at the I/O balls. The read port has dedicated data outputs to support READ operations, while the write port has dedicated input balls to support WRITE operations. Output data is referenced to the free-running output data clock. This architecture eliminates the need for high-speed bus turnaround.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock(s).

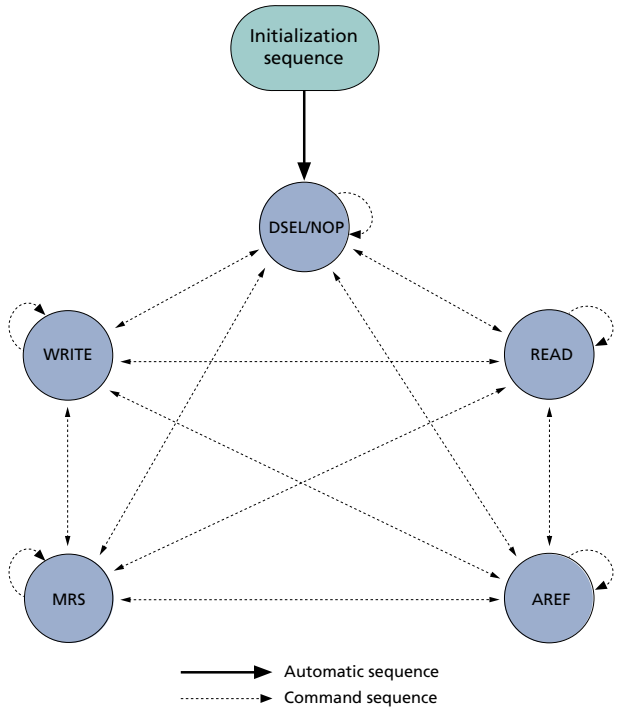
Read and write accesses to the device are burst-oriented. The burst length (BL) is programmable from 2, 4, or 8 by setting the mode register.

The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

Bank-scheduled refresh is supported with the row address generated internally.

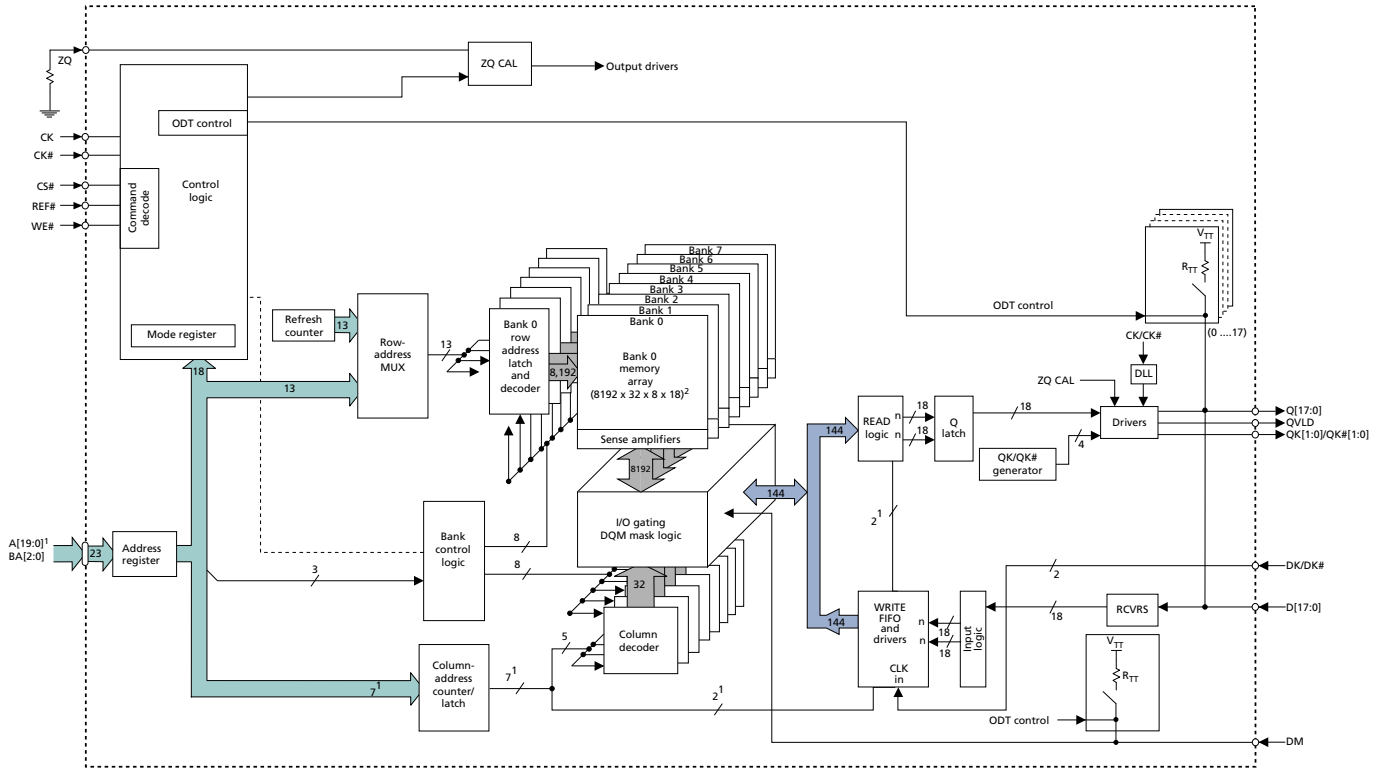
The µBGA 144-ball package is used to enable ultra high-speed data transfer rates and a simple upgrade path from early generation devices.

Figure 2: State Diagram



Functional Block Diagrams

Figure 3: 16 Meg x 18 Functional Block Diagram



Notes:
1. Examples for BL = 2; column address will be reduced with an increase in burst length.
2. The "8" = (length of burst) x 2^(number of column addresses to WRITE FIFO and READ logic).

Ball Assignments and Descriptions

Table 1: 16 Meg x 18 Ball Assignments (Top View) 144-Ball BGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	V_{REF}	V_{SS}	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TMS	TCK
B	V_{DD}	D4	Q4	V_{SSQ}					V_{SSQ}	Q0	D0	V_{DD}
C	V_{TT}	D5	Q5	V_{DDQ}					V_{DDQ}	Q1	D1	V_{TT}
D	A22[1]	D6	Q6	V_{SSQ}					V_{SSQ}	QK0#	QK0	V_{SS}
E	A21[2]	D7	Q7	V_{DDQ}					V_{DDQ}	Q2	D2	A20[2]
F	A5	D8	Q8	V_{SSQ}					V_{SSQ}	Q3	D3	QVLD
G	A8	A6	A7	V_{DD}					V_{DD}	A2	A1	A0
H	BA2	A9	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A4	A3
J	NF[3]	NF[3]	V_{DD}	V_{DD}					V_{DD}	V_{DD}	BA0	CK
K	DK	DK#	V_{DD}	V_{DD}					V_{DD}	V_{DD}	BA1	CK#
L	REF#	CS#	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A14	A13
M	WE#	A16	A17	V_{DD}					V_{DD}	A12	A11	A10
N	A18	D14	Q14	V_{SSQ}					V_{SSQ}	Q9	D9	A19
P	A15	D15	Q15	V_{DDQ}					V_{DDQ}	Q10	D10	DM
R	V_{SS}	QK1	QK1#	V_{SSQ}					V_{SSQ}	Q11	D11	V_{SS}
T	V_{TT}	D16	Q16	V_{DDQ}					V_{DDQ}	Q12	D12	V_{TT}
U	V_{DD}	D17	Q17	V_{SSQ}					V_{SSQ}	Q13	D13	V_{DD}
V	V_{REF}	ZQ	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TDO	TDI

Notes:
1. Reserved for future use. This may be optionally connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may be optionally connected to GND.
3. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may be optionally connected to GND.

Table 2: Ball Descriptions

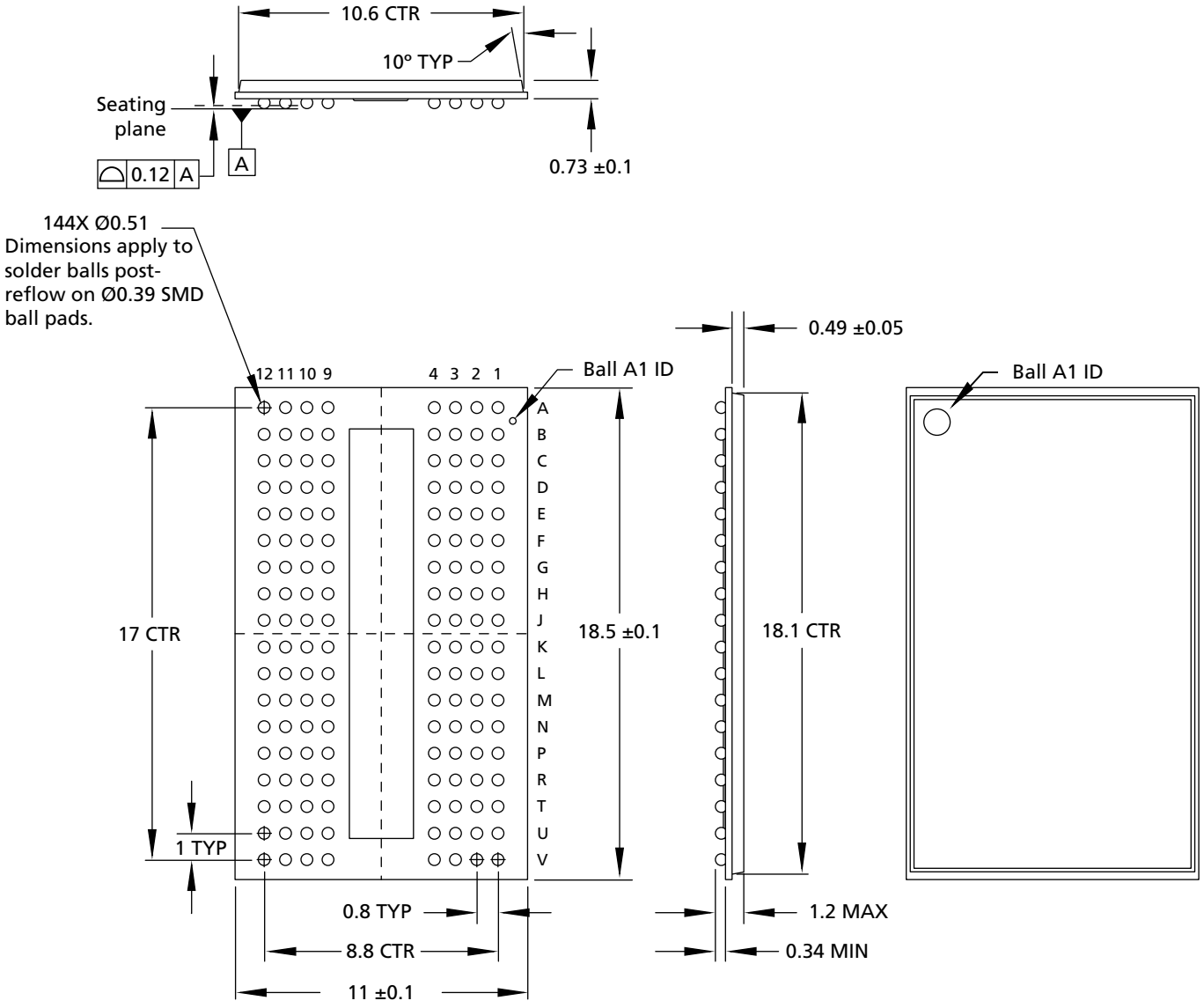
Symbol	Type	Description
A0–A19	Input	**Address inputs:** A0–A19 define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK.
BA0–BA2	Input	**Bank address inputs:** Select to which internal bank a command is being applied.
CK, CK#	Input	**Input clock:** CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	**Chip select:** CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
D0–D17	Input	**Data input:** The D signals form the 18-bit input data bus. During WRITE commands, the data is sampled at both edges of DK.

Table 2: Ball Descriptions (Continued)

Symbol	Type	Description
DK, DK#	Input	**Input data clock:** DK and DK# are the differential input data clocks. All input data is referenced to both edges of DK. DK# is ideally 180 degrees out of phase with DK. D0–D17 are referenced to DK and DK#.
DM	Input	**Input data mask:** The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM is sampled on both edges of DK. Tie signal to ground if not used.
TCK	Input	**IEEE 1149.1 clock input:** This ball must be tied to V_{SS} if the JTAG function is not used.
TMS, TDI	Input	**IEEE 1149.1 test inputs:** These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	**Command inputs:** Sampled at the positive edge of CK, WE# and REF# define (together with CS#) the command to be executed.
Q0–Q17	Output	**Data output:** The Q signals form the 18-bit output data bus. During READ commands, the data is referenced to both edges of QK.
QK*x*, QK*x*#	Output	**Output data clocks:** QK*x* and QK*x*# are opposite polarity, output data clocks. They are free-running, and during READs are edge-aligned with data output from the device. QK*x*# is ideally 180 degrees out of phase with QK*x*. QK0 and QK0# are aligned with Q0–Q8 and QK1 and QK1# are aligned with Q9–Q17.
QVLD	Output	**Data valid:** The QVLD pin indicates valid output data. QVLD is edge-aligned with QK*x* and QK*x*#.
TDO	Output	**IEEE 1149.1 test output:** JTAG output. This ball may be left as no connect if the JTAG function is not used.
ZQ	Reference	**External impedance (25–60Ω:** This signal is used to tune the device outputs to the system data bus impedance. Q output impedance is set to 0.2 × RQ, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode. Connecting ZQ to V_{DD} invokes the maximum impedance mode. Refer to figure: Mode Register Definition in Nonmultiplexed Address Mode to activate this function.
V_{DD}	Supply	**Power supply:** Nominally 1.8V. For range, see table: DC Electrical Characteristics and Operating Conditions.
V_{DDQ}	Supply	**DQ power supply:** Nominally, 1.5V or 1.8V. Isolated on the device for improved noise immunity. For range, see table: DC Electrical Characteristics and Operating Conditions.
V_{EXT}	Supply	**Power supply:** Nominally, 2.5V. For range, see table: DC Electrical Characteristics and Operating Conditions.
V_{REF}	Supply	**Input reference voltage:** Nominally $V_{DDQ}/2$. Provides a reference voltage for the input buffers.
V_{SS}	Supply	Ground.
V_{SSQQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
V_{TT}	Supply	**Power supply:** Isolated termination supply. Nominally, $V_{DDQ}/2$. For range, see table: DC Electrical Characteristics and Operating Conditions.
A20–A21	–	**Reserved for future use:** These signals are internally connected and can be treated as address inputs.
A22	–	**Reserved for future use:** This signal is not connected and can be connected to ground.
NF	–	**No function:** These balls can be connected to ground.

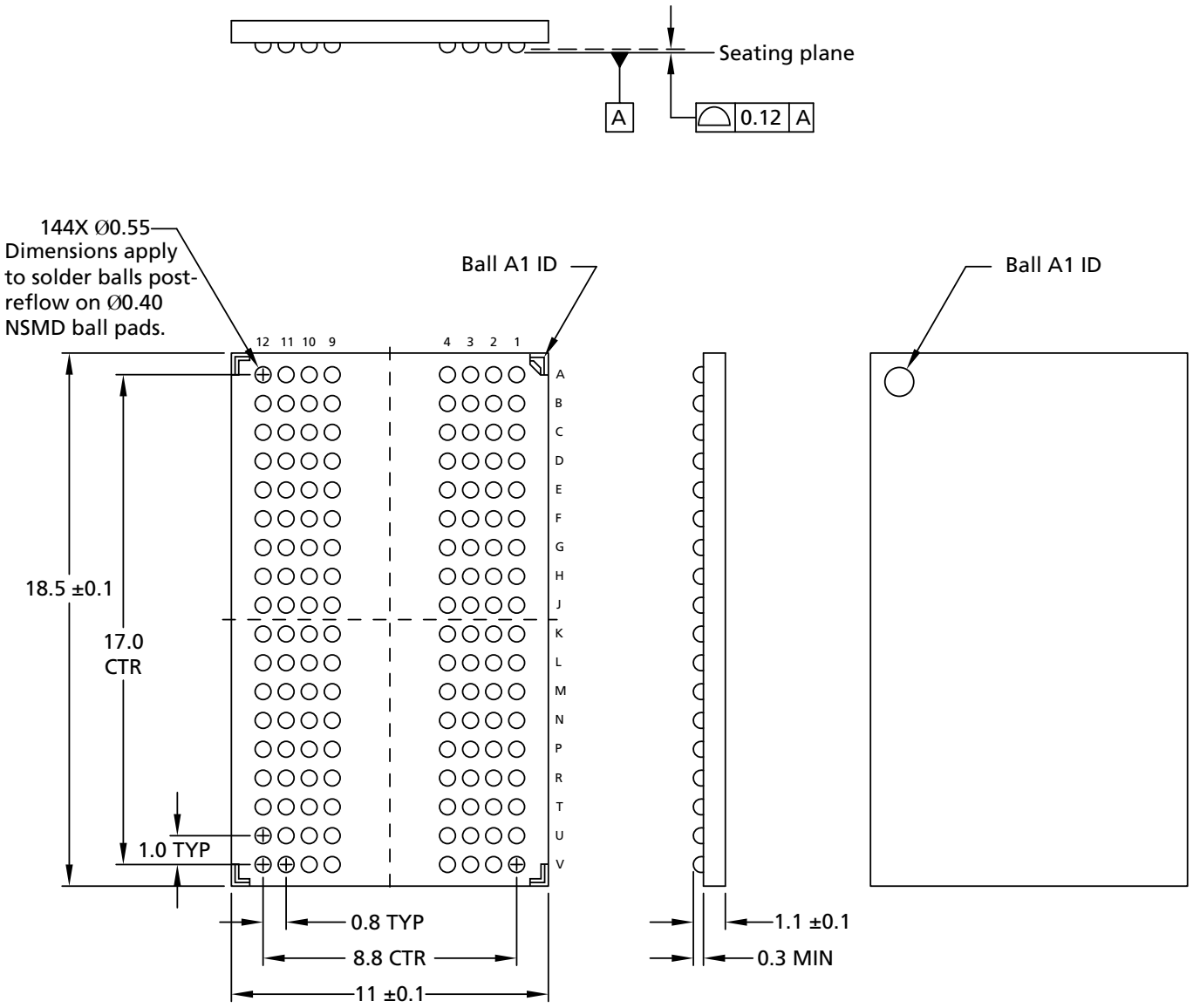
Package Dimensions

Figure 4: 144-Ball µBGA



Notes:
1. All dimensions are in millimeters.
2. Solder Ball Material:
   SAC305 (96.5% Sn, 3% Ag, 0.5% Cu) or
   Eutectic (62% Sn, 36% Pb, 2% Ag)

Figure 5: 144-Ball FBGA



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Electrical Specifications – I_{DD}

Table 3: I_{DD} Operating Conditions and Maximum Limits – Rev. A

Description	Conditions	Symbol	-25	-33	-5	Unit
Standby current	^{t}CK = Idle; All banks idle; No inputs toggling	I_{SB1} (V_{DD})	48	48	48	mA
		I_{SB1} (V_{EXT})	26	26	26	
Active standby current	^{t}CK = MIN, CS# = 1; No commands; Bank address incremented and half address/data change once every 4 clock cycles	I_{SB2} (V_{DD})	288	233	189	mA
		I_{SB2} (V_{EXT})	26	26	26	
Operational current	BL = 2; ^{t}CK = MIN; ^{t}RC = MIN; 1 bank active; Half address changes once per ^{t}RC; Read followed by write sequence	I_{DD1} (V_{DD})	348	305	255	mA
		I_{DD1} (V_{EXT})	41	36	36	
Operational current	BL = 4; ^{t}CK = MIN; ^{t}RC = MIN; 1 bank active; Half address changes once per ^{t}RC; Read followed by write sequence	I_{DD2} (V_{DD})	362	319	269	mA
		I_{DD2} (V_{EXT})	48	42	42	
Operational current	BL = 8; ^{t}CK = MIN; ^{t}RC = MIN; 1 bank active; Half address changes once per ^{t}RC; Read followed by write sequence	I_{DD3} (V_{DD})	408	368	286	mA
		I_{DD3} (V_{EXT})	55	48	48	
Burst refresh current	^{t}CK = MIN; ^{t}RC = MIN; Cyclic bank refresh; Data inputs are switching	I_{REF1} (V_{DD})	785	615	430	mA
		I_{REF1} (V_{EXT})	133	111	105	
Distributed refresh current	^{t}CK = MIN; ^{t}RC = MIN; Single bank refresh; Half address/data toggle	I_{REF2} (V_{DD})	325	267	221	mA
		I_{REF2} (V_{EXT})	48	42	42	
Operating burst write current example	BL = 2; ^{t}CK = MIN; ^{t}RC = MIN; Cyclic bank access; Half of address bits change every clock cycle; Continuous data	I_{DD2W} (V_{DD})	970	819	597	mA
		I_{DD2W} (V_{EXT})	100	90	69	
Operating burst write current example	BL = 4; ^{t}CK = MIN; ^{t}RC = MIN; Cyclic bank access; Half of address bits change every 2 clock cycles; Continuous data	I_{DD4W} (V_{DD})	779	609	439	mA
		I_{DD4W} (V_{EXT})	88	77	63	
Operating burst write current example	BL = 8; ^{t}CK = MIN; ^{t}RC = MIN; Cyclic bank access; Half of address bits change every 4 clock cycles; Continuous data	I_{DD8W} (V_{DD})	668	525	364	mA
		I_{DD8W} (V_{EXT})	60	51	40	
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Measurement is taken during continuous READ	I_{DD2R} (V_{DD}) x18	860	735	525	mA
		I_{DD2R} (V_{EXT})	100	90	69	
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every 2 clocks; Measurement is taken during continuous READ	I_{DD4R} (V_{DD}) x18	680	525	380	mA
		I_{DD4R} (V_{EXT})	88	77	63	
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every 4 clock cycles; Measurement is taken during continuous READ	I_{DD8R} (V_{DD}) x18	570	450	310	mA
		I_{DD8R} (V_{EXT})	60	51	40	

Table 4: I_{DD} Operating Conditions and Maximum Limits – Rev. B

Description	Conditions	Symbol	-18	-25E	-25	-33	Unit
Standby current	tCK = Idle; All banks idle; No inputs toggling	I_{SB1} (V_{DD})	55	55	55	55	mA
		I_{SB1} (V_{EXT})	5	5	5	5	
Active standby current	tCK = MIN, CS# = 1; No commands; Bank address incremented and half address/data change once every 4 clock cycles	I_{SB2} (V_{DD})	250	215	215	190	mA
		I_{SB2} (V_{EXT})	5	5	5	5	
Operational current	BL = 2; tCK = MIN; tRC = MIN; 1 bank active; Half address changes once per tRC; Read followed by write sequence	I_{DD1} (V_{DD})	310	285	260	225	mA
		I_{DD1} (V_{EXT})	10	10	10	10	
Operational current	BL = 4; tCK = MIN; tRC = MIN; 1 bank active; Half address changes once per tRC; Read followed by write sequence	I_{DD2} (V_{DD})	315	290	260	220	mA
		I_{DD2} (V_{EXT})	10	10	10	10	
Operational current	BL = 8; tCK = MIN; tRC = MIN; 1 bank active; Half address changes once per tRC; Read followed by write sequence	I_{DD3} (V_{DD})	330	305	275	230	mA
		I_{DD3} (V_{EXT})	15	15	15	15	
Burst refresh current	tCK = MIN; tRC = MIN; Cyclic bank refresh; Data inputs are switching	I_{REF1} (V_{DD})	660	540	530	430	mA
		I_{REF1} (V_{EXT})	45	30	30	25	
Distributed refresh current	tCK = MIN; tRC = MIN; Single bank refresh; Half address/data toggle	I_{REF2} (V_{DD})	295	265	250	215	mA
		I_{REF2} (V_{EXT})	10	10	10	10	
Operating burst write current example	BL = 2; tCK = MIN; tRC = MIN; Cyclic bank access; Half of address bits change every clock cycle; Continuous data	I_{DD2W} (V_{DD})	830	655	655	530	mA
		I_{DD2W} (V_{EXT})	40	35	35	30	
Operating burst write current example	BL = 4; tCK = MIN; tRC = MIN; Cyclic bank access; Half of address bits change every 2 clock cycles; Continuous data	I_{DD4W} (V_{DD})	580	465	465	385	mA
		I_{DD4W} (V_{EXT})	25	20	20	20	
Operating burst write current example	BL = 8; tCK = MIN; tRC = MIN; Cyclic bank access; Half of address bits change every 4 clock cycles; Continuous data	I_{DD8W} (V_{DD})	445	370	370	305	mA
		I_{DD8W} (V_{EXT})	25	20	20	20	
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Measurement is taken during continuous READ	I_{DD2R} (V_{DD}) x18	805	640	640	515	mA
		I_{DD2R} (V_{EXT})	40	35	35	30	
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every 2 clocks; Measurement is taken during continuous READ	I_{DD4R} (V_{DD}) x18	545	440	440	365	mA
		I_{DD4R} (V_{EXT})	25	20	20	20	
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every 4 clock cycles; Measurement is taken during continuous READ	I_{DD8R} (V_{DD}) x18	410	335	335	280	mA
		I_{DD8R} (V_{EXT})	25	20	20	20	

Notes:
1. I_{DD} specifications are tested after the device is properly initialized. +0°C ≤ T_c ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, +2.38V ≤ V_{EXT} ≤ +2.63V, +1.4V ≤ V_{DDQ} ≤ V_{DD}, V_{REF} = V_{DDQ}/2.
2. tCK = tDK = MIN; tRC = MIN.
3. Input slew rate is specified in the Input AC Logic Levels table.
4. Definitions for I_{DD} conditions:
   4a. LOW is defined as V_{IN} ≤ $V_{IL(AC)}$ MAX.

4b. HIGH is defined as $V_{IN} \geq V_{IH(AC)}$ MAX.
4c. Stable is defined as inputs remaining at a HIGH or LOW level.
4d. Floating is defined as inputs at $V_{REF} = V_{DDQ}/2$.
4e. Continuous is defined as half the D or Q signals changing between HIGH and LOW every half clock cycle (twice per clock).
4f. Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
4g. Sequential bank access is defined as the bank address incrementing by one every $_tRC$.
4h. Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2, this is every clock; for BL = 4, this is every other clock; and for BL = 8, this is every fourth clock.

5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
6. I_{DD} parameters are specified with ODT disabled.
7. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
8. IDD tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#). Parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5: Absolute Maximum Ratings

Parameter	Min	Max	Units
I/O voltage	–0.3	V_{DDQ} + 0.3	V
Voltage on V_{EXT} supply relative to V_{SS}	–0.3	+2.8	V
Voltage on V_{DD} supply relative to V_{SS}	–0.3	+2.1	V
Voltage on V_{DDQ} supply relative to V_{SS}	–0.3	+2.1	V

AC and DC Operating Conditions

Table 6: DC Electrical Characteristics and Operating Conditions

Description	Conditions	Symbol	Min	Max	Units	Notes
Supply voltage	–	V_{EXT}	2.38	2.63	V	
Supply voltage	–	V_{DD}	1.7	1.9	V	2
Isolated output buffer supply	–	V_{DDQ}	1.4	V_{DD}	V	2, 3
Reference voltage	–	V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	4, 5, 6
Termination voltage	–	V_{TT}	0.95 × V_{REF}	1.05 × V_{REF}	V	7, 8
Input high (logic 1) voltage	–	V_{IH}	V_{REF} + 0.1	V_{DDQ} + 0.3	V	2
Input low (logic 0) voltage	–	V_{IL}	V_{SSQ} - 0.3	V_{REF} - 0.1	V	2
Output high current	V_{OH} = V_{DDQ}/2	I_{OH}	(V_{DDQ}/2)/ (1.15 × RQ/5)	(V_{DDQ}/2)/ (0.85 × RQ/5)	A	9, 10, 11
Output low current	V_{OL} = V_{DDQ}/2	I_{OL}	(V_{DDQ}/2)/ (1.15 × RQ/5)	(V_{DDQ}/2)/ (0.85 × RQ/5)	A	9, 10, 11
Clock input leakage current	0V ≤ V_{IN} ≤ V_{DD}	I_{LC}	–5	5	µA	
Input leakage current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	–5	5	µA	
Output leakage current	0V ≤ V_{IN} ≤ V_{DDQ}	I_{LO}	–5	5	µA	
Reference voltage current	–	I_{REF}	–5	5	µA	

Notes:
1. Applies to the entire table: Unless otherwise noted: +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V
2. All voltages referenced to V_{SS} (GND).
3. Overshoot: $V_{IH(AC)}$ ≤ V_{DD} + 0.7V for t ≤ ^{t}CK/2. Undershoot: $V_{IL(AC)}$ ≥ –0.5V for t ≤ ^{t}CK/2. During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals may not have pulse widths less than ^{t}CK/2 or operate at frequencies exceeding ^{t}CK (MAX).
4. V_{DDQ} can be set to a nominal 1.5V ± 0.1V or 1.8V ± 0.1V supply.
5. Typically the value of V_{REF} is expected to be 0.5 x V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
6. Peak-to-peak AC noise on V_{REF} must not exceed ±2% $V_{REF(DC)}$.

7. V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2% of the DC value. Thus, from $V_{DDQ}/2$, V_{REF} is allowed ±2% $V_{DDQ}/2$ for DC error and an additional ±2% $V_{DDQ}/2$ for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
8. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
9. On-die termination may be selected using mode register bit 9 (see figure: Mode Register Definition in Nonmultiplexed Address Mode). A resistance R_{TT} from each data input signal to the nearest V_{TT} can be enabled. R_{TT} = 125–185Ω at 95°C T_C.
10. I_{OH} and I_{OL} are defined as absolute values and are measured at $V_{DDQ}/2$. I_{OH} flows from the device, I_{OL} flows into the device.
11. If MRS bit A8 is 0, use RQ = 250Ω in the equation in lieu of presence of an external impedance matched resistor.
12. For V_{OL} and V_{OH}, refer to the RLDRAM 2, HSPICE, or IBIS driver models.

Table 7: Input AC Logic Levels

Description	Symbol	Min	Max	Units
Input high (logic 1) voltage	V_{IH}	V_{REF} + 0.2	–	V
Input low (logic 0) voltage	V_{IL}	–	V_{REF} - 0.2	V

Notes:
1. Unless otherwise noted: +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V
2. All voltages referenced to V_{SS} (GND).
3. The AC and DC input level specifications are as defined in the HSTL standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
4. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between $V_{il(AC)}$ and $V_{IH(AC)}$ (see figure below).

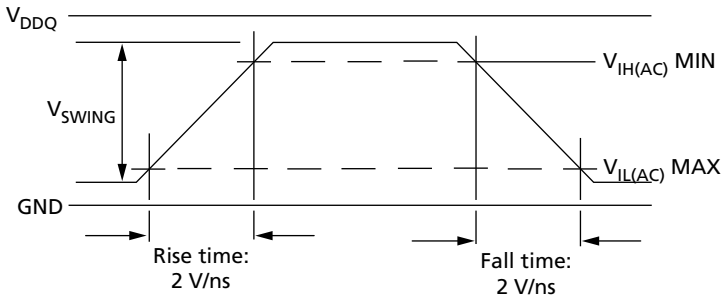


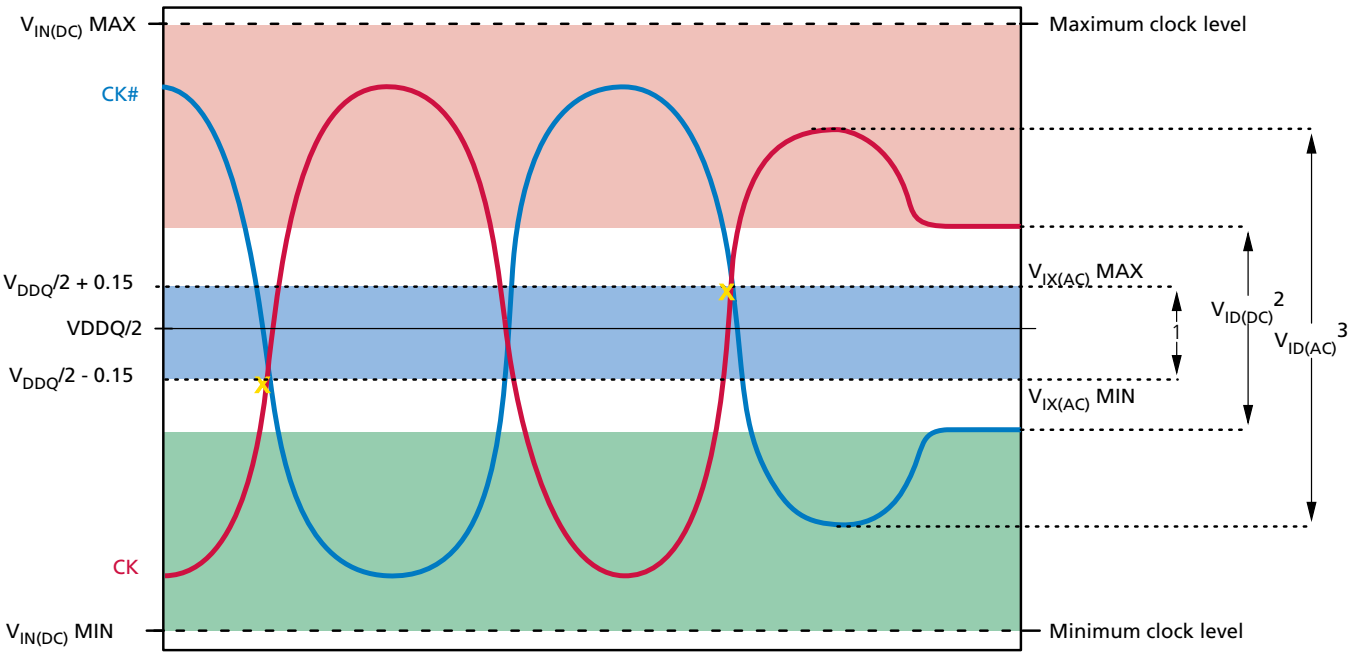
Table 8: Differential Input Clock Operating Conditions

Notes 1–5 apply to the entire table.

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input voltage level: CK and CK#	$V_{IN(DC)}$	–0.3	V_{DDQ} + 0.3	V	
Clock input differential voltage: CK and CK#	$V_{ID(DC)}$	0.2	V_{DDQ} + 0.6	V	5
Clock input differential voltage: CK and CK#	$V_{ID(AC)}$	0.4	V_{DDQ} + 0.6	V	5
Clock input crossing point voltage: CK and CK#	$V_{IX(AC)}$	$V_{DDQ}/2$ - 0.15	$V_{DDQ}/2$ + 0.15	V	6

Notes:
1. Unless otherwise noted: +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V
2. DK*x* and DK*x*# have the same requirements as CK and CK#.
3. All voltages referenced to V_{SS} (GND).
4. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is V_{REF}.
5. CK and CK# input slew rate must be ≥2 V/ns (≥4 V/ns if measured differentially).
6. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
7. The value of V_{IX} is expected to equal $V_{DDQ}/2$ of the transmitting device and must track variations in the DC level of the same.

Figure 6: Clock Input



Notes:
1. CK and CK# must cross within this region.
2. CK and CK# must meet at least $V_{ID(DC)}$ MIN when static and centered around $V_{DDQ}/2$.
3. Minimum peak-to-peak swing.
4. It is a violation to tri-state CK and CK# after the part is initialized.

Input Slew Rate Derating

The following two tables define the address, command, and data setup and hold derating values. These values are added to the default ^{t}AS/^{t}CS/^{t}DS and ^{t}AH/^{t}CH/^{t}DH specifications when the slew rate of any of these input signals is less than the 2 V/ns the nominal setup and hold specifications are based upon.

To determine the setup and hold time needed for a given slew rate, add the ^{t}AS/^{t}CS default specification to the "^{t}AS/^{t}CS V_{REF} to CK/CK# Crossing" and the ^{t}AH/^{t}CH default specification to the "^{t}AH/^{t}CH CK/CK# Crossing to V_{REF}" derated values on the Address and Command Setup and Hold Derating Values table. The derated data setup and hold values can be determined in a like manner using the "^{t}DS V_{REF} to CK/CK# Crossing" and "^{t}DH to CK/CK# Crossing to V_{REF}" values on the Data Setup and Hold Derating Values table. The derating values on the Address and Command Setup and Hold Derating Values table and the Data Setup and Hold Derating Values table apply to all speed grades.

The setup times on the Address and Command Setup and Hold Derating Values table and the Data Setup and Hold Derating Values table represent a rising signal. In this case, the time from which the rising signal crosses $V_{IH(AC)}$ min to the CK/CK# cross point is static and must be maintained across all slew rates. The derated setup timing represents the point at which the rising signal crosses $V_{REF(DC)}$ to the CK/CK# cross point. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between $V_{IH(AC)}$ MIN and the CK/CK# cross point. The setup values in the Address and Command Setup and Hold Derating Values table and the Data Setup and Hold Derating Values table are also valid for falling signals (with respect to $V_{IH(AC)}$ max and the CK/CK# cross point).

The hold times in the Address and Command Setup and Hold Derating Values table and the Data Setup and Hold Derating Values table represent falling signals. In this case, the time from which the falling signal crosses the CK/CK# cross point to when the signal crosses $V_{IH(DC)}$ MIN is static and must be maintained across all slew rates. The derated hold timing represents the delta between the CK/CK# cross point to when the falling signal crosses $V_{REF(DC)}$. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between the CK/CK# cross point and $V_{IH(DC)}$. The hold values in the Address and Command Setup and Hold Derating Values table and the Data Setup and Hold Derating Values table are also valid for rising signals (with respect to $V_{IL(DC)}$ max and the CK and CK# cross point).

Table 9: Address and Command Setup and Hold Derating Values

Command/ Address Slew Rate (V/ns)	^{t}AS/^{t}CS V_{REF} to CK/CK# Crossing	^{t}AS/^{t}CS $V_{IH(AC)}$ Min to CK/CK# Crossing	^{t}AH/^{t}CH CK/CK# Crossing to V_{REF}	^{t}AH/^{t}CH CK/CK# Crossing to $V_{IH(DC)}$ Min	Units
CK, CK# Differential Slew Rate: 2.0 V/ns					
2.0	0	–100	0	–50	ps
1.9	5	–100	3	–50	ps
1.8	11	–100	6	–50	ps
1.7	18	–100	9	–50	ps
1.6	25	–100	13	–50	ps
1.5	33	–100	17	–50	ps

Table 9: Address and Command Setup and Hold Derating Values (Continued)

Command/ Address Slew Rate (V/ns)	$^{t}AS/^{t}CS$ V_{REF} to CK/CK# Crossing	$^{t}AS/^{t}CS$ $V_{IH(AC)}$ Min to CK/CK# Crossing	$^{t}AH/^{t}CH$ CK/CK# Crossing to V_{REF}	$^{t}AH/^{t}CH$ CK/CK# Crossing to $V_{IH(DC)}$ Min	Units
1.4	43	–100	22	–50	ps
1.3	54	–100	27	–50	ps
1.2	67	–100	34	–50	ps
1.1	82	–100	41	–50	ps
1.0	100	–100	50	–50	ps
CK, CK# Differential Slew Rate: 1.5 V/ns					
2.0	30	–70	30	–20	ps
1.9	35	–70	33	–20	ps
1.8	41	–70	36	–20	ps
1.7	48	–70	39	–20	ps
1.6	55	–70	43	–20	ps
1.5	63	–70	47	–20	ps
1.4	73	–70	52	–20	ps
1.3	84	–70	57	–20	ps
1.2	97	–70	64	–20	ps
1.1	112	–70	71	–20	ps
1.0	130	–70	80	–20	ps
CK, CK# Differential Slew Rate: 1.0 V/ns					
2.0	60	–40	60	10	ps
1.9	65	–40	63	10	ps
1.8	71	–40	66	10	ps
1.7	78	–40	69	10	ps
1.6	85	–40	73	10	ps
1.5	93	–40	77	10	ps
1.4	103	–40	82	10	ps
1.3	114	–40	87	10	ps
1.2	127	–40	94	10	ps
1.1	142	–40	101	10	ps
1.0	160	–40	110	10	ps

Table 10: Data Setup and Hold Derating Values

Data Slew Rate (V/ns)	^{t}DS V_{REF} to CK/CK# Crossing	^{t}DS $V_{IH(AC)}$ Min to CK/CK# Crossing	^{t}DH CK/CK# Crossing to V_{REF}	^{t}DH CK/CK# Crossing to $V_{IH(DC)}$ Min	Units
DK, DK# Differential Slew Rate: 2.0 V/ns					
2.0	0	–100	0	–50	ps
1.9	5	–100	3	–50	ps
1.8	11	–100	6	–50	ps
1.7	18	–100	9	–50	ps
1.6	25	–100	13	–50	ps
1.5	33	–100	17	–50	ps
1.4	43	–100	22	–50	ps
1.3	54	–100	27	–50	ps
1.2	67	–100	34	–50	ps
1.1	82	–100	41	–50	ps
1.0	100	–100	50	–50	ps
DK, DK# Differential Slew Rate: 1.5 V/ns					
2.0	30	–70	30	–20	ps
1.9	35	–70	33	–20	ps
1.8	41	–70	36	–20	ps
1.7	48	–70	39	–20	ps
1.6	55	–70	43	–20	ps
1.5	63	–70	47	–20	ps
1.4	73	–70	52	–20	ps
1.3	84	–70	57	–20	ps
1.2	97	–70	64	–20	ps
1.1	112	–70	71	–20	ps
1.0	130	–70	80	–20	ps
DK, DK# Differential Slew Rate: 1.0 V/ns					
2.0	60	–40	60	10	ps
1.9	65	–40	63	10	ps
1.8	71	–40	66	10	ps
1.7	78	–40	69	10	ps
1.6	85	–40	73	10	ps
1.5	93	–40	77	10	ps
1.4	103	–40	82	10	ps
1.3	114	–40	87	10	ps
1.2	127	–40	94	10	ps
1.1	142	–40	101	10	ps
1.0	160	–40	110	10	ps

Figure 7: Nominal ^{t}AS/^{t}CS/^{t}DS and ^{t}AH/^{t}CH/^{t}DH Slew Rate

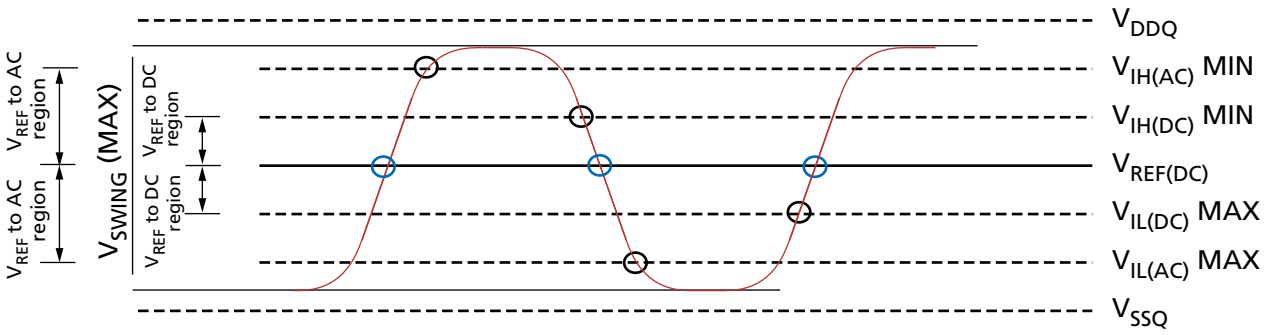


Table 11: Capacitance – µBGA

Description	Symbol	Conditions	Min	Max	Units
Address/control input capacitance	C_I	T_A = 25°C; *f* = 100 MHz V_{DD} = V_{DDQ} = 1.8V	1.0	2.0	pF
Input/output capacitance (D, Q, DM, and QK/QK#)	C_O		3.0	4.5	pF
Clock capacitance (CK/CK#, and DK/DK#)	C_{CK}		1.5	2.5	pF
JTAG pins	C_{JTAG}		1.5	4.5	pF

Notes: 1. Capacitance is not tested on ZQ pin.
2. JTAG pins are tested at 50 MHz.

Table 12: Capacitance – FBGA

Description	Symbol	Conditions	Min	Max	Units
Address/control input capacitance	C_I	T_A = 25°C; *f* = 100 MHz V_{DD} = V_{DDQ} = 1.8V	1.5	2.5	pF
Input/output capacitance (D, Q, DM, and QK/QK#)	C_O		3.5	5.0	pF
Clock capacitance (CK/CK#, and DK/DK#)	C_{CK}		2.0	3.0	pF
JTAG pins	C_{JTAG}		2.0	5.0	pF

Notes: 1. Capacitance is not tested on ZQ pin.
2. JTAG pins are tested at 50 MHz.

Table 13: AC Electrical Characteristics

Notes 1-4 apply to the entire table.

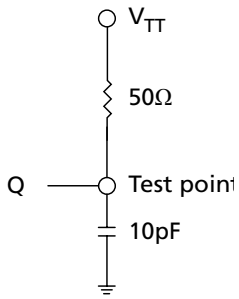
Description	Symbol	-18		-25E		-25		-33		-5		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock													
Input clock cycle time	^{t}CK	1.875	5.7	2.5	5.7	2.5	5.7	3.3	5.7	5.0	5.7	ns	
Input data clock cycle time	^{t}DK	^{t}CK		^{t}CK		^{t}CK		^{t}CK		^{t}CK		ns	
Clock jitter: period	^{t}JITper	–100	100	–150	150	–150	150	–200	200	–250	250	ps	5, 6
Clock jitter: cycle-to-cycle	^{t}JITcc		200		300		300		400		500	ps	
Clock HIGH time	^{t}CKH, ^{t}DKH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CK	
Clock LOW time	^{t}CKL, ^{t}DKL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CK	
Clock to input data clock	^{t}CKDK	–0.3	0.3	–0.45	0.5	–0.3	0.5	–0.3	1.0	–0.3	1.5	ns	
Mode register set cycle time to any command	^{t}MRSC	6	–	6	–	6	–	6	–	6	–	^{t}CK	
Setup Times													
Address/command and input setup time	^{t}AS/^{t}CS	0.3	–	0.4	–	0.4	–	0.5	–	0.8	–	ns	
Data-in and data mask to DK setup time	^{t}DS	0.17	–	0.25	–	0.25	–	0.3	–	0.4	–	ns	
Hold Times													
Address/command and input hold time	^{t}AH/^{t}CH	0.3	–	0.4	–	0.4	–	0.5	–	0.8	–	ns	
Data-in and data mask to DK hold time	^{t}DH	0.17	–	0.25	–	0.25	–	0.3	–	0.4	–	ns	
Data and Data Strobe													
Output data clock HIGH time	^{t}QKH	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CKH	
Output data clock LOW time	^{t}QKL	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CKL	
Half-clock period	^{t}QHP	MIN (^{t}QKH, ^{t}QKL)	–	MIN (^{t}QKH, ^{t}QKL)	–	MIN (^{t}QKH, ^{t}QKL)	–	MIN (^{t}QKH, ^{t}QKL)	–	MIN (^{t}QKH, ^{t}QKL)	–	–	

Table 13: AC Electrical Characteristics (Continued)

Notes 1-4 apply to the entire table.

Description	Symbol	-18		-25E		-25		-33		-5		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
QK edge to clock edge skew	^{t}CKQK	–0.2	0.2	–0.25	0.25	–0.25	0.25	–0.3	0.3	–0.5	0.5	ns	
QK edge to output data edge	^{t}QKQ0, ^{t}QKQ1	–0.12	0.12	–0.2	0.2	–0.2	0.2	–0.25	0.25	–0.3	0.3	ns	7
QK edge to any output data edge	^{t}QKQ	–0.22	0.22	–0.3	0.3	–0.3	0.3	–0.35	0.35	–0.4	0.4	ns	8
QK edge to QVLD	^{t}QKVLD	–0.22	0.22	–0.3	0.3	–0.3	0.3	–0.35	0.35	–0.4	0.4	ns	
Data valid window	^{t}DVW	^{t}QHP - (^{t}QKQ*x* [MAX] + | ^{t}QKQ*x* [MIN]|)	–	^{t}QHP - (^{t}QKQ*x* [MAX] + | ^{t}QKQ*x* [MIN]|)	–	^{t}QHP - (^{t}QKQ*x*[MAX] + |^{t}QKQ*x* [MIN]|)	–	^{t}QHP - (^{t}QKQ*x*[MAX] + |^{t}QKQ*x* [MIN]|)	–	^{t}QHP - (^{t}QKQ*x*[MAX] + |^{t}QKQ*x* [MIN]|)	–	–	
Refresh													
Average periodic refresh interval	^{t}REFI	–	0.49	–	0.49	–	0.49	–	0.49	–	0.49	µs	9

Notes:
1. All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V_{REF} of the command, address, and data signals.
2. Outputs measured with equivalent load:



3. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
4. AC timing may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. Frequency drift is not allowed.
7. ^{t}QKQ0 is referenced to Q0–Q8 and ^{t}QKQ1 is referenced to Q9–Q17 for a x18 device. For a x9 device, Q0–Q8 are referenced to ^{t}QKQ0 (x9 is only available in the 576Mb design).
8. ^{t}QKQ takes into account the skew between any QK*x* and any Q.

9. To improve efficiency, eight AREF commands (one for each bank) can be posted to the device on consecutive cycles at periodic intervals of 3.90µs.