Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CIO RLDRAM 2

MT49H64M9 – 64 Meg x 9 x 8 Banks
MT49H32M18 – 32 Meg x 18 x 8 Banks
MT49H16M36 – 16 Meg x 36 x 8 Banks

Features

- 533 MHz DDR operation (1.067 Gb/s/pin data rate)
- 38.4 Gb/s peak bandwidth (x36 at 533 MHz clock frequency)
- Organization
  - 64 Meg x 9, 32 Meg x 18, and 16 Meg x 36 I/O
  - 8 banks
- Reduced cycle time (15ns at 533 MHz)
- Nonmultiplexed addresses (address multiplexing option available)
- SRAM-type interface
- Programmable READ latency (RL), row cycle time, and burst sequence length
- Balanced READ and WRITE latencies in order to optimize data bus utilization
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Differential input data clocks (DK*x*, DK*x*#)
- On-die DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32ms refresh (16K refresh for each bank; 128K refresh command must be issued in total each 32ms)
- HSTL I/O (1.5V or 1.8V nominal)
- 25–60Ω matched impedance outputs
- 2.5V V_{EXT}, 1.8V V_{DD}, 1.5V or 1.8V V_{DDQ} I/O
- On-die termination (ODT) R_{TT}

Options[1]	Marking
• Clock cycle timing	
– 1.875ns @ ^{t}RC = 15ns	-18
– 2.5ns @ ^{t}RC = 15ns	-25E
– 2.5ns @ ^{t}RC = 20ns	-25
– 3.3ns @ ^{t}RC = 20ns	-33
• Configuration	
– 64 Meg x 9	64M9
– 32 Meg x 18	32M18
– 16 Meg x 36	16M36
• Operating temperature	
– Commercial (0° to +95°C)	None
– Industrial (T_C = –40°C to +95°C; T_A = –40°C to +85°C)	IT
• Package	
– 144-ball µBGA	FM
– 144-ball µBGA (Pb-free)	BM
– 144-ball FBGA	TR
– 144-ball FBGA (Pb-free)	SJ
• Revision	:A/:B

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on www.micron.com for available offerings.

BGA Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. Micron's BGA Part Marking Decoder is available on Micron's web site at micron.com.

Figure 1: Part Numbers

Example Part Number: MT49H16M36SJ-25 :B

MT49H	Configuration	I/O	Package	-	Speed	Temp.	:	Rev.

Configuration	
64 Meg x 9	64M9
32 Meg x 18	32M18
16 Meg x 36	16M36

I/O	
Common	None
Separate	C

Revision	
Rev. A	:A
Rev. B	:B

Package	
144-ball µBGA	FM
144-ball µBGA (Pb-free)	BM
144-ball FBGA	TR
144-ball FBGA (Pb-free)	SJ

Temperature	
Commercial	None
Industrial	IT

Speed Grade	
-18	^{t}CK = 1.875ns
-25E	^{t}CK = 2.5ns
-25	^{t}CK = 2.5ns
-33	^{t}CK = 3.3ns

Contents

List of Figures

List of Tables

General Description

RLDRAM® 2 is a high-speed memory device designed for high bandwidth data storage, telecommunications, networking, and cache applications, etc. The chip's 8-bank architecture is optimized for sustainable high-speed operation.

The DDR I/O interface transfers two data words per clock cycle at the I/O balls. Output data is referenced to the free-running output data clock.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock(s).

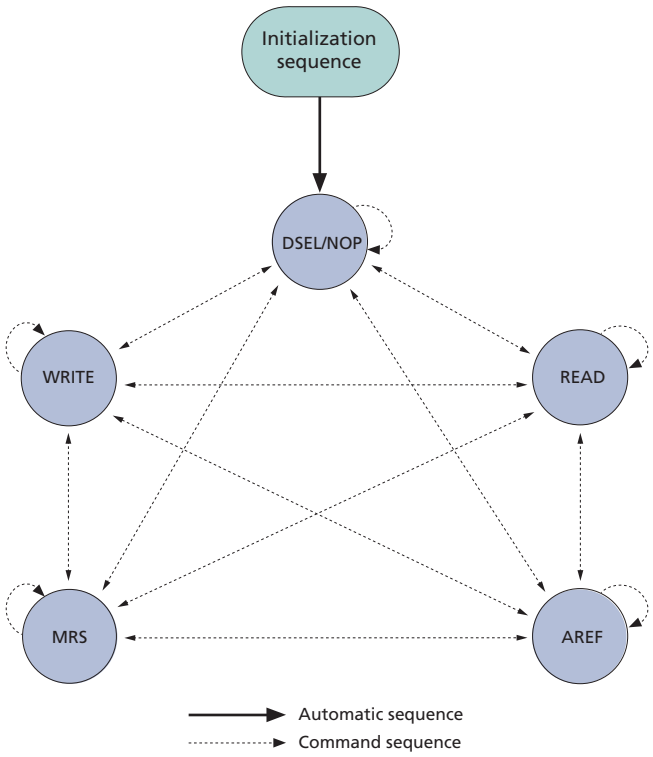
Read and write accesses are burst-oriented. The burst length (BL) is programmable from 2, 4, or 8 by setting the mode register.

The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

Bank-scheduled refresh is supported with the row address generated internally.

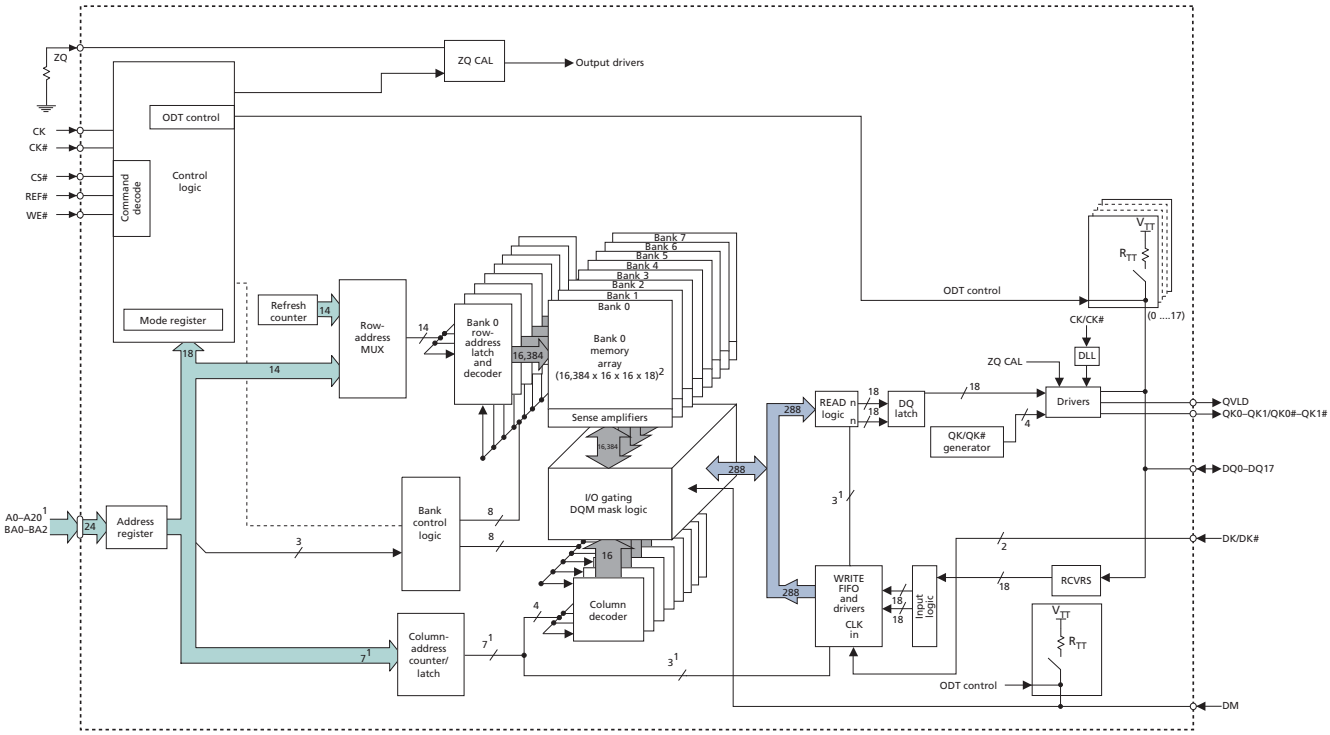
The µBGA 144-ball package enables ultra high-speed data transfer rates and a simple upgrade path from early generation devices.

Figure 2: Simplified State Diagram



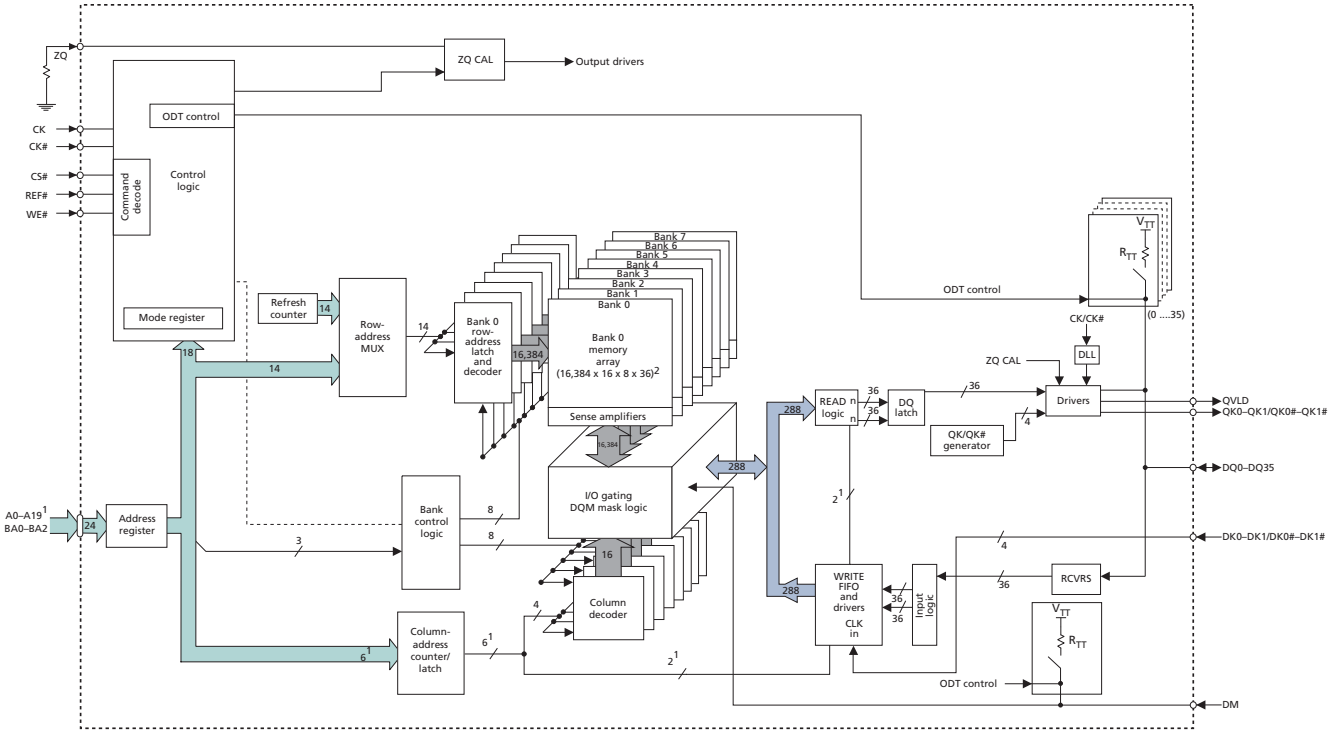
Functional Block Diagrams

Figure 3: 64 Meg x 9 Functional Block Diagram



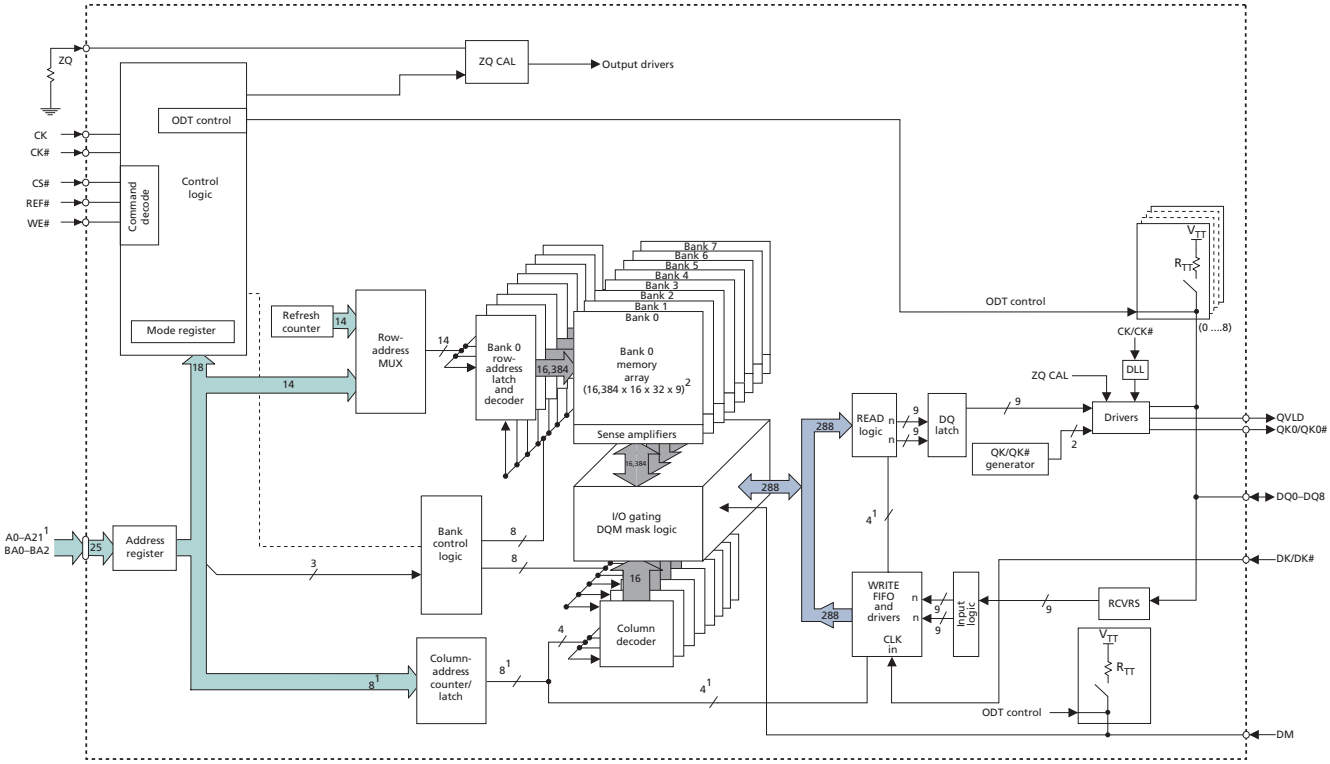
Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
2. 32 = (length of burst) x 2^(number of column addresses to WRITE FIFO and READ logic).

Figure 4: 32 Meg x 18 Functional Block Diagram



Notes: 1. Example for BL = 2; column address will be reduced with an increase in burst length.
2. 16 = (length of burst) x 2^(number of column addresses to WRITE FIFO and READ logic).

Figure 5: 16 Meg x 36 Functional Block Diagram



Notes:
1. Example for BL = 2; column address will be reduced with an increase in burst length.
2. 8 = (length of burst) x 2^(number of column addresses to WRITE FIFO and READ logic).

Ball Assignments and Descriptions

Table 1: 64 Meg x 9 Ball Assignments (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	V_{REF}	V_{SS}	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TMS	TCK
B	V_{DD}	DNU[3]	DNU[3]	V_{SSQ}					V_{SSQ}	DQ0	DNU[3]	V_{DD}
C	V_{TT}	DNU[3]	DNU[3]	V_{DDQ}					V_{DDQ}	DQ1	DNU[3]	V_{TT}
D	A22[1]	DNU[3]	DNU[3]	V_{SSQ}					V_{SSQ}	QK0#	QK0	V_{SS}
E	A21	DNU[3]	DNU[3]	V_{DDQ}					V_{DDQ}	DQ2	DNU[3]	A20
F	A5	DNU[3]	DNU[3]	V_{SSQ}					V_{SSQ}	DQ3	DNU[3]	QVLD
G	A8	A6	A7	V_{DD}					V_{DD}	A2	A1	A0
H	B2	A9	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A4	A3
J	NF[2]	NF[2]	V_{DD}	V_{DD}					V_{DD}	V_{DD}	B0	CK
K	DK	DK#	V_{DD}	V_{DD}					V_{DD}	V_{DD}	B1	CK#
L	REF#	CS#	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A14	A13
M	WE#	A16	A17	V_{DD}					V_{DD}	A12	A11	A10
N	A18	DNU[3]	DNU[3]	V_{SSQ}					V_{SSQ}	DQ4	DNU[3]	A19
P	A15	DNU[3]	DNU[3]	V_{DDQ}					V_{DDQ}	DQ5	DNU[3]	DM
R	V_{SS}	DNU[3]	DNU[3]	V_{SSQ}					V_{SSQ}	DQ6	DNU[3]	V_{SS}
T	V_{TT}	DNU[3]	DNU[4]	V_{DDQ}					V_{DDQ}	DQ7	DNU[3]	V_{TT}
U	V_{DD}	DNU[3]	DNU[3]	V_{SSQ}					V_{SSQ}	DQ8	DNU[3]	V_{DD}
V	V_{REF}	ZQ	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TDO	TDI

Notes:
1. Reserved for future use. This signal is not connected.
2. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to GND.
3. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND. Note that if ODT is enabled on Rev. A die, these pins will be connected to V_{TT}. The DNU pins are High-Z on Rev. B die when ODT is enabled.

Table 2: 32 Meg x 18 Ball Assignments (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	V_{REF}	V_{SS}	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TMS	TCK
B	V_{DD}	DNU[4]	DQ4	V_{SSQ}					V_{SSQ}	DQ0	DNU[4]	V_{DD}
C	V_{TT}	DNU[4]	DQ5	V_{DDQ}					V_{DDQ}	DQ1	DNU[4]	V_{TT}
D	A22[1]	DNU[4]	DQ6	V_{SSQ}					V_{SSQ}	QK0#	QK0	V_{SS}
E	A21[2]	DNU[4]	DQ7	V_{DDQ}					V_{DDQ}	DQ2	DNU[4]	A20
F	A5	DNU[4]	DQ8	V_{SSQ}					V_{SSQ}	DQ3	DNU[4]	QVLD
G	A8	A6	A7	V_{DD}					V_{DD}	A2	A1	A0
H	B2	A9	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A4	A3
J	NF[3]	NF[3]	V_{DD}	V_{DD}					V_{DD}	V_{DD}	B0	CK
K	DK	DK#	V_{DD}	V_{DD}					V_{DD}	V_{DD}	B1	CK#
L	REF#	CS#	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A14	A13
M	WE#	A16	A17	V_{DD}					V_{DD}	A12	A11	A10
N	A18	DNU[4]	DQ14	V_{SSQ}					V_{SSQ}	DQ9	DNU[4]	A19
P	A15	DNU[4]	DQ15	V_{DDQ}					V_{DDQ}	DQ10	DNU[4]	DM
R	V_{SS}	QK1	QK1#	V_{SSQ}					V_{SSQ}	DQ11	DNU[4]	V_{SS}
T	V_{TT}	DNU[4]	DQ16	V_{DDQ}					V_{DDQ}	DQ12	DNU[4]	V_{TT}
U	V_{DD}	DNU[4]	DQ17	V_{SSQ}					V_{SSQ}	DQ13	DNU[4]	V_{DD}
V	V_{REF}	ZQ	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TDO	TDI

Notes:
1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.
3. No function. This signal is internally connected and has parasitic characteristics of a clock input signal. This may optionally be connected to GND.
4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND. Note that if ODT is enabled on Rev. A die, these pins will be connected to V_{TT}. The DNU pins are High-Z on Rev. B die when ODT is enabled.

Table 3: 16 Meg x 36 Ball Assignments (Top View) 144-Ball µBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	V_{REF}	V_{SS}	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TMS	TCK
B	V_{DD}	DQ8	DQ9	V_{SSQ}					V_{SSQ}	DQ1	DQ0	V_{DD}
C	V_{TT}	DQ10	DQ11	V_{DDQ}					V_{DDQ}	DQ3	DQ2	V_{TT}
D	A22[1]	DQ12	DQ13	V_{SSQ}					V_{SSQ}	QK0#	QK0	V_{SS}
E	A21[2]	DQ14	DQ15	V_{DDQ}					V_{DDQ}	DQ5	DQ4	A20[2]
F	A5	DQ16	DQ17	V_{SSQ}					V_{SSQ}	DQ7	DQ6	QVLD
G	A8	A6	A7	V_{DD}					V_{DD}	A2	A1	A0
H	B2	A9	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A4	A3
J	DK0	DK0#	V_{DD}	V_{DD}					V_{DD}	V_{DD}	B0	CK
K	DK1	DK1#	V_{DD}	V_{DD}					V_{DD}	V_{DD}	B1	CK#
L	REF#	CS#	V_{SS}	V_{SS}					V_{SS}	V_{SS}	A14	A13
M	WE#	A16	A17	V_{DD}					V_{DD}	A12	A11	A10
N	A18	DQ24	DQ25	V_{SSQ}					V_{SSQ}	DQ35	DQ34	A19
P	A15	DQ22	DQ23	V_{DDQ}					V_{DDQ}	DQ33	DQ32	DM
R	V_{SS}	QK1	QK1#	V_{SSQ}					V_{SSQ}	DQ31	DQ30	V_{SS}
T	V_{TT}	DQ20	DQ21	V_{DDQ}					V_{DDQ}	DQ29	DQ28	V_{TT}
U	V_{DD}	DQ18	DQ19	V_{SSQ}					V_{SSQ}	DQ27	DQ26	V_{DD}
V	V_{REF}	ZQ	V_{EXT}	V_{SS}					V_{SS}	V_{EXT}	TDO	TDI

Notes:
1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.

Table 4: Ball Descriptions

Symbol	Type	Description
A0–A21	Input	**Address inputs:** A0–A21 define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK.
BA0–BA2	Input	**Bank address inputs:** Select to which internal bank a command is being applied.
CK, CK#	Input	**Input clock:** CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	**Chip select:** CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
DK, DK#	Input	**Input data clock:** DK and DK# are the differential input data clocks. All input data is referenced to both edges of DK. DK# is ideally 180 degrees out of phase with DK. For the x36 device, DQ0–DQ17 are referenced to DK0 and DK0# and DQ18–DQ35 are referenced to DK1 and DK1#. For the x9 and x18 devices, all DQs are referenced to DK and DK#. All DK*x* and DK*x*# pins must always be supplied to the device.

Table 4: Ball Descriptions (Continued)

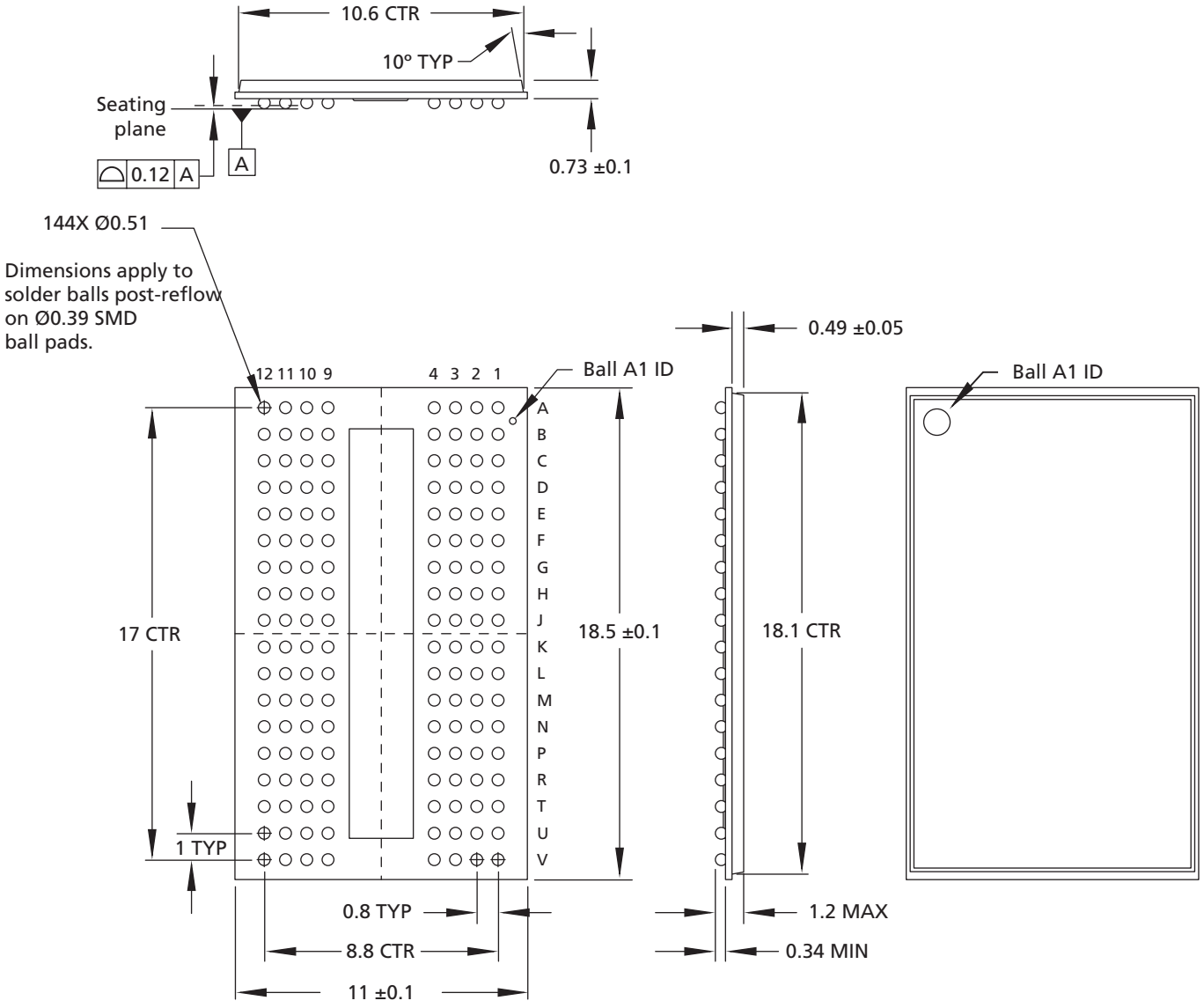
Symbol	Type	Description
DM	Input	**Input data mask:** The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM is sampled on both edges of DK (DK1 for the x36 configuration). Tie signal to ground if not used.
TCK	Input	**IEEE 1149.1 clock input:** This ball must be tied to V_{ss} if the JTAG function is not used.
TMS, TDI	Input	**IEEE 1149.1 test inputs:** These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	**Command inputs:** Sampled at the positive edge of CK, WE# and REF# define (together with CS#) the command to be executed.
DQ0–DQ35	I/O	**Data input:** The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK*x*. During WRITE commands, the data is sampled at both edges of DK.
QK*x*, QK*x*#	Output	**Output data clocks:** QK*x* and QK*x*# are opposite polarity, output data clocks. They are free-running, and during READs, are edge-aligned with data output from the RLDRAM. QK*x*# is ideally 180 degrees out of phase with QK*x*. For the x36 device, QK0 and QK0# are aligned with DQ0–DQ17, and QK1 and QK1# are aligned with DQ18–DQ35. For the x18 device, QK0 and QK0# are aligned with DQ0–DQ8, while QK1 and QK1# are aligned with Q9–Q17. For the x9 device, all DQs are aligned with QK0 and QK0#.
QVLD	Output	**Data valid:** The QVLD pin indicates valid output data. QVLD is edge-aligned with QK*x* and QK*x*#.
TDO	Output	**IEEE 1149.1 test output:** JTAG output. This ball may be left as no connect if the JTAG function is not used.
ZQ	Reference	**External impedance (25–60Ω):** This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 × RQ, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode. Connecting ZQ to V_{DD} invokes the maximum impedance mode. Refer to Mode Register Definition in Nonmultiplexed Address Mode to activate this function.
V_{DD}	Supply	**Power supply:** Nominally, 1.8V. See DC Electrical Characteristics and Operating Conditions for range.
V_{ddq}	Supply	**DQ power supply:** Nominally, 1.5V or 1.8V. Isolated on the device for improved noise immunity. See DC Electrical Characteristics and Operating Conditions for range.
V_{EXT}	Supply	**Power supply:** Nominally, 2.5V. See DC Electrical Characteristics and Operating Conditions for range.
V_{ref}	Supply	**Input reference voltage:** Nominally $V_{ddq}/2$. Provides a reference voltage for the input buffers.
V_{ss}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
V_{tt}	Supply	**Power supply:** Isolated termination supply. Nominally, $V_{ddq}/2$. See DC Electrical Characteristics and Operating Conditions for range.
A22	–	**Reserved for future use:** This signal is not connected and may be connected to ground.

Table 4: Ball Descriptions (Continued)

Symbol	Type	Description
DNU	–	**Do not use:** These balls may be connected to ground. Note that if ODT is enabled on Rev. A die, these pins will be connected to V_{tt}. The DNU pins are High-Z on Rev. B die when ODT is enabled.
NF	–	**No function:** These balls can be connected to ground.

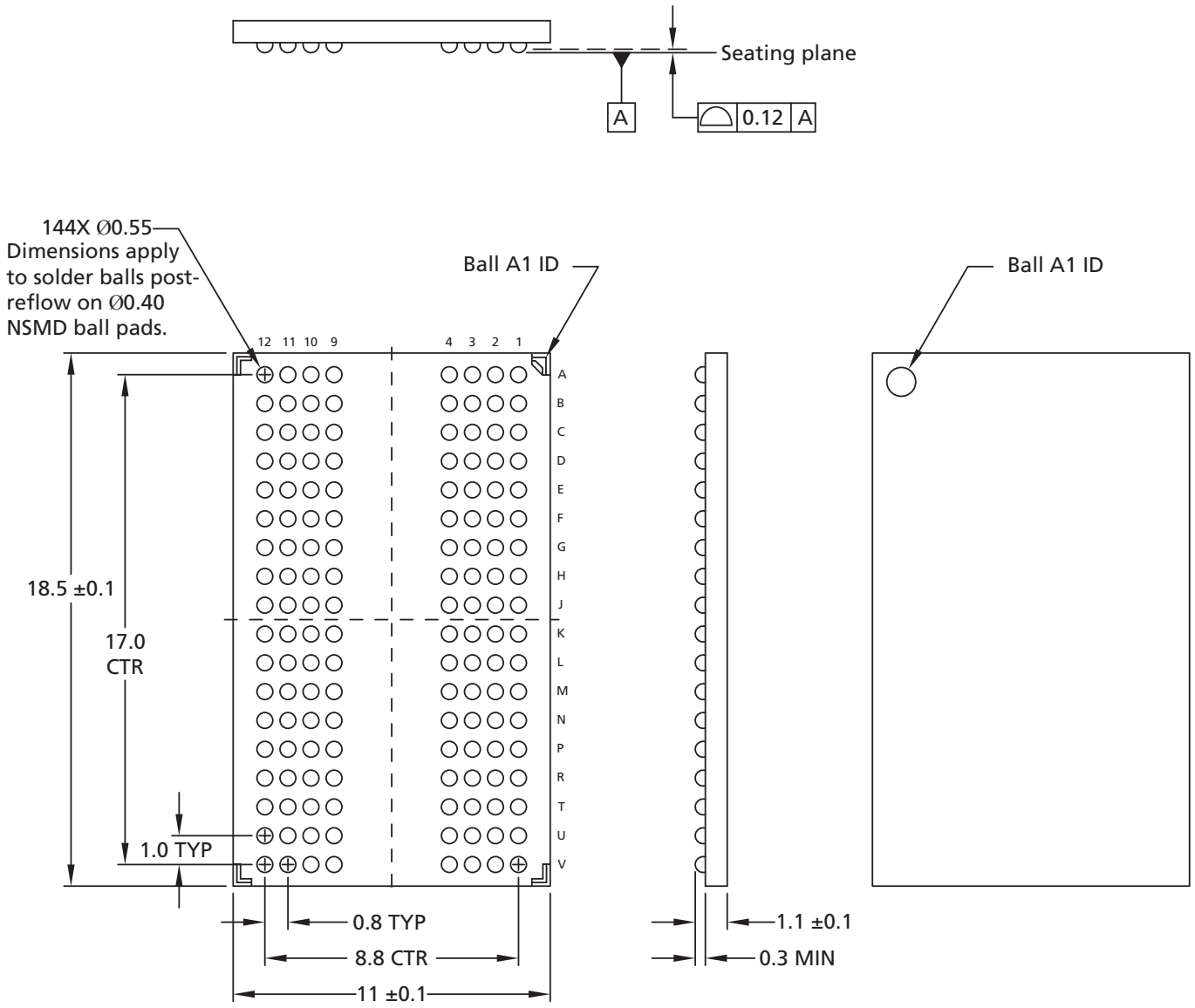
Package Dimensions

Figure 6: 144-Ball µBGA



Notes:
1. All dimensions are in millimeters.
2. Solder Ball Material :
   SAC305 (96.5% Sn, 3% Ag, 0.5% Cu) or
   Eutectic (62% Sn, 36% Pb, 2% Ag)

Figure 7: 144-Ball FBGA



Notes:
1. All dimensions are in millimeters.
2. Solder Ball Material :
   SAC302 (96.8% Sn, 3% Ag, 0.2% Cu) or
   Eutectic (62% Sn, 36% Pb, 2% Ag)

Electrical Specifications – I_{DD}

Table 5: I_{DD} Operating Conditions and Maximum Limits – Rev. A

Description	Condition	Symbol	-18	-25E	-25	-33	Units
Standby current	tCK = idle; All banks idle; No inputs toggling	I_{SB1} (V_{DD}) x9/x18	55	53	48	48	mA
		I_{SB1} (V_{DD}) x36	55	53	48	48	
		I_{SB1} (V_{EXT})	5	5	5	5	
Active standby current	CS# = 1; No commands; Bank address incremented and half address/data change once every four clock cycles	I_{SB2} (V_{DD}) x9/x18	365	293	288	233	mA
		I_{SB2} (V_{DD}) x36	365	293	288	233	
		I_{SB2} (V_{EXT})	5	5	5	5	
Operational current	BL = 2; Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD1} (V_{DD}) x9/x18	465	380	348	305	mA
		I_{DD1} (V_{DD}) x36	485	400	374	343	
		I_{DD1} (V_{EXT})	15	15	15	13	
Operational current	BL = 4; Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD2} (V_{DD}) x9/x18	475	400	362	319	mA
		I_{DD2} (V_{DD}) x36	510	425	418	389	
		I_{DD2} (V_{EXT})	15	15	15	13	
Operational current	BL = 8; Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD3} (V_{DD}) x9/x18	505	430	408	368	mA
		I_{DD3} (V_{DD}) x36	625	540	460	425	
		I_{DD3} (V_{EXT})	20	20	20	18	
Burst refresh current	Eight bank cyclic refresh; Continuous address/data; Command bus remains in refresh for all eight banks	I_{REF1} (V_{DD}) x9/x18	995	790	785	615	mA
		I_{REF1} (V_{DD}) x36	995	915	785	615	
		I_{REF1} (V_{EXT})	80	80	80	70	
Distributed refresh current	Single bank refresh; Sequential bank access; Half address transitions once every tRC; Continuous data	I_{REF2} (V_{DD}) x9/x18	425	330	325	267	mA
		I_{REF2} (V_{DD}) x36	425	390	326	281	
		I_{REF2} (V_{EXT})	20	20	20	18	
Operating burst write current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous WRITE	I_{DD2W} (V_{DD}) x9/x18	1335	980	970	819	mA
		I_{DD2W} (V_{DD}) x36	1545	1,105	1,100	914	
		I_{DD2W} (V_{EXT})	50	50	50	40	
Operating burst write current example	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DD4W} (V_{DD}) x9/x18	985	785	779	609	mA
		I_{DD4W} (V_{DD}) x36	1185	887	882	790	
		I_{DD4W} (V_{EXT})	30	30	30	25	

Table 5: I_{DD} Operating Conditions and Maximum Limits – Rev. A (Continued)

Description	Condition	Symbol	-18	-25E	-25	-33	Units
Operating burst write current example	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DD8W} (V_{DD}) x9/x18	770	675	668	525	mA
		I_{DD8W} (V_{DD}) x36	1095	755	750	580	
		I_{DD8W} (V_{EXT})	30	30	30	25	
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous READ	I_{DD2R} (V_{DD}) x9/x18	1225	940	935	735	mA
		I_{DD2R} (V_{DD}) x36	1270	995	990	795	
		I_{DD2R} (V_{EXT})	50	50	50	40	
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous READ	I_{DD4R} (V_{DD}) x9/x18	860	685	680	525	mA
		I_{DD4R} (V_{DD}) x36	920	735	730	660	
		I_{DD4R} (V_{EXT})	30	30	30	25	
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous READ	I_{DD8R} (V_{DD}) x9/x18	655	575	570	450	mA
		I_{DD8R} (V_{DD}) x36	855	665	660	505	
		I_{DD8R} (V_{EXT})	30	30	30	25	

Table 6: I_{DD} Operating Conditions and Maximum Limits – Rev. B

Description	Condition	Symbol	-18	-25E	-25	-33	Units
Standby current	^{t}CK = idle; All banks idle; No inputs toggling	I_{SB1} (V_{DD}) x9/x18	55	55	55	55	mA
		I_{SB1} (V_{DD}) x36	55	55	55	55	
		I_{SB1} (V_{EXT})	5	5	5	5	
Active standby current	CS# = 1; No commands; Bank address incremented and half address/data change once every four clock cycles	I_{SB2} (V_{DD}) x9/x18	250	215	215	190	mA
		I_{SB2} (V_{DD}) x36	250	215	215	190	
		I_{SB2} (V_{EXT})	5	5	5	5	
Operational current	BL = 2; Sequential bank access; Bank transitions once every ^{t}RC; Half address transitions once every ^{t}RC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD1} (V_{DD}) x9/x18	310	285	260	225	mA
		I_{DD1} (V_{DD}) x36	320	295	270	230	
		I_{DD1} (V_{EXT})	10	10	10	10	
Operational current	BL = 4; Sequential bank access; Bank transitions once every ^{t}RC; Half address transitions once every ^{t}RC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD2} (V_{DD}) x9/x18	315	290	260	220	mA
		I_{DD2} (V_{DD}) x36	330	305	275	230	
		I_{DD2} (V_{EXT})	10	10	10	10	
Operational current	BL = 8; Sequential bank access; Bank transitions once every ^{t}RC; Half address transitions once every ^{t}RC; Read followed by write sequence; Continuous data during WRITE commands	I_{DD3} (V_{DD}) x9/x18	330	305	275	230	mA
		I_{DD3} (V_{DD}) x36	390	365	320	265	
		I_{DD3} (V_{EXT})	15	15	15	15	
Burst refresh current	Eight bank cyclic refresh; Continuous address/data; Command bus remains in refresh for all eight banks	I_{REF1} (V_{DD}) x9/x18	660	540	530	430	mA
		I_{REF1} (V_{DD}) x36	670	545	535	435	
		I_{REF1} (V_{EXT})	45	30	30	25	
Distributed refresh current	Single bank refresh; Sequential bank access; Half address transitions once every ^{t}RC; Continuous data	I_{REF2} (V_{DD}) x9/x18	295	265	250	215	mA
		I_{REF2} (V_{DD}) x36	295	265	250	215	
		I_{REF2} (V_{EXT})	10	10	10	10	
Operating burst write current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous WRITE	I_{DD2W} (V_{DD}) x9/x18	830	655	655	530	mA
		I_{DD2W} (V_{DD}) x36	885	700	700	565	
		I_{DD2W} (V_{EXT})	40	35	35	30	
Operating burst write current example	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DD4W} (V_{DD}) x9/x18	580	465	465	385	mA
		I_{DD4W} (V_{DD}) x36	635	510	510	420	
		I_{DD4W} (V_{EXT})	25	20	20	20	

Table 6: I_{DD} Operating Conditions and Maximum Limits – Rev. B (Continued)

Description	Condition	Symbol	-18	-25E	-25	-33	Units
Operating burst write current example	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous WRITE	I_{DD8W} (V_{DD}) x9/x18	445	370	370	305	mA
		I_{DD8W} (V_{DD}) x36	560	455	455	375	
		I_{DD8W} (V_{EXT})	25	20	20	20	
Operating burst read current example	BL = 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous READ	I_{DD2R} (V_{DD}) x9/x18	805	640	640	515	mA
		I_{DD2R} (V_{DD}) x36	850	675	675	540	
		I_{DD2R} (V_{EXT})	40	35	35	30	
Operating burst read current example	BL = 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous READ	I_{DD4R} (V_{DD}) x9/x18	545	440	440	365	mA
		I_{DD4R} (V_{DD}) x36	590	475	475	390	
		I_{DD4R} (V_{EXT})	25	20	20	20	
Operating burst read current example	BL = 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous READ	I_{DD8R} (V_{DD}) x9/x18	410	335	335	280	mA
		I_{DD8R} (V_{DD}) x36	525	425	425	350	
		I_{DD8R} (V_{EXT})	25	20	20	20	

Notes:
1. I_{DD} specifications are tested after the device is properly initialized. +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, +2.38V ≤ V_{EXT} ≤ +2.63V, +1.4V ≤ V_{DDQ} ≤ V_{DD}, V_{REF} = V_{DDQ}/2.
2. ^{t}CK = ^{t}DK = MIN, ^{t}RC = MIN.
3. Input slew rate is specified in the Input AC Logic Levels table.
4. Definitions for I_{DD} conditions:
   - LOW = V_{IN} ≤ $V_{IL(AC)}$ MAX.
   - HIGH = V_{IN} ≥ $V_{IH(AC)}$ MIN.
   - Stable = Inputs remain at a HIGH or LOW level.
   - Floating = Inputs at V_{REF} = V_{DDQ}/2.
   - Continuous data = Half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
   - Continuous address = Half the address signals changing between HIGH and LOW every clock cycle (once per clock).
   - Sequential bank access = Bank address increments by one every ^{t}RC.
   - Cyclic bank access = Bank address increments by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
6. I_{DD} parameters are specified with ODT disabled.
7. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
8. I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Parameter	Min	Max	Units
I/O voltage	–0.3	V_{DDQ} + 0.3	V
Voltage on V_{EXT} supply relative to V_{SS}	–0.3	+2.8	V
Voltage on V_{DD} supply relative to V_{SS}	–0.3	+2.1	V
Voltage on V_{DDQ} supply relative to V_{SS}	–0.3	+2.1	V

AC and DC Operating Conditions

Table 8: DC Electrical Characteristics and Operating Conditions

Note 1 applies to the entire table; Unless otherwise noted: +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V

Description	Conditions	Symbol	Min	Max	Units	Notes
Supply voltage	–	V_{EXT}	2.38	2.63	V	
Supply voltage	–	V_{DD}	1.7	1.9	V	2
Isolated output buffer supply	–	V_{DDQ}	1.4	V_{DD}	V	2, 3
Reference voltage	–	V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	4, 5, 6
Termination voltage	–	V_{TT}	0.95 × V_{REF}	1.05 × V_{REF}	V	7, 8
Input high (logic 1) voltage	–	V_{IH}	V_{REF} + 0.1	V_{DDQ} + 0.3	V	2
Input low (logic 0) voltage	–	V_{IL}	V_{SSQ} - 0.3	V_{REF} - 0.1	V	2
Output high current	V_{OH} = V_{DDQ}/2	I_{OH}	(V_{DDQ}/2)/(1.15 × RQ/5)	(V_{DDQ}/2)/(0.85 × RQ/5)	A	9, 10, 11
Output low current	V_{OL} = V_{DDQ}/2	I_{OL}	(V_{DDQ}/2)/(1.15 × RQ/5)	(V_{DDQ}/2)/(0.85 × RQ/5)	A	9, 10, 11
Clock input leakage current	0V ≤ V_{IN} ≤ V_{DD}	I_{LC}	–5	5	µA	
Input leakage current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	–5	5	µA	
Output leakage current	0V ≤ V_{IN} ≤ V_{DDQ}	I_{LO}	–5	5	µA	
Reference voltage current	–	I_{REF}	–5	5	µA	

Notes:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH(AC)}$ ≤ V_{DD} + 0.7V for t ≤ $^tCK/2$. Undershoot: $V_{IL(AC)}$ ≥ –0.5V for t ≤ $^tCK/2$. During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals may not have pulse widths less than $^tCK/2$ or operate at frequencies exceeding ^tCK (MAX).
3. V_{DDQ} can be set to a nominal 1.5V ± 0.1V or 1.8V ± 0.1V supply.
4. Typically the value of V_{REF} is expected to be 0.5 x V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
5. Peak-to-peak AC noise on V_{REF} must not exceed ±2% $V_{REF(DC)}$.
6. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2% of the DC value. Thus, from V_{DDQ}/2, V_{REF} is allowed ±2% V_{DDQ}/2 for DC error and an additional ±2% V_{DDQ}/2 for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. On-die termination may be selected using mode register bit 9 (see the Mode Register Definition in Nonmultiplexed Address Mode figure). A resistance R_{TT} from each data input signal to the nearest V_{TT} can be enabled. R_{TT} = 125–185Ω at 95°C T_C.
9. I_{OH} and I_{OL} are defined as absolute values and are measured at V_{DDQ}/2. I_{OH} flows from the device, I_{OL} flows into the device.
10. If MRS bit A8 is 0, use RQ = 250Ω in the equation in lieu of presence of an external impedance matched resistor.
11. For V_{O0L} and V_{OH}, refer to the RLDRAM 2 HSPICE or IBIS driver models.

Table 9: Input AC Logic Levels

Notes 1–3 apply to entire table; Unless otherwise noted: +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V

Description	Symbol	Min	Max	Units
Input high (logic 1) voltage	V_{IH}	V_{REF} + 0.2	–	V
Input low (logic 0) voltage	V_{IL}	–	V_{REF} - 0.2	V

Notes:
1. All voltages referenced to V_{SS} (GND).
2. The AC and DC input level specifications are as defined in the HSTL standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
3. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$. See illustration below:

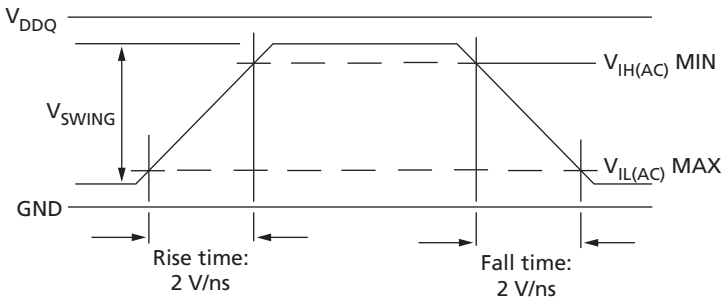


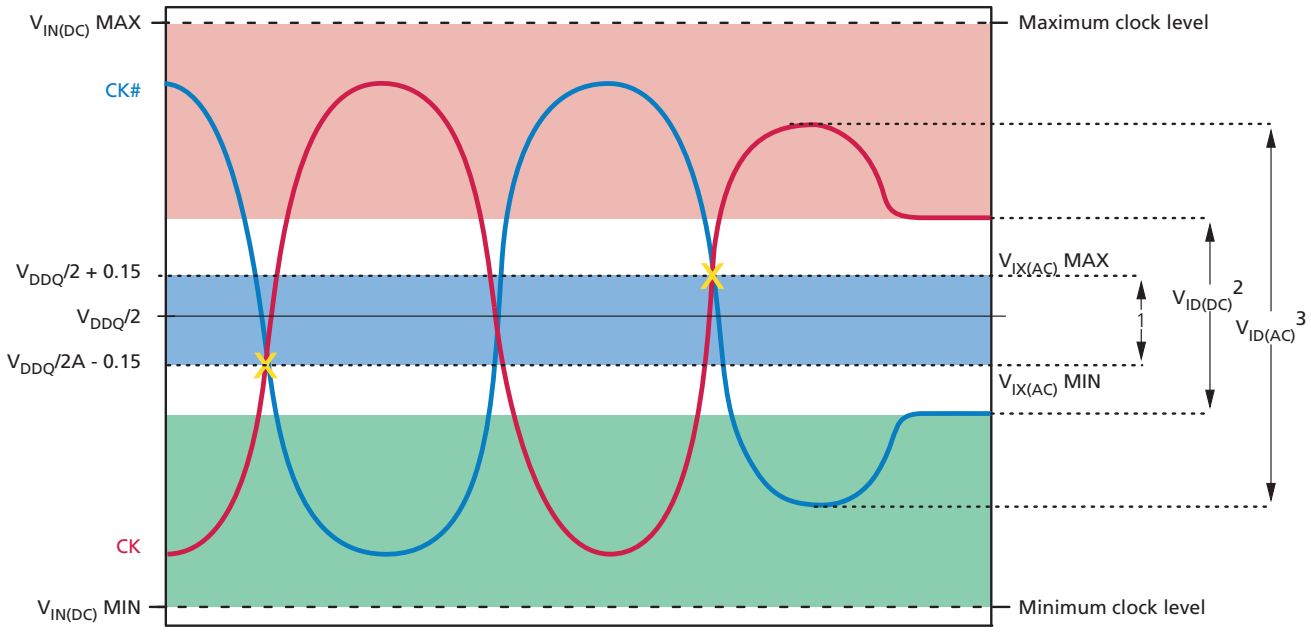
Table 10: Differential Input Clock Operating Conditions

Notes 1–4 apply to the entire table; Unless otherwise noted: +0°C ≤ T_C≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input voltage level: CK and CK#	$V_{IN(DC)}$	–0.3	V_{DDQ} + 0.3	V	
Clock input differential voltage: CK and CK#	$V_{ID(DC)}$	0.2	V_{DDQ} + 0.6	V	5
Clock input differential voltage: CK and CK#	$V_{ID(AC)}$	0.4	V_{DDQ} + 0.6	V	5
Clock input crossing point voltage: CK and CK#	$V_{IX(AC)}$	V_{DDQ}/2 - 0.15	V_{DDQ}/2 + 0.15	V	6

Notes:
1. DK*x* and DK*x*# have the same requirements as CK and CK#.
2. All voltages referenced to V_{SS} (GND).
3. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is V_{REF}.
4. CK and CK# input slew rate must be ≥2 V/ns (≥4 V/ns if measured differentially).
5. V_{id} is the magnitude of the difference between the input level on CK and the input level on CK#.
6. The value of V_{IX} is expected to equal V_{DDQ}/2 of the transmitting device and must track variations in the DC level of the same.

Figure 8: Clock Input



Notes:
1. CK and CK# must cross within this region.
2. CK and CK# must meet at least $V_{ID(DC)}$ MIN when static and centered around V_{ddq}/2.
3. Minimum peak-to-peak swing.
4. It is a violation to tristate CK and CK# after the part is initialized.