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Features

- Meets requirements of GR-253-CORE for SONET Stratum 3 and SONET minimum clock
- Meets requirements of GR-1244-CORE Stratum 3
- Meets requirements of G.813 Option 1 and Option 2 for SDH Equipment Clocks (SEC) with external jitter attenuator
- Provides OC-3/STM-1, DS3, E3, 19.44 MHz, DS2, E1, T1, 8 kHz and ST-BUS clock outputs
- Accepts reference inputs from two independent sources
- Selectable 1.544 MHz, 2.048 MHz, 19.44 MHz or 8kHz input reference frequencies
- Holdover accuracy of 0.02 ppm
- Adjustable output clock phase supporting master-slave arrangements
- Hardware or microprocessor control (8 bit microprocessor interface)
- 3.3 V supply
- JTAG boundary scan

January 2005

Ordering Information

MT90401AB	80 Pin LQFP	Trays
MT90401AB1	80 Pin LQFP*	Trays

*Pb Free Matte Tin

-40°C to +85°C

Applications

- SONET/SDH Add/Drop multiplexers
- SONET/SDH uplinks
- Integrated access devices
- ATM edge switches

Description

The MT90401 is a digital phase locked loop (DPLL) that is designed to synchronize SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) networking equipment. The MT90401 is used to ensure that the timing of outgoing signals remains within the limits specified by Telcordia, ANSI and the ITU during normal operation and in the presence of disturbances on the incoming synchronization signals.

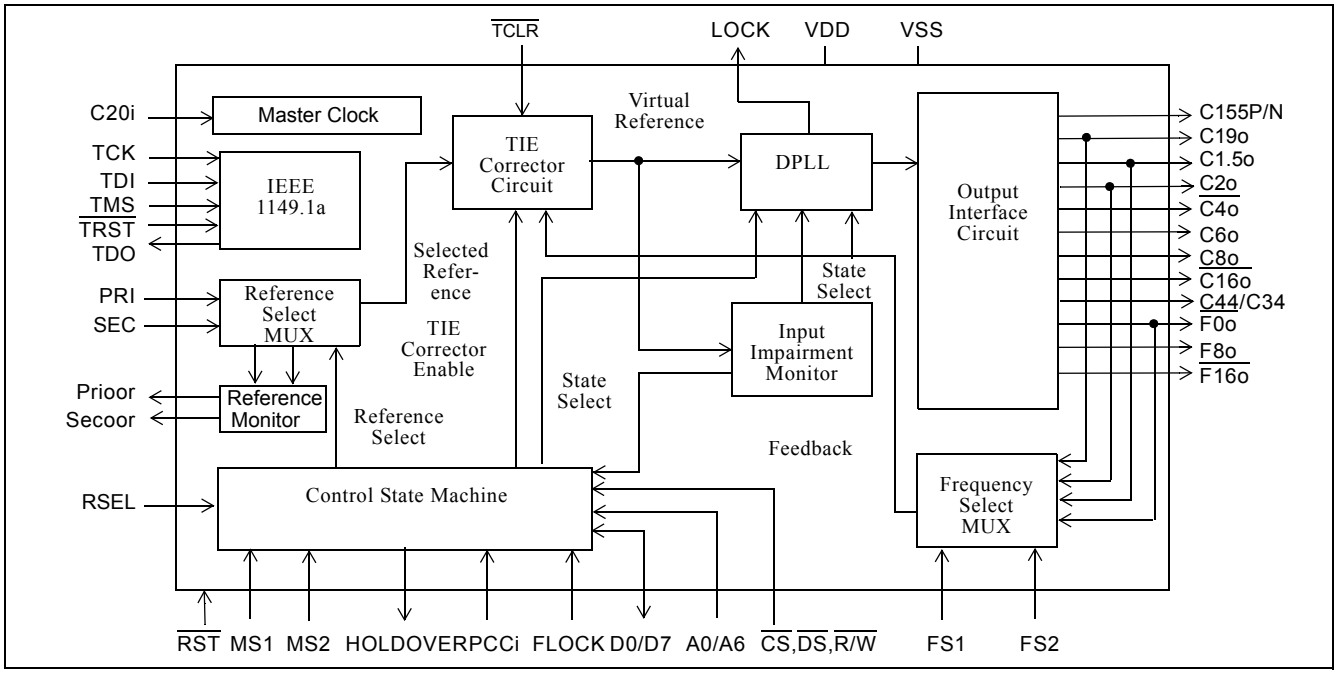

Figure 1 - Functional Block Diagram

The MT90401 can operate in free-run, locked or holdover mode. The loop filter corner frequency can be selected to suit SONET applications or to suit SDH applications. The MT90401 uses an external 20 MHz oscillator as its master clock and it does not require external loop filter components.

In Hardware Mode, the MT90401 can be controlled and monitored via external pins. In Microport Mode, a microprocessor can be used for more comprehensive control and monitoring.

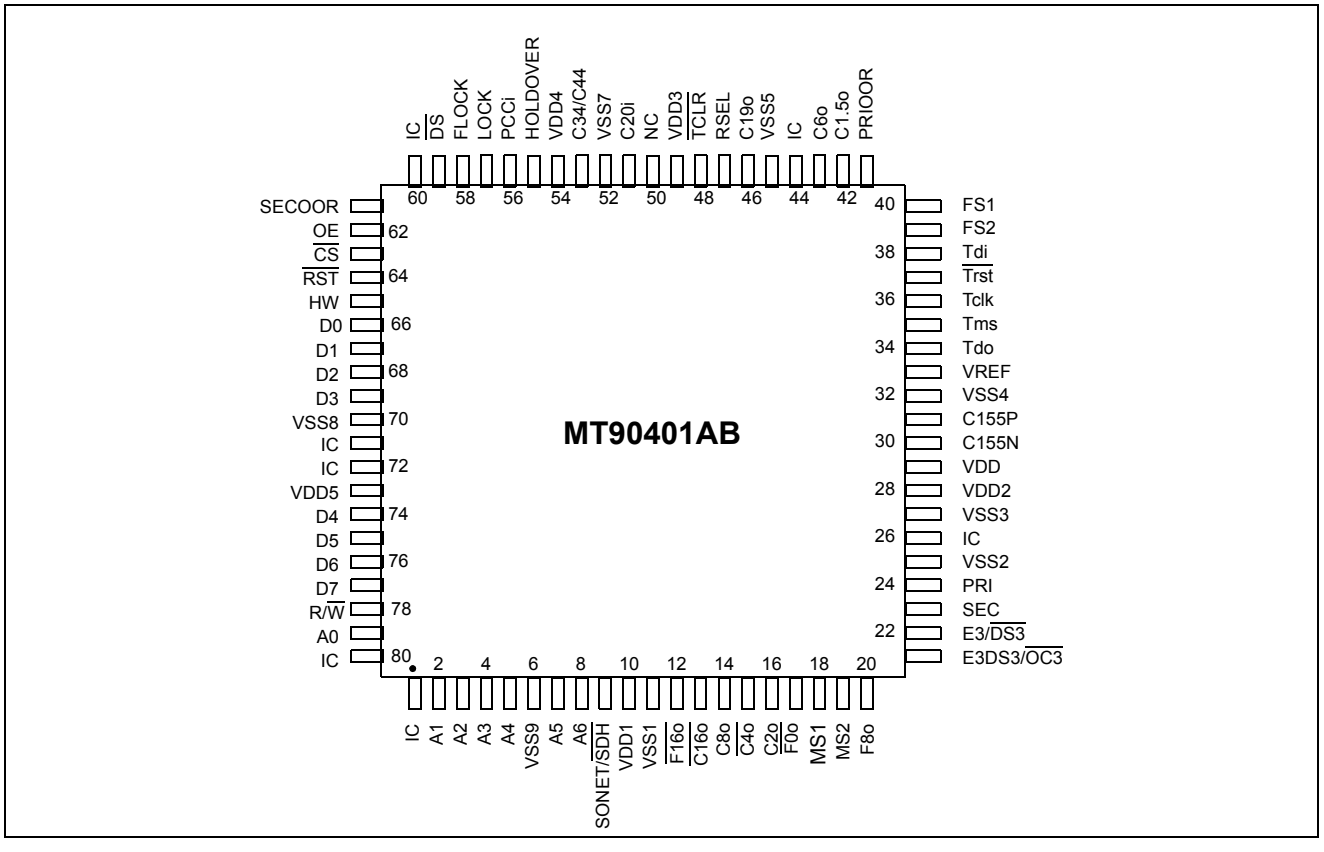

Figure 2 - Pin Connections 80 Pin LQFP for MT90401

Pin Description

Pin #	Name	Description
1	IC	**Internal Connection**. Leave unconnected.
2-5	A1 - A4	**Address 1 to 4 (5 V tolerant Inputs).** Address inputs for the parallel processor interface.
6	V_{SS9}	**Digital ground.** 0 Volts
7, 8	A5, A6	**Address 5, to 6 (5 V tolerant Input).** Address inputs for the parallel processor interface.
9	SONET/$\overline{SDH}$	**SONET/$\overline{SDH}$ (Input).** In hardware mode set this pin high to have a loop filter corner frequency of 70 millihertz and limit the phase slope to 885 ns per second. Set this pin low to have a corner frequency of approximately 1.1 hertz and limit the phase slope to 53 ns per 1.326 ms. This pin performs no function if the device is not in hardware mode.
10	V_{DD1}	**Positive Power Supply.** Digital supply.
11	V_{SS1}	**Digital ground.** 0 Volts
12	$\overline{F16o}$	**Frame Pulse ST-BUS 8.192 Mb/s (CMOS Output).** This is an 8kHz 61ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s.
13	$\overline{C16o}$	**Clock 16.384 MHz (CMOS Output).** This output is used for ST-BUS operation with a 16.384 MHz clock.
14	C8o	**Clock 8.192 MHz (CMOS Output).** This output is used for ST-BUS operation at 8.192 Mb/s.
15	$\overline{C4o}$	**Clock 4.096 MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s.
16	C2o	**Clock 2.048 MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048 Mb/s.
17	$\overline{F0o}$	**Frame Pulse ST-BUS 2.048 Mb/s (CMOS Output).** This is an 8 kHz 244 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s.
18	MS1	**Mode/Control Select 1 (Input).** This input, together with MS2, determines the state (Normal, Holdover, or Freerun) of operation. See Table 3 on page 15. The logic level at this input is gated in by the rising edge of F8o. This pin performs no function if the device is not in hardware mode.
19	MS2	**Mode/Control Select 2 (Input).** This input, together with MS1, determines the state (Normal, Holdover or Freerun) of operation. See Table 3 on page 15. The logic level at this input is gated in by the rising edge of F8o. This pin performs no function if the device is not in hardware mode.
20	F8o	**Frame Pulse Generic (CMOS Output).** This is an 8 kHz 122 ns active high framing pulse, which marks the beginning of a TDM frame. This is typically used for TDM streams operating at 8.192 Mb/s.
21	E3DS3/$\overline{OC3}$	**E3DS3 or OC-3 Selection (Input).** In Hardware Mode a low on this pin enables the differential 155.52 MHz output clock on the C155N/C155P pins; this will also cause the C34/C44 pin to output its nominal clock frequency divided by 4. In Hardware Mode, a high on this pin disables the differential 155.52 MHz output clock on the C155N/C155P pins; this will also cause the C34/C44 pin to output its nominal clock frequency. This pin performs no function if the device is not in Hardware Mode.

Pin Description (continued)

Pin #	Name	Description
22	E3/$\overline{DS3}$	**E3 or DS3 Selection (Input).** In Hardware Mode a low on this pin selects a clock rate of 44.736 MHz for the C34/C44 pin, while a high selects a clock rate of 34.368 MHz. This pin performs no function if the device is not in hardware mode.
23	SEC	**Secondary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) may be used. In hardware mode the selection of the input reference is based upon the MS1, MS2 and RSEL control inputs.
24	PRI	**Primary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) may be used. In hardware mode the selection of the input reference is based upon the MS1, MS2 and RSEL control inputs.
25	V_{SS2}	**Digital ground.** 0 Volts
26	IC	**Internal Connection.** Leave unconnected
27	V_{SS3}	**Analog ground.** 0 Volts
28	V_{DD2}	**Positive Analog Power Supply.** Analog supply.
29	V_{DD}	**Positive Power Supply.** Digital supply.
30 31	C155N, C155P	**LVDS 155.52 MHz (Output)).** Differential outputs generating a 155.52 MHz clock
32	V_{SS4}	**Digital ground.** 0 Volts
33	VREF	**LVDS Reference Voltage (Input).**
34	Tdo	**IEEE 1149.1a Test Data Output (Output).** If not used, this pin should be left unconnected.
35	Tms	**IEEE 1149.1a Test Mode Selection (Input)**. If not used, this pin should be pulled high.
36	Tclk	**IEEE 1149.1a Test Clock Signal (Input)**. If not used, this pin should be pulled high.
37	$\overline{Trst}$	**IEEE 1149.1a Reset Signal (Input).** If not used, this pin should be held low.
38	Tdi	**IEEE 1149.1a Test Data Input (Input).** If not used, this pin should be pulled high.
39	FS2	**Frequency Select 2 (Input).** This input, in conjunction with FS1, selects which of four possible frequencies (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) may be input to the PRI and SEC inputs. For more details see FS2 bit description in Table 6 - Control Register 1 (Address 00H - Read/Write).
40	FS1	**Frequency Select 1 (Input).** This input, in conjunction with FS2, selects which of four possible frequencies (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) may be input to the PRI and SEC inputs. For more details see FS1 bit description in Table 6 - Control Register 1 (Address 00H - Read/Write).
41	PRIOOR	**Primary Reference Out Of Range (CMOS Output).** A logic high at this pin indicates that the primary reference is off the PLL center frequency by more than 12 ppm. The measurement is done on a 1 second basis using a signal derived from the 20 MHz clock input on C20i. When the accuracy of the 20 MHz clock is ± 4.6 ppm, the effective out of range limits of the PRIOOR signal will be +16.6 ppm to -7.4 ppm or +7.4 ppm to -16.6 ppm.
42	C1.5o	**Clock 1.544 MHz (CMOS Output).** This output is used in T1 applications.
43	C6	**Clock 6.312 MHz (CMOS Output).** This output is used for DS2 or J2 applications.
44	IC	**Internal Connection.** Tie low for normal operation.

Pin Description (continued)

Pin #	Name	Description
45	V_{SS5}	**Digital ground.** 0 Volts
46	C19o	**Clock 19.44 MHz (CMOS Output).** This output is used in OC-N and STM-N applications.
47	RSEL	**Reference Source Select (Input).** A logic low selects the PRI (primary) reference source as the input reference signal and a logic high selects the SEC (secondary) input. The logic level at this input is gated in by the rising edge of F8o. For more details see RSEL bit description in Table 6 - Control Register 1 (Address 00H - Read/Write).
48	$\overline{\text{TCLR}}$	**TIE Circuit Clear (Input).** A logic low at this input clears the Time Interval Error (TIE) correction circuit resulting in a realignment of output phase with input phase. The $\overline{\text{TCLR}}$ pin should be held low for a minimum of 300 ns. When this pin is held low, the time interval error correction circuit is disabled.
49	V_{DD3}	**Positive Power Supply. Digital supply**.
50	NC	**No Connection.**
51	C20i	**20 MHz Clock Input (5 V tolerant Input).** This pin is the input for the master 20 MHz clock.
52	V_{SS7}	**Digital ground.** 0Volts
53	C34/C44	**Controlled Clock 34.368 MHz / Clock 44.736 MHz (CMOS Output).** This output clock is programmable to be either 34.368 MHz (for E3 applications) or 44.736 MHz (for DS3 applications). The output clock is controlled via control pins in Hardware Mode or control bits when the device is in Microport Mode. If the E3DS3/$\overline{\text{OC3}}$ control pin or control bit is high, the C34/C44 pin will output its nominal frequency. If the E3DS3/OC3 control pin or bit is low, the C34/C44 pin will output its nominal frequency divided by 4. (C8.5o/C11o)
54	V_{DD4}	**Positive Power Supply.** Digital supply.
55	HOLDOVER	**Holdover (CMOS Output).** This output goes high when the device is in holdover mode.
56	PCCi	**Phase Continuity Control Input (3 V Input).** The signal at this pin affects the state changes between Primary Holdover Mode and Primary Normal Mode and Primary Holdover Mode and Secondary Normal Mode. The logic level at this input is gated by the rising edge of F8o. See Figure 12, “Control State Diagram” on page 21 for details.
57	LOCK	**Lock Indicator (CMOS Output).** This output goes high when the PLL is in frequency lock to the input reference.
58	FLOCK	**Fast Lock Mode (Input).** In hardware mode, hold this pin high to lock faster than normal to the input reference. This pin performs no function if the device is not in hardware mode. In Fast Lock Mode, the wander generation of the PLL is, of necessity, compromised.
59	$\overline{\text{DS}}$	**Data Strobe (5 V tolerant Input)**. This input is the active low data strobe of the Motorola processor interface.
60	IC	**Internal Connection.** Tie low for normal operation.
61	SECOOR	**Secondary Reference Out Of Capture Range (CMOS Output).** A logic high at this pin indicates that the secondary reference is off the PLL center frequency by more than 12 ppm. The measurement is done on a 1 second basis using a signal derived from the 20 MHz clock input on the C20i pin. When the accuracy of the 20 MHz clock is ± 4.6 ppm the effective out of range limits of the SECOOR signal will be +16.6 ppm to -7.4 ppm or +7.4 ppm to -16.6 ppm.

Pin Description (continued)

Pin #	Name	Description
62	OE	**Output Enable (Input)**. Tie high for normal operation. Tie low to force output clocks pins F16, F8, C16, C8, C4, C2 to a high impedance state.
63	$\overline{CS}$	**Chip Select (5 V tolerant Input)**. This active low input enables the non-multiplexed Motorola parallel microprocessor interface of the MT90401. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all bus I/O pins will be in a high impedance state.
64	$\overline{RST}$	**RESET (5 V tolerant Input).** This active low input puts the MT90401 in a reset condition. $\overline{RST}$ should be set to high for normal operation. The MT90401 should be reset after power-up and after the selected reference frequency is changed. The $\overline{RST}$ pin must be held low for a minimum of 1msec. to reset the device properly.
65	HW	**Hardware Mode (Input)**. If this pin is tied low, the device is in microport mode and is controlled via the microport. If it is tied high, the device is in hardware mode and is controlled via the control pins MS1, MS2, FS1, FS2, FLOCK and SONET/$\overline{SDH}$.
66-69	D0 - D3	**Data 0 to Data 3 (5 V tolerant Three-state I/O)**. These signals combined with D4-D7 form the bidirectional data bus of the parallel processor interface (D0 is the least significant bit).
70	V_{SS8}	**Digital ground.** 0 Volts.
71	IC	**Internal Connection.** Tie low for normal operation.
72	IC	**Internal Connection.** Tie low for normal operation.
73	V_{DD5}	**Positive Power Supply.** Digital supply.
74-77	D4 - D7	**Data 4 to Data 7 (5 V tolerant Three-state I/O).** These signals combined with D0-D3 form the bidirectional data bus of the parallel processor interface (D7 is the most significant bit).
78	R/$\overline{W}$	**Read/$\overline{\text{Write}}$ Select (5 V tolerant Input).** This input controls the direction of the data bus D[0:7] during a microprocessor access. When R/$\overline{W}$ is high, the parallel processor is reading data from the MT90401. When low, the parallel processor is writing data to the MT90401.
79	A0	**Address 0 (5 V tolerant Input).** Address input for the parallel processor interface. A0 is the least significant input.
80	IC	**Internal Connection.** Tie low for normal operation.

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1.0 Functional Description

The MT90401 is a SONET/SDH System Synchronizer, providing timing (clock) and synchronization (frame) signals to interface circuits for Digital Telecommunications Transmission links. Figure 1 is a functional block diagram which is described in the following sections.

1.1 Reference Select MUX Circuit

The MT90401 accepts two simultaneous reference input signals and operates on their falling edges. Either the primary reference (PRI) signal or the secondary reference (SEC) signal can be selected as input to the TIE Corrector Circuit. The selection is based on the Control, Mode and Reference Selection of the device. See Table 1 and Table 4.

1.2 Frequency Select MUX Circuit

The MT90401 operates with one of four possible input reference frequencies (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz). The frequency select inputs, FS1 and FS2, which come from pins in hardware mode and control bits in microport mode determine which of the four frequencies may be used at the reference inputs (PRI and SEC). Both inputs must have the same frequency applied to them. A reset ($\overline{RST}$) must be performed after every frequency select input change. See Table 1 - Input Frequency Selection.

FS2	FS1	Input Frequency
0	0	19.44 MHz See FS2 and FS1 bit description in Table 6 - Control Register 1 (Address 00H - Read/Write)
0	1	8 kHz
1	0	1.544 MHz
1	1	2.048 MHz

Table 1 - Frequency Selection

1.3 Time Interval Error (TIE) Corrector Circuit

The TIE corrector circuit, when enabled, prevents a step change in phase on the input reference signals (PRI or SEC) from causing a step change in phase at the input of the DPLL block of Figure 1.

During reference input rearrangement, such as during a switch from the primary reference (PRI) to the secondary reference (SEC), a step change in phase on the input signals will occur. A phase step at the input of the DPLL would lead to unacceptable phase changes in the output signal.

As shown in Figure 3, the TIE Corrector Circuit receives one of the two reference (PRI or SEC) signals, passes the signal through a programmable delay line, and uses this delayed signal as an internal virtual reference, which is input to the DPLL. Therefore, the virtual reference is a delayed version of the selected reference. During a switch from one reference to the other, the State Machine first changes the mode of the device from Normal to Holdover. In Holdover Mode, the DPLL no longer uses the virtual reference signal, but generates an accurate clock signal using storage techniques. The Compare Circuit then measures the phase delay between the current phase (feedback signal) and the phase of the new reference signal. This delay value is passed to the Programmable Delay Circuit (See Figure 3). The new virtual reference signal is now at the same phase position as the previous reference signal would have been if the reference switch had not taken place. The State Machine then returns the device to Normal Mode.

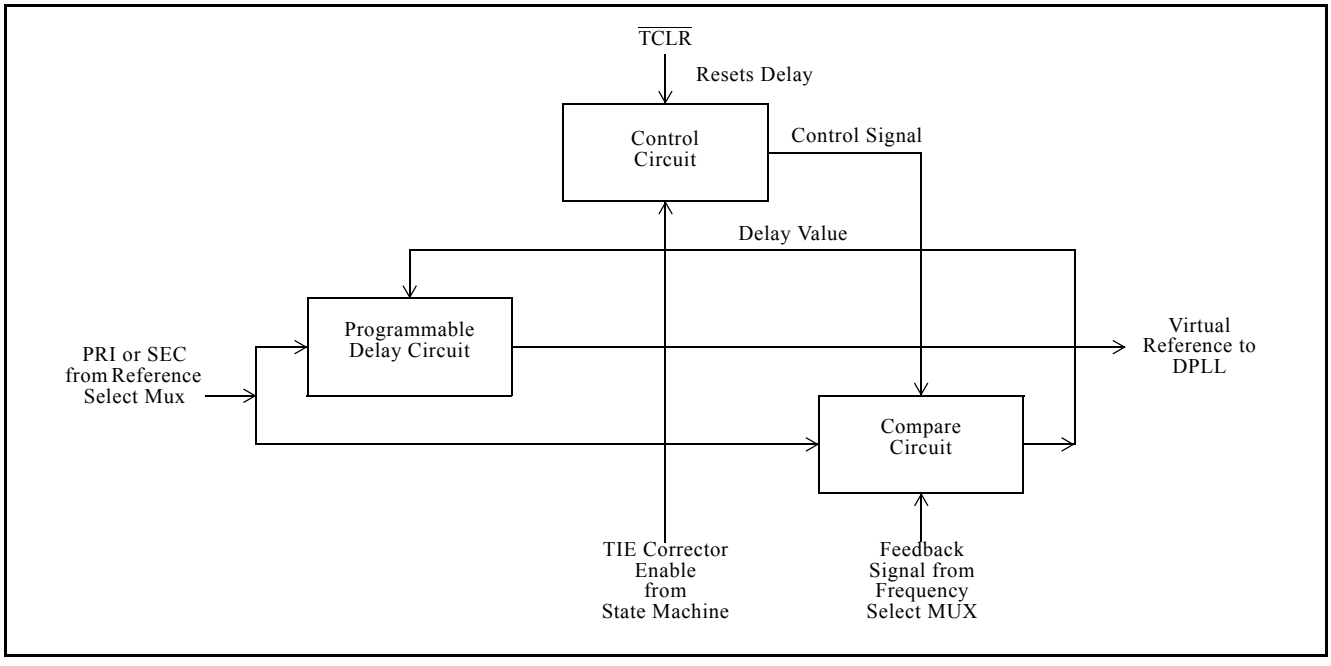

Figure 3 - TIE Corrector Circuit

The DPLL now uses the new virtual reference signal, and since no phase step took place at the input of the DPLL, no phase step occurs at the output of the DPLL. In other words, reference switching will not create a phase change at the input of the DPLL, or at the output of the DPLL.

Since internal delay circuitry maintains the alignment between the old virtual reference and the new virtual reference, a phase error may exist between the selected input reference signal and the output signal of the DPLL. This phase error is a function of the difference in phase between the two input reference signals during reference rearrangements. Each time a reference switch is made, the delay between input signal and output signal will change. The value of this delay is the accumulation of the error measured during each reference switch.

The programmable delay circuit can be reset to zero by applying a logic low pulse to the TIE Circuit Clear ($\overline{\text{TCLR}}$) pin. A minimum reset pulse width is 300 ns. This results in a phase realignment between the input reference signal and the output signal as shown in Figure 16. The speed of the phase alignment correction is limited to 885 ns/s in SONET mode and 53 ns per 1.326 ms in SDH mode, convergence is in the direction of least phase travel.

The state diagram of Figure 12 indicates the state changes for which the TIE Corrector Circuit is activated.

1.4 Digital Phase Lock Loop (DPLL)

As shown in Figure 4, the DPLL of the MT90401 consists of a Phase Detector, Phase Slope Limiter, Loop Filter, Digitally Controlled Oscillator, and a Control Circuit.

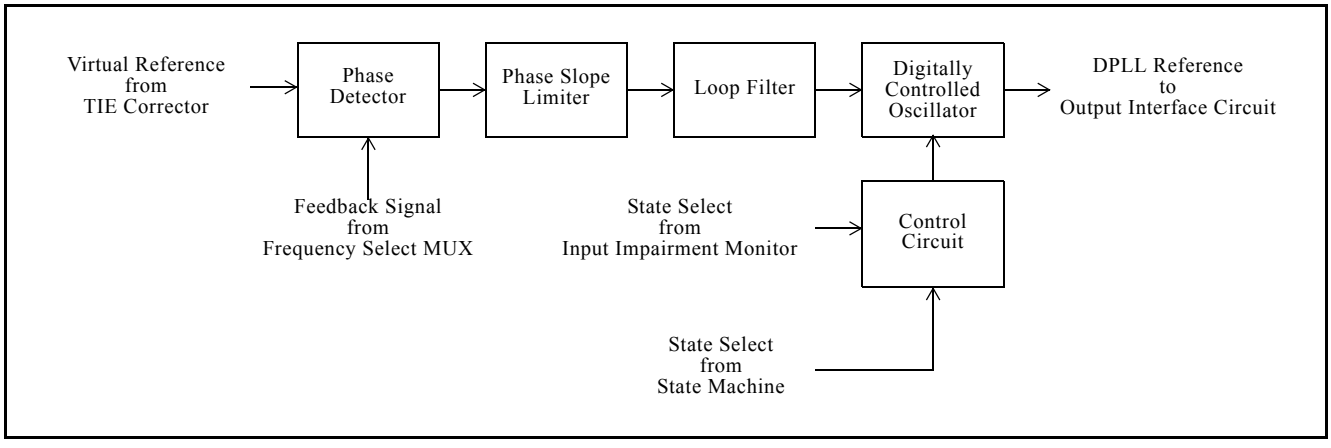

Figure 4 - DPLL Block Diagram

Phase Detector - the Phase Detector compares the virtual reference signal from the TIE Corrector circuit with the feedback signal from the Frequency Select MUX circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Phase Slope Limiter circuit. The Frequency Select MUX allows the proper feedback signal to be externally selected (e.g., 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz).

Phase Slope Limiter - the Phase Slope Limiter receives the error signal from the Phase Detector and ensures that the DPLL responds to all input transient conditions with a limited output phase slope. In SONET Mode the maximum output phase slope is limited to 885 ns/s as per Telcordia GR-253-CORE. In SDH Mode the maximum output phase slope is 53 ns per 1.326 ms.

Loop Filter - the Loop Filter is a low pass filter, that defines the network jitter and wander transfer requirements for all input reference frequencies (8 kHz, 1.544 MHz, 2.048 MHz, or 19.44 MHz). In SONET mode the loop filter has a cut-off frequency of 70 mHz to comply with Telcordia GR-253-CORE and GR-1244-CORE. In SDH mode the loop filter has a cut-off frequency of 1.1Hz to comply with ITU-T G.813 Option 1 and GR-1244-CORE.

Control Circuit - the Control Circuit uses status and control information from the State Machine and the Input Impairment Circuit to set the mode of the DPLL. The three possible modes are Normal, Holdover and Freerun.

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the MT90401.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover Mode, the DCO is free running at a frequency equal to the last locked frequency the DCO was generating while in Normal Mode. In order to improve accuracy of the Holdover Mode the actual frequency sample is taken 30 to 60 ms before switching into holdover.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the C20i 20 MHz source.

Telcordia GR-253-CORE requires that, during recovery from holdover, SONET clocks not change their output frequency at a rate faster than 2.9 ppm per second. In SONET Mode the MT90401 limits the rate of change of its output frequency (frequency slope) to less than 1.9ppm per second; this limit remains in place when the PLL is in Fast Lock Mode.

Lock Indicator - If the PLL is in frequency lock (frequency lock means the center frequency of the PLL is identical to the line frequency), and the input phase offset is small enough such that no phase slope limiting is exhibited, then the lock signal will be set high.

1.5 Output Interface Circuit

The output of the DCO (DPLL) is used by the Output Interface Circuit to provide the output signals shown in Figure 5. The Output Interface Circuit uses five Tapped Delay Lines in MT90401 followed by a T1 Divider Circuit, an E1 Divider Circuit, a DS2 Divider Circuit, and a x4/x8 PLL, to generate the required output signals.

Five tapped delay lines are used to generate 8.592 MHz, 11.184 MHz, 16.384 MHz, 12.352 MHz, 12.624 MHz and 19.44 MHz signals.

The E1 Divider Circuit uses the 16.384 MHz signal to generate four clock outputs and three frame pulse outputs. The C8o, $\overline{\text{C4o}}$ and C2o clocks are generated by simply dividing the $\overline{\text{C16o}}$ clock by two, four and eight respectively. These outputs have a nominal 50% duty cycle. The frame pulse outputs ($\overline{\text{F0o}}$, F8o, and $\overline{\text{F16o}}$) are generated directly from the C16 clock.

The T1 Divider Circuit uses the 12.352 MHz signal to generate C1.5o. This output has a nominal 50% duty cycle. The DS2 Divider Circuit uses the 12.624 MHz signal to generate the clock output C6o. This output has a nominal 50% duty cycle.

The 19.44 MHz signal is output on the C19o pin and it is multiplied by an internal PLL to generate the 155.52 MHz clock output on the C155P/N pins. The C155P/N clock has a nominal 50% duty cycle.

The 8.592 MHz and 11.184 MHz signals are multiplied by an internal PLL to generate the 34.368 MHz or 44.736 MHz clock output on the C34/C44 pin. If the internal PLL is dedicated to the C155P/N clock then the C34/C44 pin will output the 8.592 MHz or 11.184 MHz clocks. The 34.368 Mhz and 44.736 MHz clocks have a nominal 50% duty cycle. The duty cycles of the 8.592 MHz and 11.184 MHz signals are dependent on the duty cycle of the 20 MHz clock input to the C20i pin.

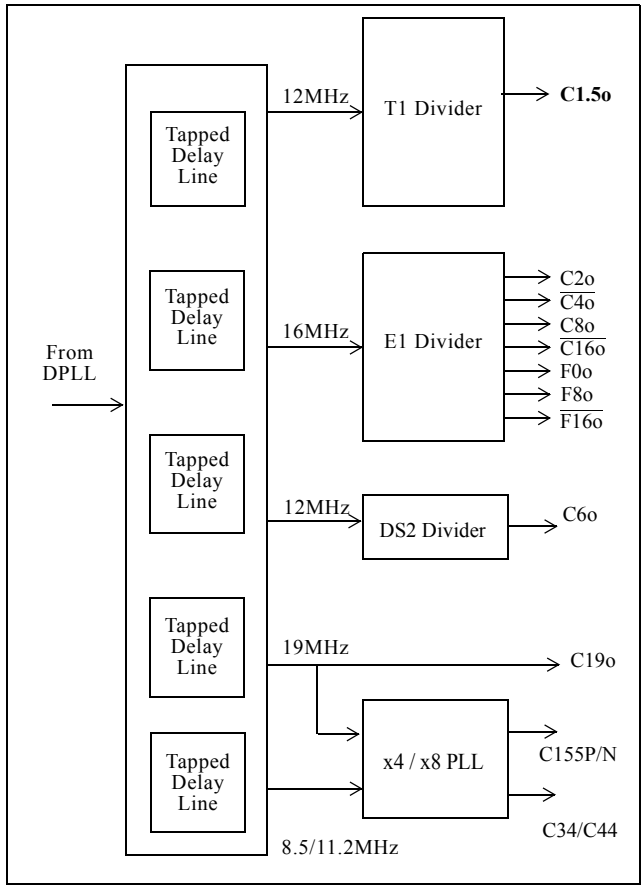

Figure 5 - Output Interface Circuit Block Diagram

The T1 and E1 signals are generated from a common DPLL signal. Consequently, all frame pulses and clock outputs are locked to one another for all operating states, and are also locked to the selected input reference in Normal Mode. See Figure 18.

All frame pulses and clock outputs have limited driving capability, and should be buffered when driving capacitive loads exceeding 30 pF.

1.6 Input Impairment Monitor

This circuit monitors the input signal to the DPLL and automatically enables the Auto-Holdover when the frequency of the incoming signal is outside the Auto-Holdover capture range. (See Performance Characteristics - Mode Switching). This includes a complete loss of incoming signal, or a large frequency shift in the incoming signal. When the incoming signal returns to normal, the DPLL is returned to Normal Mode with the output signal locked to the input signal. The holdover output signal in the MT90401 is based on the incoming signal 30 ms (minimum) to 60 ms prior to entering the Holdover Mode. The amount of phase drift while in holdover is negligible because the Holdover Mode is very accurate (i.e., 0.02 ppm). Consequently, the phase delay between the input and output after switching back to Normal Mode is preserved.

1.7 State Machine Control

An internal state machine can be enabled to control the TIE Corrector Circuit as shown in Figure 1. In hardware mode, control is based on the logic levels at the control inputs RSEL, MS1, MS2 and PCCi (See Figure 6). In Microport mode, control is based on the state of control bits RSEL, MS1 and MS2 and the PCCi pin. When switching from Primary Holdover to Primary Normal, the TIE Corrector Circuit is enabled when PCCi = 1, and disabled when PCCi = 0.

All state machine changes occur synchronously on the rising edge of F8o. See the Control and Mode of Operation section for full details.

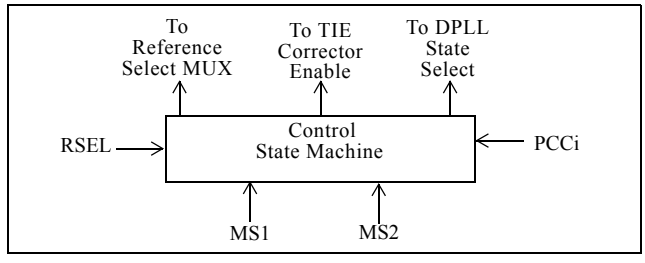

Figure 6 - Control State Machine Block Diagram

1.8 Master Clock

The MT90401 uses an external oscillator as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

2.0 Control and Mode of Operation

The MT90401 has three possible modes of operation, Normal, Holdover and Freerun.

In hardware mode the Mode/Control Select pins MS2 and MS1 select the mode and method of control as shown in Table 3.

RSEL	Input Reference
0	PRI
1	SEC

Table 2 - Input Reference Selection

MS2	MS1	Mode
0	0	NORMAL
0	1	HOLDOVER
1	0	FREERUN
1	1	Reserved

Table 3 - Operating Modes and States

The active reference input (PRI or SEC) is selected by the RSEL pin as shown in Table 2. Refer to Table 4 and Figure 12 for details of the state change sequences.

2.1 Normal Mode

Normal Mode is typically used when a slave clock source, synchronized to the network is required.

In Normal Mode, the MT90401 provides timing and frame synchronization signals, which are synchronized to one of two reference inputs (PRI or SEC). The input reference signal may have a nominal frequency of 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz.

The selection of input references is control dependent as shown in state table 4. The reference frequencies are selected by the frequency control pins/bits FS2 and FS1 as shown in Table 1.

2.2 Holdover Mode

Holdover Mode is typically used when network synchronization is temporarily disrupted.

In Holdover Mode, the MT90401 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal

When in Normal Mode, and locked to the input reference signal, a numerical value corresponding to the MT90401 output reference frequency is stored alternately in two memory locations every 30 ms. When the device is switched into Holdover Mode, the value in memory from between 30 ms and 60 ms is used to set the output frequency of the device.

The frequency accuracy of Holdover Mode is $\pm$0.02 ppm, which translates to a worst case 14 frame (125 us) slips in 24 hours. This is better than the Telcordia GR-1244-CORE Stratum 3 requirement of $\pm$0.37 ppm (255 frame slips per 24 hours).

Two factors affect the accuracy of Holdover Mode. One is drift on the Master Clock and the other is jitter on the reference signal. The drift on the Master Clock oscillator propagates unattenuated and causes the same drift on the output clocks. This drift can only be reduced by selecting more stable Master Clock oscillator. For example, a $\pm$4.6 ppm temperature compensated clock oscillator may have a temperature coefficient of 0.03 ppm per degree C. The 10 degC change while in Holdover Mode, will result in an additional offset in frequency accuracy equal to 0.3ppm which is much greater than the internal holdover accuracy of the MT90401 (0.02 ppm).

The other factor affecting accuracy is large jitter on the reference input prior (30 ms to 60 ms) to the mode switch. For instance, jitter of 7.5 UI at 700 Hz may reduce the Holdover Mode accuracy from 0.02 ppm to 0.10 ppm.

2.3 Freerun Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved. In Freerun Mode, the MT90401 provides timing and synchronization signals which are based on the master clock frequency (C20i) only, and are not synchronized to the reference signals (PRI and SEC).

The accuracy of the output clock is equal to the accuracy of the master clock (C20i). So if a $\pm$20 ppm output clock is required, the master clock must also be $\pm$20 ppm. See Applications - Master Clock section.

2.4 Fast Lock Mode

Fast Lock Mode is a submode of Normal Mode, it is used to allow the MT90401 to lock to a reference eight times more quickly than normal. Fast Lock Mode necessarily compromises the wander generation characteristics of the MT90401. When the MT90401 is in Fast Lock Mode and SONET Mode at the same time, the PLL frequency slope is limited to less than 1.9 ppm per second.

2.5 Transitions from Freerun Mode or Holdover Mode to Normal Mode

Telcordia GR-253-CORE requires SONET Internal Clocks to settle within 100 s after transitioning from Freerun Mode or Holdover Mode to Normal Mode. During such a transition, the wander filtering requirements for a SONET Internal Clock are relaxed to make a 100 s settling time possible.

To meet the GR-253-CORE 100 s settling time requirement at power-up and during a transition from Freerun Mode to Normal Mode the MT90401 should be placed in its SDH Mode until lock is achieved. When the PLL indicates lock the MT90401 should be placed in SONET Mode.

During a transition from Holdover Mode to Normal Mode, GR-253-CORE requires a SONET Internal Clock to limit the frequency slope to less than 2.9 ppm per second. To meet the 100 s settling time during such a transition it is necessary to keep the MT90401 in SONET Mode and Fast Lock Mode until lock is achieved. When the PLL indicates lock the MT90401 can be taken out of its Fast Lock Mode.

A transition from Holdover Mode to Normal Mode can result in a large initial frequency offset, for example 4.6 ppm, between the clock's reference and its output. The 2.9 ppm per second frequency slope limit required by GR-253-CORE places a lower limit on the time it takes for a SONET Internal Clock to acquire a new frequency. While the clock is acquiring the new frequency a phase error will accumulate which could cause the clock's settling time to be longer than 100 s. GR-1244-CORE and GR-253-CORE allow a clock to ignore some of the phase error accumulated during the transition from Holdover Mode to Normal Mode.

During a transition from Holdover Mode to Normal Mode, if the MT90401 has not achieved lock within 16 seconds, it is recommended that the PLL be put briefly into its Holdover Mode and then returned to Normal Mode by toggling the MS1 pin or the MS1 control bit. Toggling the PLL into and out of Holdover will clear any accumulated phase error and reduce the settling time.

3.0 MT90401 Measures of Performance

The following are some synchronizer performance indicators and their corresponding definitions.

3.1 Jitter Generation

Jitter generation is the amount of jitter produced by a PLL and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Jitter generation may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Jitter generation is usually measured with various band-limiting filters depending on the applicable standards.

3.2 Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards (see Figures 7, 8 and 9).

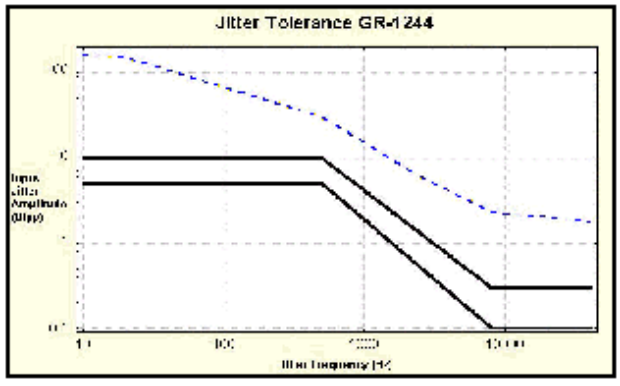

Figure 7 - Jitter Tolerance GR-1244 1.544 MHz Reference

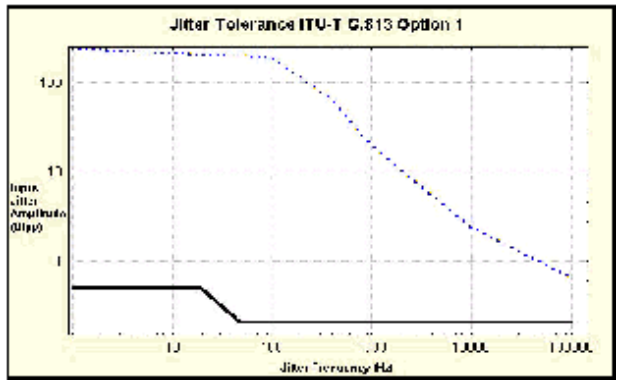

Figure 8 - Jitter Tolerance ITU-T G.813 Option 1

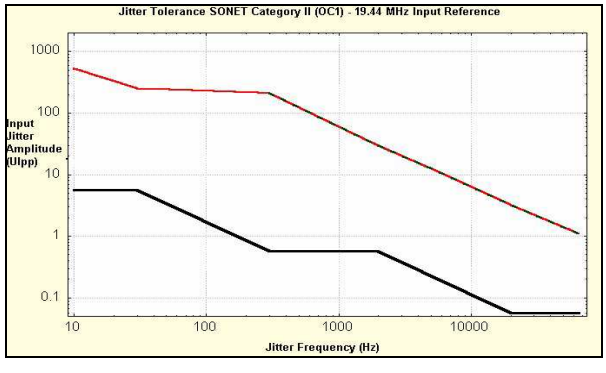

Figure 9 - Jitter Tolerance SONET Category II (OC1) 19.44 MHz Input Reference

3.3 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the MT90401, two internal elements determine the jitter attenuation. This includes the low pass loop filter and the phase slope limiter. Both of these parameters have different settings depending on whether the device is in

SONET or SDH mode. For SONET mode the loop filter has a corner frequency of 70 millihertz and the output phase slope is limited to 885 ns per second. For SDH mode the loop filter has a corner frequency of 1.1 Hertz and a maximum phase slope of 53 ns per 1.326 milliseconds. If the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited.

The MT90401 has ten outputs that can be locked to four possible input frequencies for a total of 40 possible jitter transfer functions. Since all outputs are derived from the same internal signal, the jitter transfer values for the four cases, 8 kHz to 8 kHz, 1.544 MHz to 1.544 MHz, 2.048 MHz to 2.048 MHz 19.44 MHz to 19.44 MHz can be applied to all outputs.

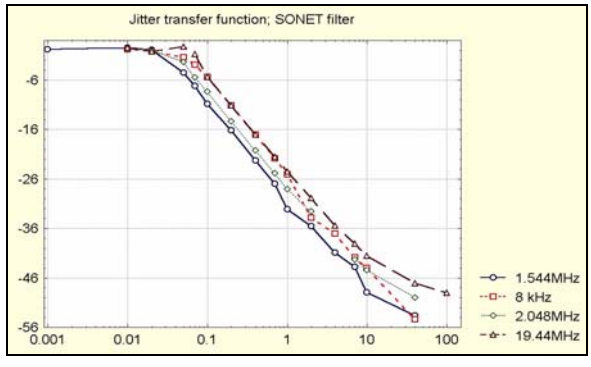

Figure 10 - Jitter and Wander Transfer with SONET filter

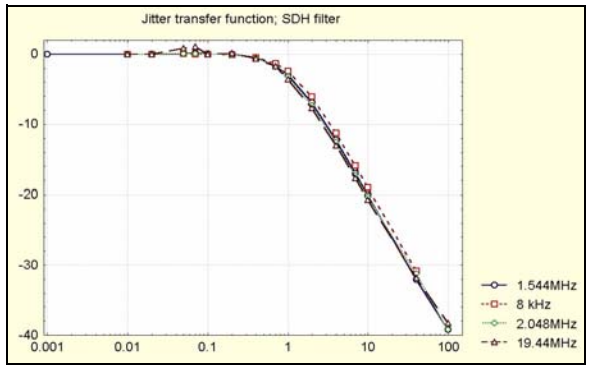

Figure 11 - Jitter and Wander Transfer with SDH Filter

It should be noted that 1 UI at 1.544 MHz is 648 ns, which is not equal to 1 UI at 2.048 MHz, which is 488 ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

Example: *What is the T1 and E1 output jitter when the T1 input jitter is 20UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18 dB?*

$$OutputT1 = InputT1 \times 10^{\left(\frac{-A}{20}\right)}$$

$$OutputT1 = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5UI(T1)$$

$$OutputE1 = OutputT1 \times \frac{(1UIT1)}{(1UIE1)}$$

$$OutputE1 = OutputT1 \times \frac{(644ns)}{(488ns)} = 3.3UI(T1)$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the four jitter transfer functions provided.

Since intrinsic jitter generation is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

Description				**State**				
Input Controls				**Freerun**	**Normal (PRI)**	**Normal (SEC)**	**Holdover (PRI)**	**Holdover (SEC)**
MS2	**MS1**	**RSEL**	**PCCi**	**S0**	**S1**	**S2**	**S1H**	**S2H**
0	0	0	0	S1	-	S1 MTIE	S1	S1 MTIE
0	0	0	1	S1	-	S1 MTIE	S1 MTIE	S1 MTIE
0	0	1	X	S2	S2 MTIE	-	S2 MTIE	S2 MTIE
0	1	0	X	/	S1H	/		/
0	1	1	X	/	S2H	S2H	/	-
1	0	X	X	-	S0	S0	S0	S0

Legend:
- No Change
/ Not Valid
MTIE State change occurs with TIE Corrector Circuit
Refer to Control State Diagram for state changes to and from Auto-Holdover State

Table 4 - Control State Table

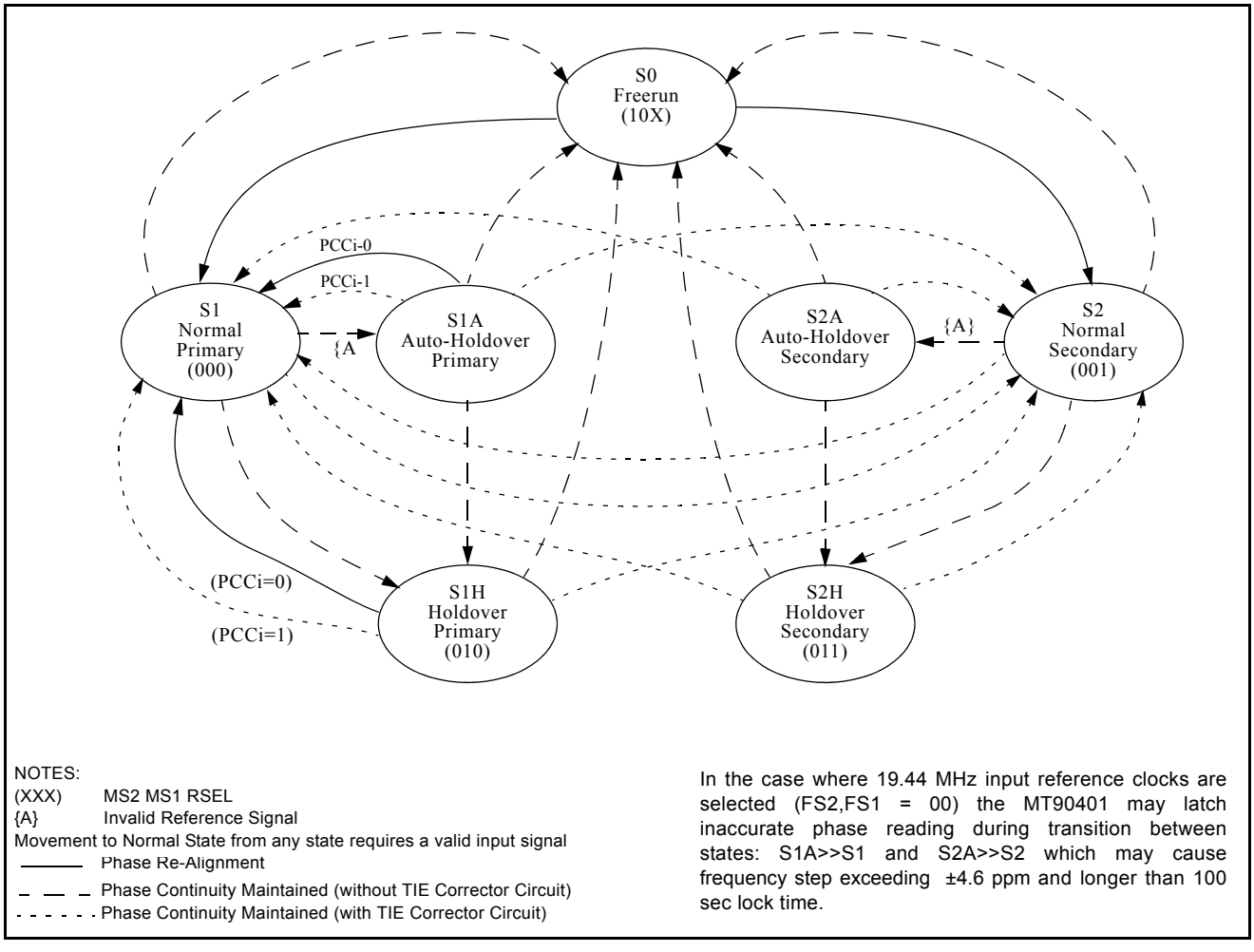

Figure 12 - Control State Diagram

3.4 Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the MT90401, the Freerun accuracy is equal to the Master Clock (C20i) accuracy.

3.5 Holdover Accuracy

Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the MT90401, the storage value is determined while the device is in Normal Mode and locked to an external reference signal. The initial frequency offset of the MT90401 in Holdover Mode is $\pm 20 \times 10^{-9}$. This is more accurate than Telcordia's GR-1244-CORE stratum 3 requirements of $\pm 50 \times 10^{-9}$. Once the MT90401 has transitioned into Holdover Mode, holdover stability is determined by the stability of the 20 MHz Master Clock Oscillator.

The absolute Master Clock (C20i) accuracy of the MT90401 does not affect Holdover accuracy, but the change in C20i accuracy while in Holdover Mode does.

3.6 Capture Range

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The MT90401 capture range is equal to ±52 ppm minus the accuracy of the master clock (C20i). For example, a ±32 ppm master clock results in a capture range of ±20 ppm.

MT90401 provides two pins and two bits, PRIOOR and SECOOR, to indicate whether the primary and secondary reference are within the 12 ppm of the nominal frequency. When the accuracy of the 20 MHz oscillator is 4.6 ppm the effective out of range limits of the PRIOOR and SECOOR pins will be +16.6 ppm to -7.4 ppm or +7.4 ppm to -16.6 ppm. Both references are monitored at the same time. PRIOOR and SECOOR are updated every 1.0 to 1.5 seconds.

3.7 Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the MT90401.

3.8 Phase Slope

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. An ideal signal is one that is at exactly the nominal frequency and is completely free of jitter and wander.

3.9 Frequency Slope

Frequency slope is measured in ppm per second and is the rate at which the fractional frequency offset of a given signal changes. The fractional frequency offset is calculated with respect to an ideal signal. The given signal is typically the output signal. An ideal signal is one that is at exactly the nominal frequency and is completely free of jitter and wander.

3.10 Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

3.11 Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

$$MTIE(S) = TIEmax(t) - TIEmin(t)$$

3.12 Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a reference switch or a mode change.

3.13 Phase Lock Time

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

1. initial input to output phase difference
2. initial input to output frequency difference
3. synchronizer loop filter
4. synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The MT90401 loop filter and limiter were optimized to meet the GR-253-CORE, GR-1244-CORE, and G-813 jitter transfer and phase slope requirements.

4.0 MT90401 and Network Specifications

The MT90401 meets all applicable PLL requirements for the following specifications.

1. Telcordia GR-1244-CORE December 2000 for Stratum 3, SONET Minimum Clock (SMC), Stratum 4 Enhanced and Stratum 4
2. Telcordia GR-253-CORE September 2000 for SONET Internal Clocks
3. ANSI T1.101 (DS1) February 1994 for Stratum 3, Stratum 4 Enhanced and Stratum 4
4. ANSI T1.105.09-1996 for SONET Minimum Clocks (SMCs)
5. ITU-T G.813 August 1996 for Option1 and Option 2 clocks (with external jitter attenuator)

5.0 Applications

This section contains MT90401 application specific details for Master clock operation, LVDS output drivers setup, microport functionality and output clock phase adjustment.

5.1 Master Clock

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the C20i input pin.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the MT90401 will always equal 52 ppm. For example, if the master timing source is $\pm$20 ppm, then the capture range will be $\pm$32 ppm.

5.2 TIE Correction (using PCCi)

When Primary Holdover Mode is entered for short time periods, TIE correction should not be enabled. This will prevent unwanted accumulated phase change between the input and output.

For example, we can estimate phase accumulation for a case when ten Normal to Holdover to Normal sequential mode changes occur, with each Holdover entered for 2 s with TIE enabled. Each mode change could account for a phase shift as large as 250 ns. Thus, the accumulated phase could be as large as 2.9 us, and, the overall MTIE could be as large as 2.9 us.

$$Phase_{hold} = 0.02ppm \times 2s = 40ns$$
$$Phase_{state} = 50ns + 200ns = 250ns$$
$$Phase_{10} = 10 \times (250ns + 40ns) = 2.9us$$

- 0.02 ppm is the accuracy of Holdover Mode
- 50 ns is the maximum phase continuity of the MT90401 from Normal Mode to Holdover Mode
- 200 ns is the maximum phase continuity of the MT90401 from Holdover Mode to Normal Mode (with or without TIE Corrector Circuit)

When the same ten Normal to Holdover to Normal mode changes occur with TIE disabled, the overall MTIE will only be 250 ns. There would be no accumulated phase change, since the input to output phase is re-aligned after every Holdover to Normal state change.

5.3 C155 clock generation and LVDS output drivers

The MT90401 provides a 155.52 MHz clock that is frequency locked to the internally generated 19.44 MHz clock. The locking of both clocks is achieved by the internal analog PLL that multiplies the 19.44 MHz clock eight times. This C155 clock is output on pins C155P and C155N in LVDS format. The LVDS offset voltage Vos is set by applying an external 1.25 V reference voltage to the Vref input (pin 33). This pin can be connected to a common 1.25 V voltage reference that may exist on the customer board or alternatively can be generated by a simple voltage divider as it is shown in Figure 13 - LVDS Voltage Offset Vos Generation Circuit. To ensure proper operation of LVDS drivers, the decoupling capacitor must be placed very close to the MT90401 package.

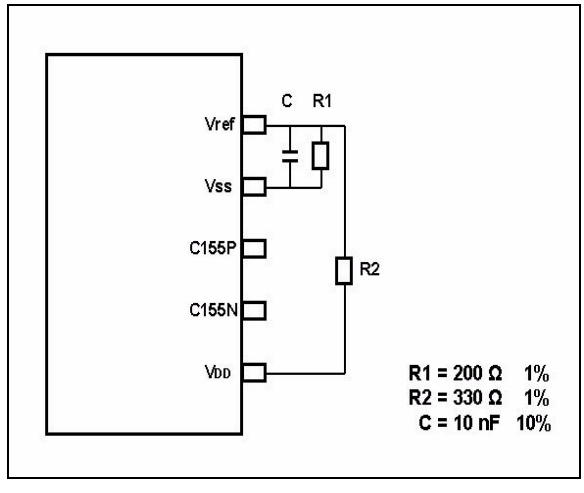

Figure 13 - LVDS Voltage Offset Vos Generation Circuit

5.4 Microport

If the HW pin is tied low, an 8 bit Motorola microprocessor may be used to control the PLL and report on the device status. In this case the control pins SONET/$\overline{\text{SDH}}$, RSEL, MS1, MS2, FS1, FS2, and FLOCK are unused and they are replaced by the control bits SONET/$\overline{\text{SDH}}$, RSEL, MS1, MS2, FS1, FS2, FLOCK. The input pin PCCi remains in use. The output pins LOCK, HOLDOVER, SECOOR, PRIOOR function whether the device is in microprocessor mode or hardware mode, but these signals are also available in Status Register 1. The microport provides additional functionality not available in hardware.

5.5 Output Phase Adjustment

Two control registers are available to program the output phase offset of the generated clocks. All 16.384 MHz derived outputs clocks, F16o, F80, F0o, C16o, C8o, C4o and C2o can be collectively shifted up to 125 microseconds with a step size of 60 nS with respect to the input reference by programming the Set Delay Word 1 and Set Delay Word 2 registers.

Control and Status Registers			
Address ($A_6A_5A_4A_3A_2A_1A_0$)	**Register**	**Read/ Write**	**Function**
00H (Table 6)	Control Register 1	Read/ Write	RSEL, FS2, FS1, MS2, MS1, SONET/$\overline{SDH}$ FLOCK, TCLR
01H (Table 7)	Status Register 1	Read Only	PRIOOR, SECOOR, LOCK, HOLDOVER, RSV, FLim, RSV, RSV
02H	Reserved	Read Only	
03H	Reserved	Read Only	
04H (Table 8)	Control Register 2	Read/ Write	E3/DS3/$\overline{OC3}$, E3/$\overline{DS3}$, RSV=0, RSV=0, RSV=0, RSV=0, RSV=0, RSV=0.
05H	Reserved	Read /Write	Set all bits to zero.
06H (Table 9)	Set Delay Word 2	Read/ Write	RSV=0, RSV=0, RSV=0, RSV=0, OffEn, C16OCNT10,C16OCNT9, C16OCNT8
07H (Table 10)	Set Delay Word 1	Read/ Write	C16OCNT7-0
08H	Reserved	Read/ Write	Set all bits to zero.
09H	Reserved	Read Only	
0AH	Reserved	Read Only	
0BH	Reserved	Read Only	
0CH	Reserved	Read Only	
0DH	Reserved	Read Only	

Table 5 - Register Map