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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Features

- Supports AT&T TR62411 and Bellcore GR-1244-CORE Stratum 3, Stratum 4 Enhanced and Stratum 4 timing for DS1 interfaces
- Supports ITU-T G.813 Option 1 clocks for 2048 kbit/s interfaces
- Supports ITU-T G.812 Type IV clocks for 1,544 kbit/s interfaces and 2,048 kbit/s interfaces
- Supports ETSI ETS 300 011, TBR 4, TBR 12 and TBR 13 timing for E1 interfaces
- Selectable 1.544 MHz, 2.048 MHz or 8 kHz input reference signals
- Provides C1.5, C2, C3, C4, C6, C8, C16, and C19 (STS-3/OC3 clock divided by 8) output clock signals
- Provides 5 different 8 KHz framing pulses
- Holdover frequency accuracy of 0.05 PPM
- Holdover indication
- Attenuates wander from 1.9 Hz
- Provides Time Interval Error (TIE) correction

Ordering Information

MT9044AP	44 Pin PLCC	Tubes
MT9044AL	44 Pin MQFP	Trays
MT9044APR	44 Pin PLCC	Tape & Reel
MT9044APR1	44 Pin PLCC*	Tape & Reel
MT9044AP1	44 Pin PLCC*	Tubes
MT9044AL1	44 Pin MQFP*	Trays

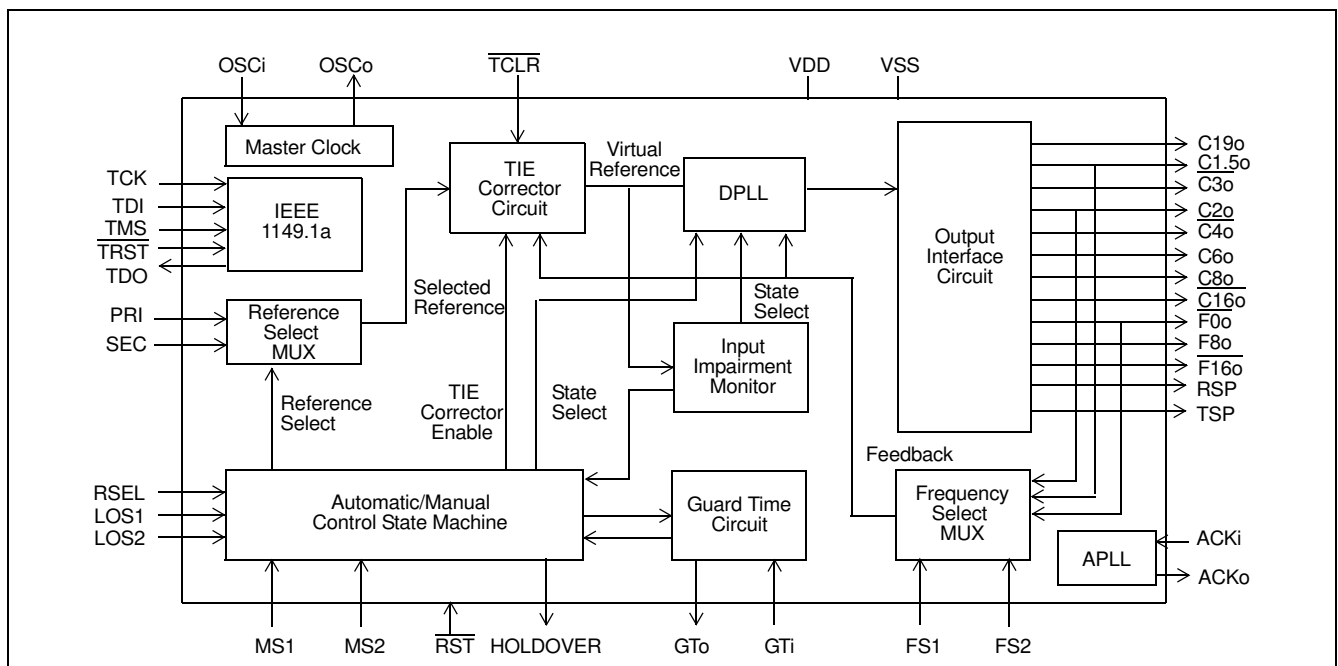
* Pb Free Matte Tin

-40°C to +85°C

- Accepts reference inputs from two independent sources
- JTAG Boundary Scan

Applications

- Synchronization and timing control for multitrunk T1,E1 and STS-3/OC3 systems
- ST-BUS clock and frame pulse sources


Figure 1 - Functional Block Diagram

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912,
 France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

Change Summary

Changes from November 2004 Issue to November 2005 Issue. Page, section, figure and table numbers refer to this issue.

Page	Item	Change
6	Pin Description - Pin 28 $\overline{\text{RST}}$	The sentence "While the $\overline{\text{RST}}$ pin is low, all frame and clock outputs are at logic high." is changed to "While the $\overline{\text{RST}}$ pin is low, all frame outputs except RSP and TSP and all clock outputs except C6o, C16o and C19o are at logic high. The RSP, TSP, C6o and C16o are at logic low during reset. The C19o is free-running during reset."

Changes from November 2003 Issue to November 2004 Issue. Page, section, figure and table numbers refer to this issue.

Page	Item	Change
21	Guard Time Calculation	Example time increases from to 0.9 to 1.45 seconds
27	Table "DC Electrical Characteristics" line item 7	Changed Minimum Schmitt high level input voltage V_{SIH} from 2.3 volts to 3.4 volts

Description

The MT9044 T1/E1/OC3 System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization signals for multitrunk T1 and E1 primary rate transmission links and STS-3/OC3 links.

The MT9044 generates ST-BUS clock and framing signals that are phase locked to either a 2.048 MHz, 1.544 MHz, or 8 kHz input reference.

The MT9044 is compliant with AT&T TR62411 and Bellcore GR-1244-CORE Stratum 3, Stratum 4 Enhanced, and Stratum 4; and ETSI ETS 300 011; and ITU-T G.813 Option 1 for 2048 kbit/s interfaces. It will meet the jitter/wander tolerance, jitter/wander transfer, intrinsic jitter/wander, frequency accuracy, capture range, phase change slope, holdover frequency and MTIE requirements for these specifications.

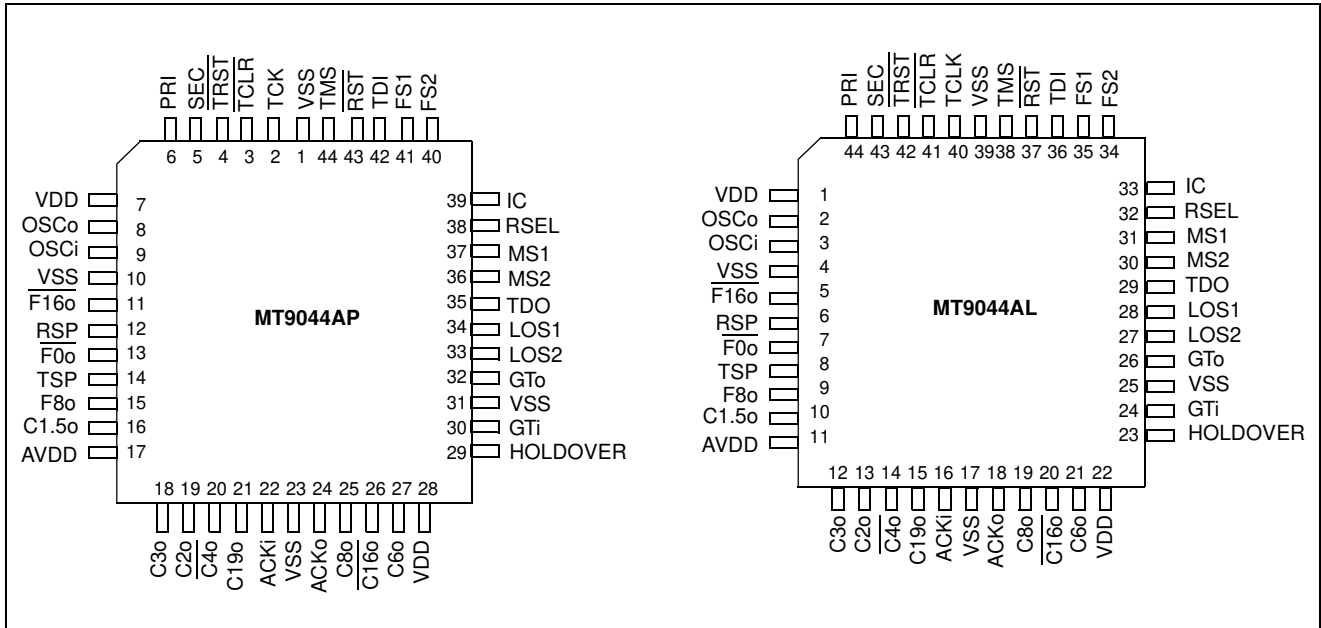


Figure 2 - Pin Connections

Pin Description

Pin # PLCC	Pin # MQFP	Name	Description
1,10, 23,31	39,4,17 ,25	V _{SS}	Ground. 0 Volts.
2	40	TCK	Test Clock (TTL Input): Provides the clock to the JTAG test logic. This pin is internally pulled up to V _{DD} .
3	41	$\overline{\text{TCLR}}$	TIE Circuit Reset (TTL Input): A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a re-alignment of input phase with output phase as shown in Figure 19. The $\overline{\text{TCLR}}$ pin should be held low for a minimum of 300 ns. This pin is internally pulled down to VSS.
4	42	$\overline{\text{TRST}}$	Test Reset (TTL Input): Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin is internally pulled down to VSS.
5	43	SEC	Secondary Reference (TTL Input). This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of three possible frequencies (8 kHz, 1.544 MHz, or 2.048 MHz) may be used. The selection of the input reference is based upon the MS1, MS2, LOS1, LOS2, RSEL, and GTi control inputs (Automatic or Manual). This pin is internally pulled up to V _{DD} .
6	44	PRI	Primary Reference (TTL Input). See pin description for SEC. This pin is internally pulled up to V _{DD} .
7,28	1,22	V _{DD}	Positive Supply Voltage. +5V _{DC} nominal.
8	2	OSCo	Oscillator Master Clock (CMOS Output). For crystal operation, a 20 MHz crystal is connected from this pin to OSCi, see Figure 10. For clock oscillator operation, this pin is left unconnected, see Figure 9.
9	3	OSCi	Oscillator Master Clock (CMOS Input). For crystal operation, a 20 MHz crystal is connected from this pin to OSCo, see Figure 10. For clock oscillator operation, this pin is connected to a clock source, see Figure 9.
11	5	$\overline{\text{F16o}}$	Frame Pulse ST-BUS 8.192 Mb/s (CMOS Output). This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s. See Figure 20.
12	6	RSP	Receive Sync Pulse (CMOS Output). This is an 8 kHz 488 ns active high framing pulse, which marks the end of an ST-BUS frame. This is typically used for connection to the Siemens MUNICH-32 device. See Figure 21.
13	7	$\overline{\text{F0o}}$	Frame Pulse ST-BUS 2.048 Mb/s (CMOS Output). This is an 8 kHz 244 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s. See Figure 20.
14	8	TSP	Transmit Sync Pulse (CMOS Output). This is an 8 kHz 488 ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for connection to the Siemens MUNICH-32 device. See Figure 21.
15	9	F8o	Frame Pulse (CMOS Output). This is an 8 kHz 122 ns active high framing pulse, which marks the beginning of a frame. See Figure 20.
16	10	C1.5o	Clock 1.544 MHz (CMOS Output). This output is used in T1 applications.
17	11	AVDD	Analog Vdd. +5V _{DC} nominal.
18	12	C3o	Clock 3.088 MHz (CMOS Output). This output is used in T1 applications.

Pin Description (continued)

Pin # PLCC	Pin # MQFP	Name	Description
19	13	C2o	Clock 2.048 MHz (CMOS Output). This output is used for ST-BUS operation at 2.048 Mb/s.
20	14	$\overline{C4o}$	Clock 4.096 MHz (CMOS Output). This output is used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s.
21	15	C19o	Clock 19.44 MHz (CMOS Output). This output is used in OC3/STS3 applications.
22	16	ACKi	Analog PLL Clock Input (CMOS Input). This input clock is a reference for an internal analog PLL. This pin is internally pulled down to VSS.
24	18	ACKo	Analog PLL Clock Output (CMOS Output). This output clock is generated by the internal analog PLL.
25	19	C8o	Clock 8.192 MHz (CMOS Output). This output is used for ST-BUS operation at 8.192 Mb/s.
26	20	$\overline{C16o}$	Clock 16.384 MHz (CMOS Output). This output is used for ST-BUS operation with a 16.384 MHz clock.
27	21	C6o	Clock 6.312 Mhz (CMOS Output). This output is used for DS2 applications.
29	23	HOLDOVER	Holdover (CMOS Output). This output goes to a logic high whenever the digital PLL goes into holdover mode.
30	24	GTi	Guard Time (Schmitt Input). This input is used by the MT9044 state machine in both Manual and Automatic modes. The signal at this pin affects the state changes between Primary Holdover Mode and Primary Normal Mode, and Primary Holdover Mode and Secondary Normal Mode. The logic level at this input is gated in by the rising edge of F8o. See Tables 4 and 5.
32	26	GTo	Guard Time (CMOS Output). The LOS1 input is gated by the rising edge of F8o, buffered and output on GTo. This pin is typically used to drive the GTi input through an RC circuit.
33	27	LOS2	Secondary Reference Loss (TTL Input). This input is normally connected to the loss of signal (LOS) output signal of a Line Interface Unit (LIU). When high, the SEC reference signal is lost or invalid. LOS2, along with the LOS1 and GTi inputs control the MT9044 state machine when operating in Automatic Control. The logic level at this input is gated in by the rising edge of F8o. This pin is internally pulled down to VSS.
34	28	LOS1	Primary Reference Loss (TTL Input). Typically, external equipment applies a logic high to this input when the PRI reference signal is lost or invalid. The logic level at this input is gated in by the rising edge of F8o. See LOS2 description. This pin is internally pulled down to VSS.
35	29	TDO	Test Serial Data Out (TTL Output). JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
36	30	MS2	Mode/Control Select 2 (TTL Input). This input, in conjunction with MS1, determines the device's mode (Automatic or Manual) and state (Normal, Holdover or Freerun) of operation. The logic level at this input is gated in by the rising edge of F8o. See Table 3.

Pin Description (continued)

Pin # PLCC	Pin # MQFP	Name	Description
37	31	MS1	Mode/Control Select 1 (TTL Input). The logic level at this input is gated in by the rising edge of F8o. See pin description for MS2. This pin is internally pulled down to VSS.
38	32	RSEL	Reference Source Select (TTL Input). In Manual Control, a logic low selects the PRI (primary) reference source as the input reference signal and a logic high selects the SEC (secondary) input. In Automatic Control, this pin must be at logic low. The logic level at this input is gated in by the rising edge of F8o. See Table 2. This pin is internally pulled down to VSS.
39	33	IC	Internal Connection. Tie low for normal operation.
40	34	FS2	Frequency Select 2 (TTL Input). This input, in conjunction with FS1, selects which of three possible frequencies (8 kHz, 1.544 MHz, or 2.048 MHz) may be input to the PRI and SEC inputs. See Table 1.
41	35	FS1	Frequency Select 1 (TTL Input). See pin description for FS2.
42	36	TDI	Test Serial Data In (TTL Input). JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V _{DD} .
43	37	$\overline{\text{RST}}$	Reset (Schmitt Input). A logic low at this input resets the MT9044. To ensure proper operation, the device must be reset after changes to the method of control, reference signal frequency changes and power-up. The $\overline{\text{RST}}$ pin should be held low for a minimum of 300 ns. While the $\overline{\text{RST}}$ pin is low, all frame outputs except RSP and TSP and all clock outputs except C6o, $\overline{\text{C16o}}$ and C19o are at logic high. The RSP, TSP, C6o and $\overline{\text{C16o}}$ are at logic low during reset. The C19o is free-running during reset. Following a reset, the input reference source and output clocks and frame pulses are phase aligned as shown in Figure 19.
44	38	TMS	Test Mode Select (TTL Input). JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V _{DD} .

Functional Description

The MT9044 is a Multitrunk System Synchronizer, providing timing (clock) and synchronization (frame) signals to interface circuits for T1 and E1 Primary Rate Digital Transmission links.

Figure 1 shows the functional block diagram which is described in the following sections.

Reference Select MUX Circuit

The MT9044 accepts two simultaneous reference input signals and operates on their falling edges. Either the primary reference (PRI) signal or the secondary reference (SEC) signal can be selected as input to the TIE Corrector Circuit. The selection is based on the Control, Mode and Reference Selection of the device. See Tables 1, 4 and 5.

Frequency Select MUX Circuit

The MT9044 operates with one of three possible input reference frequencies (8 kHz, 1.544 MHz or 2.048 MHz). The frequency select inputs (FS1 and FS2) determine which of the three frequencies may be used at the reference inputs (PRI and SEC). Both inputs must have the same frequency applied to them. A reset (RST) must be performed after every frequency select input change. Operation with FS1 and FS2 both at logic low is reserved and must not be used. See Table 1.

FS2	FS1	Input Frequency
0	0	Reserved
0	1	8 kHz
1	0	1.544 MHz
1	1	2.048 MHz

Table 1 - Input Frequency Selection

Time Interval Error (TIE) Corrector Circuit

The TIE corrector circuit, when enabled, prevents a step change in phase on the input reference signals (PRI or SEC) from causing a step change in phase at the input of the DPLL block of Figure 1.

During reference input rearrangement, such as during a switch from the primary reference (PRI) to the secondary reference (SEC), a step change in phase on the input signals will occur. A phase step at the input of the DPLL will lead to unacceptable phase changes in the output signal.

As shown in Figure 3, the TIE Corrector Circuit receives one of the two reference (PRI or SEC) signals, passes the signal through a programmable delay line, and uses this delayed signal as an internal virtual reference, which is input to the DPLL. Therefore, the virtual reference is a delayed version of the selected reference.

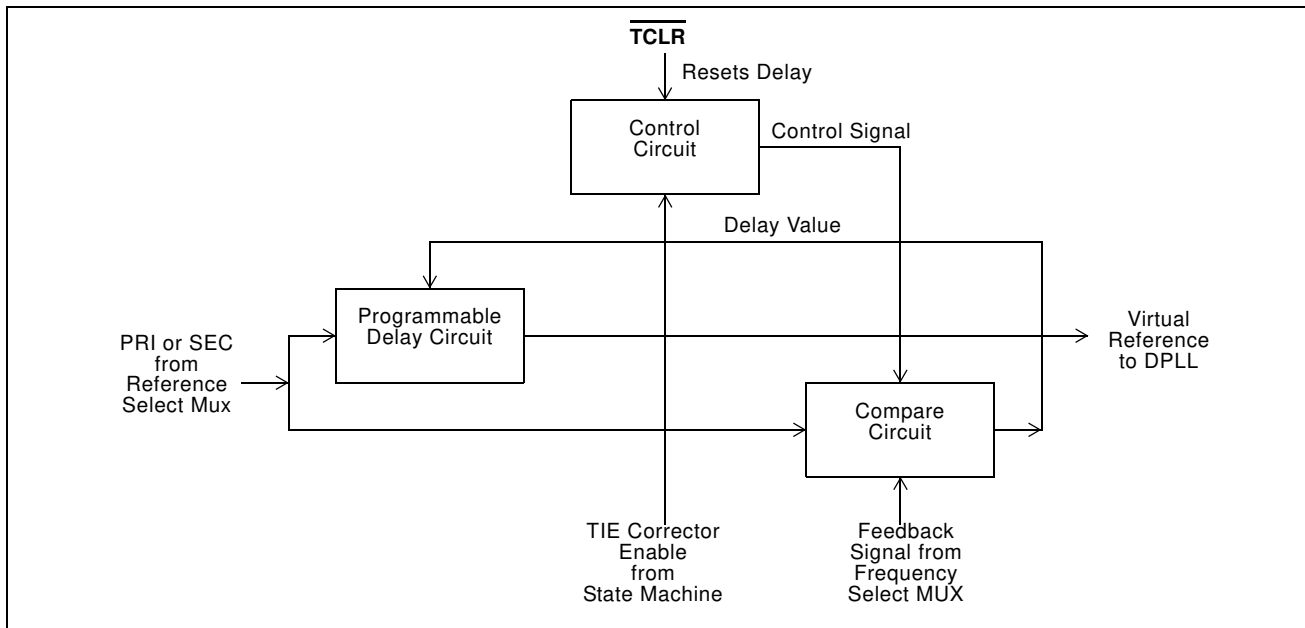


Figure 3 - TIE Corrector Circuit

During a switch, from one reference to the other, the State Machine first changes the mode of the device from Normal to Holdover. In Holdover Mode, the DPLL no longer uses the virtual reference signal, but generates an accurate clock signal using storage techniques. The Compare Circuit then measures the phase delay between the current phase (feedback signal) and the phase of the new reference signal. This delay value is passed to the Programmable Delay Circuit (See Figure 3). The new virtual reference signal is now at the same phase position as the previous reference signal would have been if the reference switch had not taken place. The State Machine then returns the device to Normal Mode.

The DPLL now uses the new virtual reference signal, and since no phase step took place at the input of the DPLL, no phase step occurs at the output of the DPLL. In other words, reference switching will not create a phase change at the input of the DPLL, or at the output of the DPLL.

Since internal delay circuitry maintains the alignment between the old virtual reference and the new virtual reference, a phase error may exist between the selected input reference signal and the output signal of the DPLL. This phase error is a function of the difference in phase between the two input reference signals during reference rearrangements. Each time a reference switch is made, the delay between input signal and output signal will change. The value of this delay is the accumulation of the error measured during each reference switch.

The programmable delay circuit can be zeroed by applying a logic low pulse to the TIE Circuit Reset ($\overline{\text{TCLR}}$) pin. A minimum reset pulse width is 300 ns. This results in a phase alignment between the input reference signal and the output signal as shown in Figure 20. The speed of the phase alignment correction is limited to 5 ns per 125 us, and convergence is in the direction of least phase travel.

The state diagrams of Figure 7 and 8 indicate the state changes that activate the TIE Corrector Circuit.

Digital Phase Lock Loop (DPLL)

As shown in Figure 4, the DPLL of the MT9044 consists of a Phase Detector, Limiter, Loop Filter, Digitally Controlled Oscillator, and a Control Circuit.

Phase Detector - the Phase Detector compares the virtual reference signal from the TIE Corrector circuit with the feedback signal from the Frequency Select MUX circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Limiter circuit. The Frequency Select MUX allows the proper feedback signal to be externally selected (e.g., 8 kHz, 1.544 MHz or 2.048 MHz).

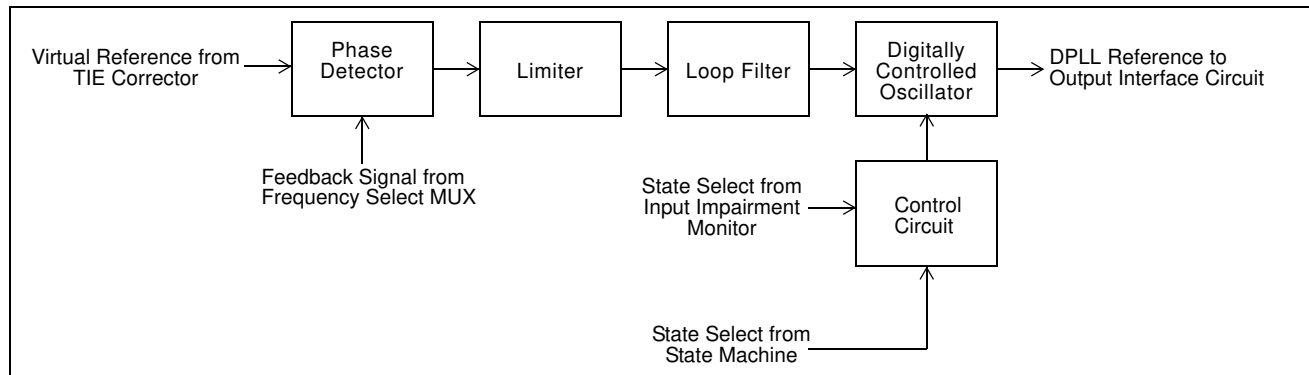


Figure 4 - DPLL Block Diagram

Limiter - the Limiter receives the error signal from the Phase Detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 5 ns per 125 us. This is well within the maximum phase slope of 7.6 ns per 125 us or 81 ns per 1.326 ms specified by AT&T TR62411, and Bellcore GR-1244-CORE.

Loop Filter - the Loop Filter is similar to a first order low pass filter with a 1.9 Hz cutoff frequency for all three reference frequency selections (8 kHz, 1.544 MHz or 2.048 MHz). This filter ensures that the jitter transfer requirements in ETS 300 011 and AT&T TR62411 are met.

Control Circuit - the Control Circuit uses status and control information from the State Machine and the Input Impairment Circuit to set the mode of the DPLL. The three possible modes are Normal, Holdover and Freerun.

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the MT9044.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover Mode, the DCO is free running at a frequency equal to the last (less 30 ms to 60 ms) frequency the DCO was generating while in Normal Mode.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20 MHz source.

Output Interface Circuit

The output of the DCO (DPLL) is used by the Output Interface Circuit to provide the output signals shown in Figure 5. The Output Interface Circuit uses four Tapped Delay Lines followed by a T1 Divider Circuit, an E1 Divider Circuit, a DS2 Divider Circuit and an analog PLL to generate the required output signals.

Four tapped delay lines are used to generate a 16.384 MHz, 12.352 MHz, 12.624 MHz and 19.44 MHz signals.

The E1 Divider Circuit uses the 16.384 MHz signal to generate four clock outputs and three frame pulse outputs. The C8o, C4o and C2o clocks are generated by simply dividing the C16o clock by two, four and eight respectively. These outputs have a nominal 50% duty cycle.

The T1 Divider Circuit uses the 12.384 MHz signal to generate two clock outputs. C1.5o and C3o are generated by dividing the internal C12 clock by four and eight respectively. These outputs have a nominal 50% duty cycle.

The DS2 Divider Circuit uses the 12.624 MHz signal to generate the clock output C6o. This output has a nominal 50% duty cycle.

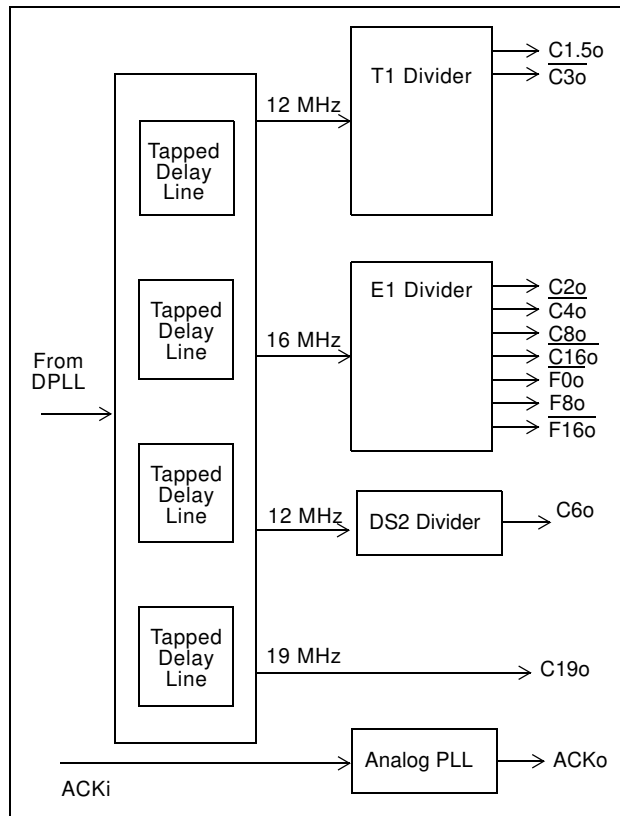


Figure 5 - Output Interface Circuit Block

The frame pulse outputs (F0o, F8o, F16o, TSP, RSP) are generated directly from the C16 clock.

The $\overline{T1}$ and $\overline{E1}$ signals are generated from a common DPLL signal. Consequently, the clock outputs $\overline{C1.5o}$, $\overline{C3o}$, $\overline{C2o}$, $\overline{C4o}$, $\overline{C8o}$, $\overline{C16o}$, $\overline{F0o}$, $\overline{F16o}$ and $\overline{C6o}$ are locked to one another for all operating states, and are also locked to the selected input reference in Normal Mode. See Figures 20 and 21.

All frame pulse and clock outputs have limited driving capability, and should be buffered when driving high capacitance (e.g. 30 pF) loads.

Analog Phase Lock Loop (APLL)

The analog PLL is intended to be used to achieve a 50% duty cycle output clock. Connecting $\overline{C19o}$ to \overline{ACKi} will generate a phase locked 19.44 MHz \overline{ACKo} output with a nominal 50% duty cycle and a maximum peak_to_peak unfiltered jitter of 0.174 U.I.. The analog PLL has an intrinsic jitter of less than 0.01 U.I. In order to achieve this low jitter level a separate pin is provided to power (\overline{AVdd}) the analog PLL.

Input Impairment Monitor

This circuit monitors the input signal to the DPLL and automatically enables the Holdover Mode (Auto-Holdover) when the frequency of the incoming signal is outside the auto-holdover capture range (See AC Electrical Characteristics - Performance). This includes a complete loss of incoming signal, or a large frequency shift in the incoming signal. When the incoming signal returns to normal, the DPLL is returned to Normal Mode with the output signal locked to the input signal. The holdover output signal is based on the incoming signal 30 ms minimum to 60 ms prior to entering the Holdover Mode. The amount of phase drift while in holdover is negligible because the Holdover Mode is very accurate (e.g., ± 0.05 ppm). The the Auto-Holdover circuit does not use TIE correction. Consequently, the phase delay between the input and output after switching back to Normal Mode is preserved (is the same as just prior to the switch to Auto-Holdover).

Automatic/Manual Control State Machine

The Automatic/Manual Control State Machine allows the MT9044 to be controlled automatically (i.e., $\overline{LOS1}$, $\overline{LOS2}$ and \overline{GTi} signals) or controlled manually (i.e., $\overline{MS1}$, $\overline{MS2}$, \overline{GTi} and \overline{RSEL} signals). With manual control a single mode of operation (i.e., Normal, Holdover and Freerun) is selected. Under automatic control the state of the $\overline{LOS1}$, $\overline{LOS2}$ and \overline{GTi} signals determines the sequence of modes that the MT9044 will follow.

As shown in Figure 1, this state machine controls the Reference Select MUX, the TIE Corrector Circuit, the DPLL and the Guard Time Circuit. Control is based on the logic levels at the control inputs $\overline{LOS1}$, $\overline{LOS2}$, \overline{RSEL} , $\overline{MS1}$, $\overline{MS2}$ and \overline{GTi} of the Guard Time Circuit (See Figure 6).

All state machine changes occur synchronously on the rising edge of $\overline{F8o}$. See the Controls and Modes of Operation section for full details on Automatic Control and Manual Control.

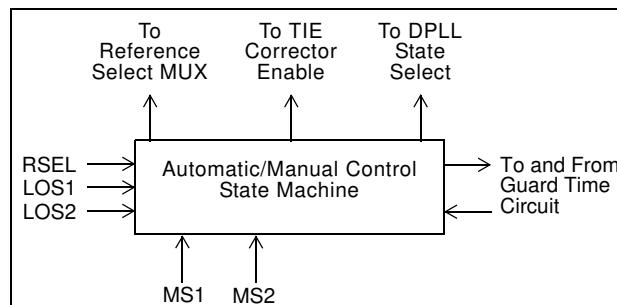


Figure 6 - Automatic/Manual Control State Machine Block Diagram

Guard Time Circuit

The GTi pin is used by the Automatic/Manual Control State Machine in the MT9044 under either Manual or Automatic control. The logic level at the GTi pin performs two functions, it enables and disables the TIE Corrector Circuit (Manual and Automatic) and it selects which mode change takes place (Automatic only). See the Applications - Guard Time section.

For both Manual and Automatic control, when switching from Primary Holdover to Primary Normal, the TIE Corrector Circuit is enabled when GTi=1, and disabled when GTi=0.

Under Automatic control and in Primary Normal Mode, two state changes are possible (not counting Auto-Holdover). These are state changes to Primary Holdover or to Secondary Normal. The logic level at the GTi pin determines which state change occurs. When GTi=0, the state change is to Primary Holdover. When GTi=1, the state change is to Secondary Normal.

Master Clock

The MT9044 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

Control and Modes of Operation

The MT9044 can operate either in Manual or Automatic Control. Each control method has three possible modes of operation, Normal, Holdover and Freerun.

As shown in Table 3, Mode/Control Select pins MS2 and MS1 select the mode and method of control.

Control	RSEL	Input Reference
MANUAL	0	PRI
	1	SEC
AUTO	0	State Machine Control
	1	Reserved

Table 2 - Input Reference Selection

MS2	MS1	Control	Mode
0	0	MANUAL	NORMAL
0	1	MANUAL	HOLDOVER
1	0	MANUAL	FREERUN
1	1	AUTO	State Machine Control

Table 3 - Operating Modes and States

Manual Control

Manual Control should be used when either very simple MT9044 control is required, or when complex control is required which is not accommodated by Automatic Control. For example, very simple control could include operation in a system which only requires Normal Mode with reference switching using only a single input stimulus (RSEL). Very simple control would require no external circuitry. Complex control could include a system which requires state changes between Normal, Holdover and Freerun Modes based on numerous input stimuli. Complex control would require external circuitry, typically a microcontroller.

Under Manual Control, one of the three modes is selected by mode/control select pins MS2 and MS1. The active reference input (PRI or SEC) is selected by the RSEL pin as shown in Table 2. Refer to Table 4 and Figure 7 for details of the state change sequences.

Automatic Control

Automatic Control should be used when simple MT9044 control is required, which is more complex than the very simple control provide by Manual Control with no external circuitry, but not as complex as Manual Control with a microcontroller. For example, simple control could include operation in a system which can be accommodated by the Automatic Control State Diagram shown in Figure 8.

Automatic Control is also selected by mode/control pins MS2 and MS1. However, the mode and active reference source is selected automatically by the internal Automatic State Machine (See Figure 6). The mode and reference changes are based on the logic levels on the LOS1, LOS2 and GTi control pins. Refer to Table 5 and Figure 8 for details of the state change sequences.

Normal Mode

Normal Mode is typically used when a slave clock source, synchronized to the network is required.

In Normal Mode, the MT9044 provides timing ($C1.5o$, $C2o$, $\overline{C3o}$, $\overline{C4o}$, $C8o$, $\overline{C16o}$, and $C19$) and frame synchronization ($\overline{F0o}$, $F8o$, $\overline{F16o}$, RSP, TSP) signals, which are synchronized to one of two reference inputs (PRI or SEC). The input reference signal may have a nominal frequency of 8 kHz, 1.544 MHz or 2.048 MHz.

From a reset condition, the MT9044 will take up to 25 seconds for the output signal to be phase locked to the selected reference.

The selection of input references is control dependent as shown in State Tables 4 and 5. The reference frequencies are selected by the frequency control pins FS2 and FS1 as shown in Table 1.

Holdover Mode

Holdover Mode is typically used for short durations (e.g., 2 seconds) while network synchronization is temporarily disrupted.

In Holdover Mode, the MT9044 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal.

When in Normal Mode, and locked to the input reference signal, a numerical value corresponding to the MT9044 output frequency is stored alternately in two memory locations every 30 ms. When the device is switched into Holdover Mode, the value in memory from between 30 ms and 60 ms is used to set the output frequency of the device.

The frequency accuracy of Holdover Mode is ± 0.05 ppm, which translates to a worst case 35 frame (125 us) slips in 24 hours. This meets the Bellcore GR-1244-CORE Stratum 3 requirement of ± 0.37 ppm (255 frame slips per 24 hours).

Two factors affect the accuracy of Holdover Mode. One is drift on the Master Clock while in Holdover Mode, drift on the Master Clock directly affects the Holdover Mode accuracy. Note that the absolute Master Clock (OSC_i) accuracy does not affect Holdover accuracy, only the change in OSC_i accuracy while in Holdover. For example, a ± 32 ppm master clock may have a temperature coefficient of ± 0.1 ppm per degree C. So a 10 degree change in temperature, while the MT9044 is in Holdover Mode may result in an additional offset (over the ± 0.05 ppm) in frequency accuracy of ± 1 ppm, which is much greater than the ± 0.05 ppm of the MT9044.

The other factor affecting accuracy is large jitter on the reference input prior (30 ms to 60 ms) to the mode switch. For instance, jitter of 7.5 UI at 700 Hz may reduce the Holdover Mode accuracy from 0.05 ppm to 0.10 ppm.

Freerun Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun Mode, the MT9044 provides timing and synchronization signals which are based on the master clock frequency (OSC_i) only, and are not synchronized to the reference signals (PRI and SEC).

The accuracy of the output clock is equal to the accuracy of the master clock (OSC_i). So if a ± 32 ppm output clock is required, the master clock must also be ± 32 ppm. See Applications - Crystal and Clock Oscillator sections.

Description				State				
Input Controls				Freerun	Normal (PRI)	Normal (SEC)	Holdover (PRI)	Holdover (SEC)
MS2	MS1	RSEL	GTi	S0	S1	S2	S1H	S2H
0	0	0	0	S1	-	S1 MTIE	S1	S1 MTIE
0	0	0	1	S1	-	S1 MTIE	S1 MTIE	S1 MTIE
0	0	1	X	S2	S2 MTIE	-	S2 MTIE	S2 MTIE
0	1	0	X	/	S1H	/	-	/
0	1	1	X	/	S2H	S2H	/	-
1	0	X	X	-	S0	S0	S0	S0

Legend:
 - No Change
 / Not Valid
 MTIE State change occurs with TIE Corrector Circuit
 Refer to Manual Control State Diagram for state changes to and from Auto-Holdover State

Table 4 - Manual Control State Table

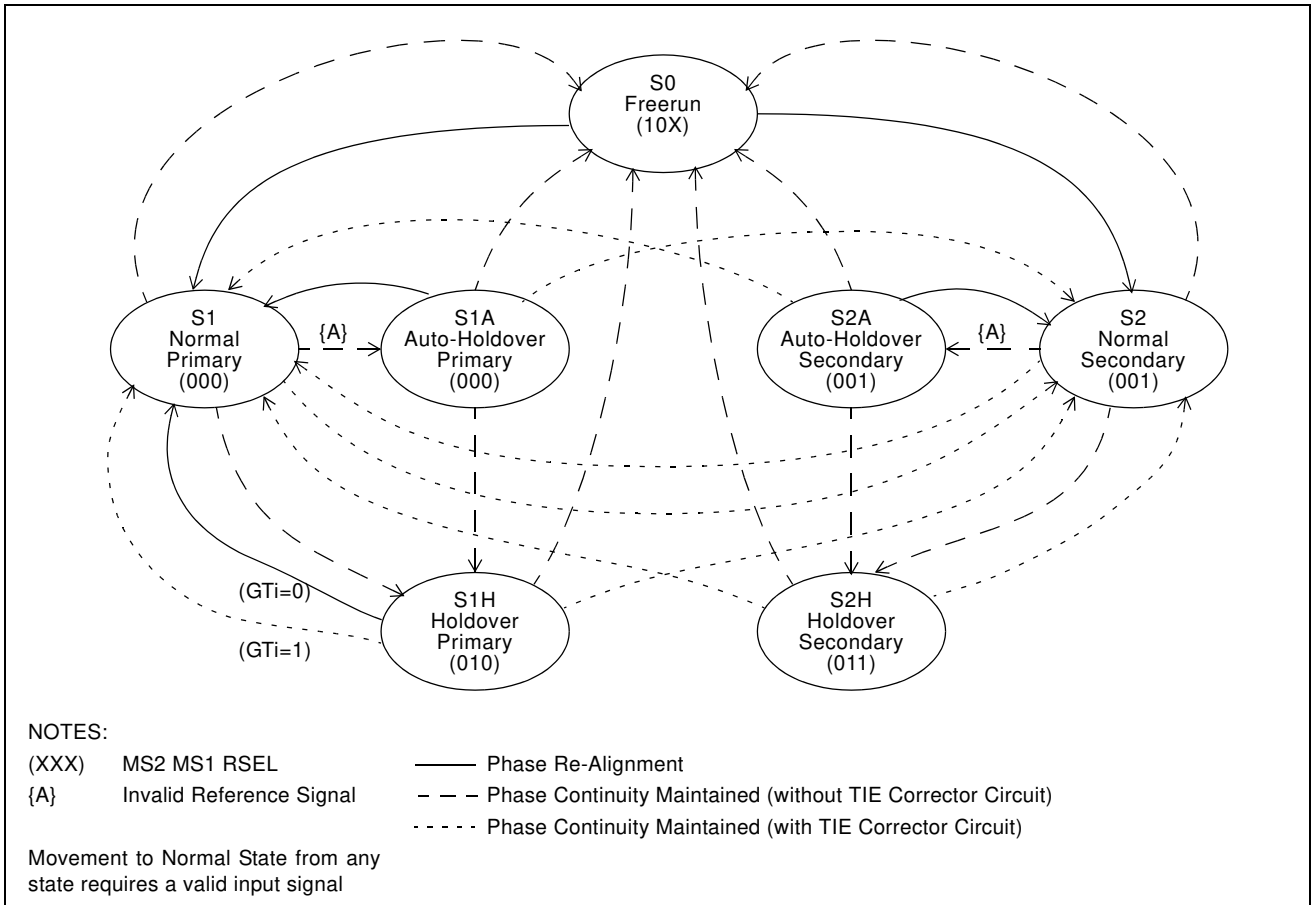


Figure 7 - Manual Control State Diagram

Description				State				
Input Controls				Freerun	Normal (PRI)	Normal (SEC)	Holdover (PRI)	Holdover (SEC)
LOS2	LOS1	GTi	RST	S0	S1	S2	S1H	S2H
1	1	X	0 to 1	-	S0	S0	S0	S0
X	0	0	1	S1	-	S1 MTIE	S1	S1 MTIE
X	0	1	1	S1	-	S1 MTIE	S1 MTIE	S1 MTIE
0	1	0	1	S1	S1H	-	-	S2 MTIE
0	1	1	1	S2	S2 MTIE	-	S2 MTIE	S2 MTIE
1	1	X	1	-	S1H	S2H	-	-

Legend:
 - No Change
 MTIE State change occurs with TIE Corrector Circuit
 Refer to Automatic Control State Diagram for state changes to and from Auto-Holdover State

Table 5 - Automatic Control (MS1=MS2=1, RSEL=0) State Table

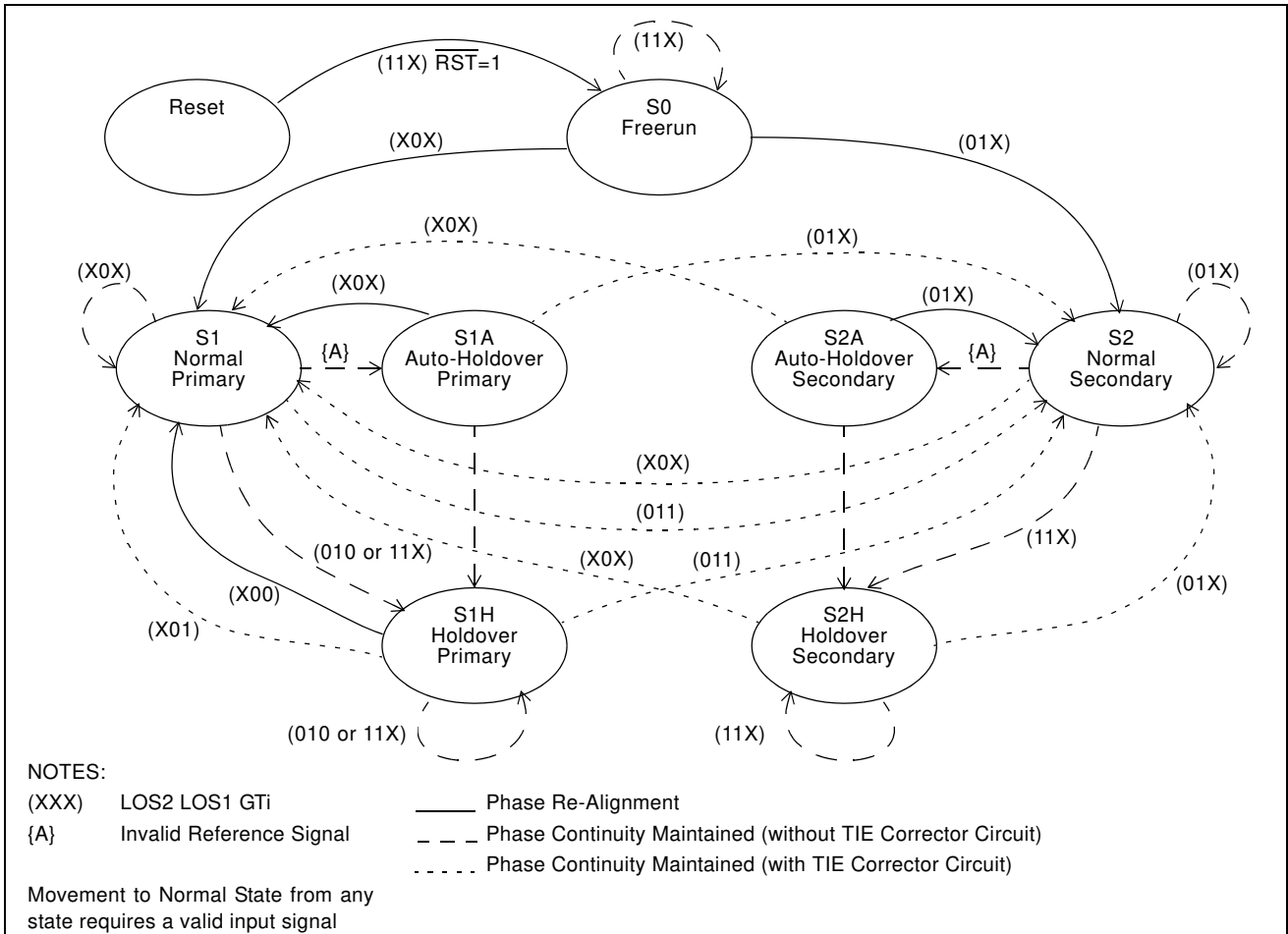


Figure 8 - Automatic Control State Diagram

MT9044 Measures of Performance

The following are some synchronizer performance indicators and their corresponding definitions.

Intrinsic Jitter

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various bandlimiting filters depending on the applicable standards.

Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the MT9044, two internal elements determine the jitter attenuation. This includes the internal 1.9 Hz low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to 5 ns/125 us. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5 ns/125 us.

The MT9044 has thirteen outputs with three possible input frequencies for a total of 39 possible jitter transfer functions. However, the data sheet section on AC Electrical Characteristics - Jitter Transfer specifies transfer values for only three cases, 8 kHz to 8 kHz, 1.544 MHz to 1.544 MHz and 2.048 MHz to 2.048 MHz. Since all outputs are derived from the same signal, these transfer values apply to all outputs.

It should be noted that 1 UI at 1.544 MHz is 644 ns, which is not equal to 1 UI at 2.048 MHz, which is 488 ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

What is the T1 and E1 output jitter when the T1 input jitter is 20 UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18 dB?

$$\begin{aligned}
 \text{OutputT1} &= \text{InputT1} \times 10^{\left(\frac{-A}{20}\right)} \\
 \text{OutputT1} &= 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5 \text{UI}(T1) \\
 \text{OutputE1} &= \text{OutputT1} \times \frac{(1 \text{UIT1})}{(1 \text{UIE1})} \\
 \text{OutputE1} &= \text{OutputT1} \times \frac{(644 \text{ns})}{(488 \text{ns})} = 3.3 \text{UI}(T1)
 \end{aligned}$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the three jitter transfer functions provided.

Note that the resulting jitter transfer functions for all combinations of inputs (8 kHz, 1.544 MHz, 2.048 MHz) and outputs (8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the MT9044, the Freerun accuracy is equal to the Master Clock (OSCi) accuracy.

Holdover Accuracy

Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the MT9044, the storage value is determined while the device is in Normal Mode and locked to an external reference signal.

The absolute Master Clock (OSCi) accuracy of the MT9044 does not affect Holdover accuracy, but the change in OSCi accuracy while in Holdover Mode does.

Capture Range

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The MT9044 capture range is equal to ± 230 ppm minus the accuracy of the master clock (OSCi). For example, a ± 32 ppm master clock results in a capture range of ± 198 ppm.

Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the MT9044.

Phase Slope

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

$$MTIE(S) = TIE_{max}(t) - TIE_{min}(t)$$

Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a reference switch or a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

In the case of the MT9044, the output signal phase continuity is maintained to within ± 5 ns at the instance (over one frame) of all reference switches and all mode changes. The total phase shift, depending on the switch or type of mode change, may accumulate up to ± 200 ns over many frames. The rate of change of the ± 200 ns phase shift is limited to a maximum phase slope of approximately 5 ns/125 μ s. This meets the maximum phase slope requirement of Bellcore GR-1244-CORE (81 ns/1.326 ms).

Phase Lock Time

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

- i) initial input to output phase difference
- ii) initial input to output frequency difference
- iii) synchronizer loop filter
- iv) synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The MT9044 loop filter and limiter were optimized to meet the AT&T TR62411 jitter transfer and phase slope requirements. Consequently, phase lock time, which is not a standards requirement, may be longer than in other applications. See AC Electrical Characteristics - Performance for maximum phase lock time.

MT9044 and Network Specifications

The MT9044 fully meets all applicable PLL requirements (intrinsic jitter/wander, jitter/wander tolerance, jitter/wander transfer, frequency accuracy, frequency holdover accuracy, capture range, phase change slope and MTIE during reference rearrangement) for the following specifications.

1. Bellcore GR-1244-CORE June 1995 for Stratum 3, Stratum 4 Enhanced and Stratum 4
2. AT&T TR62411 (DS1) December 1990 for Stratum 3, Stratum 4 Enhanced and Stratum 4
3. ANSI T1.101 (DS1) February 1994 for Stratum 3, Stratum 4 Enhanced and Stratum 4
4. ETSI 300 011 (E1) April 1992 for Single Access and Multi Access
5. TBR 4 November 1995
6. TBR 12 December 1993
7. TBR 13 January 1996
8. ITU-T I.431 March 1993
9. ITU-T G.813 August 1996 for Option1 clocks for 2048 kbit/s interfaces
10. ITU-T G.812 June 1998 for type IV clocks for 1,544 kbit/s interfaces and 2,048 kbit/s interfaces

Applications

This section contains MT9044 application specific details for clock and crystal operation, guard time usage, reset operation, power supply decoupling, Manual Control operation and Automatic Control operation.

Master Clock

The MT9044 can use either a clock or crystal as the master timing source.

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the OSCi pin. For applications not requiring an accurate Freerun Mode, tolerance of the master timing source may be ± 100 ppm. For applications requiring an accurate Freerun Mode, such as Bellcore GR-1244-CORE, the tolerance of the master timing source must be no greater than ± 32 ppm.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the MT9044 will always equal ± 230 ppm. For example, if the master timing source is ± 100 ppm, then the capture range will be ± 130 ppm.

Clock Oscillator - when selecting a Clock Oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle. See AC Electrical Characteristics.

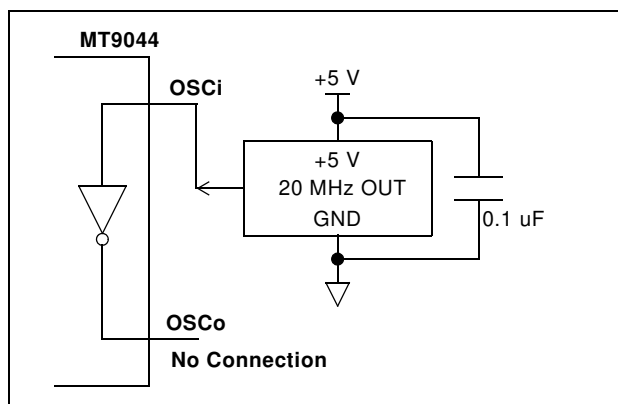


Figure 9 - Clock Oscillator Circuit

For applications requiring ± 32 ppm clock accuracy, the following clock oscillator module may be used.

CTS CXO-65-HG-5-C-20.0 MHz

Frequency: 20 MHz

Tolerance: 25 ppm 0C to 70C

Rise & Fall Time: 8 ns (0.5 V 4.5 V 50 pF)

Duty Cycle: 45% to 55%

The output clock should be connected directly (not AC coupled) to the OSCi input of the MT9044, and the OSCo output should be left open as shown in Figure 9.

Crystal Oscillator - Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 10.

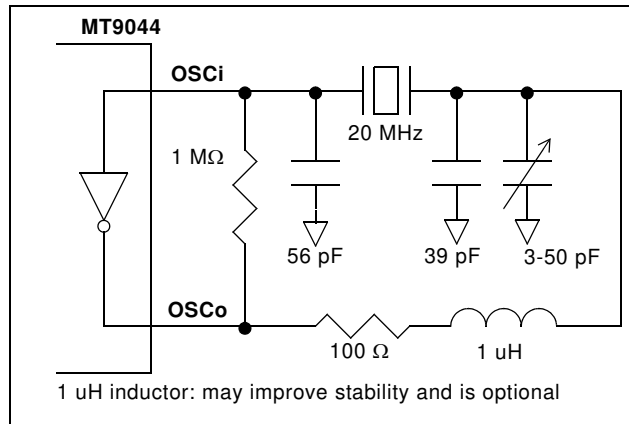


Figure 10 - Crystal Oscillator Circuit

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances, and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The trimmer capacitor shown in Figure 10 may be used to compensate for capacitive effects. If accuracy is not a concern, then the trimmer may be removed, the 39 pF capacitor may be increased to 56 pF, and a wider tolerance crystal may be substituted.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows.

<i>Frequency:</i>	<i>20 MHz</i>
<i>Tolerance:</i>	<i>As required</i>
<i>Oscillation Mode:</i>	<i>Fundamental</i>
<i>Resonance Mode:</i>	<i>Parallel</i>
<i>Load Capacitance:</i>	<i>32 pF</i>
<i>Maximum Series Resistance:</i>	<i>35 Ω</i>
<i>Approximate Drive Level:</i>	<i>1 mW</i>
<i>e.g., CTS R1027-2BB-20.0 MHz</i>	
<i>(±20 ppm absolute, ±6 ppm 0C to 50C, 32 pF, 25 Ω)</i>	

Guard Time Adjustment

Excessive switching of the timing reference (from PRI to SEC) in the MT9044 can be minimized by first entering Holdover Mode for a predetermined maximum time (i.e., guard time). If the degraded signal returns to normal before the expiry of the guard time (e.g., 2.5 seconds), then the MT9044 is returned to its Normal Mode (with no reference switch taking place). Otherwise, the reference input may be changed from Primary to Secondary.

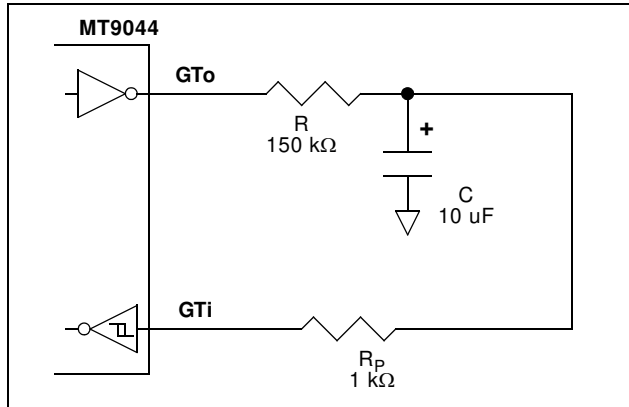


Figure 11 - Symmetrical Guard Time Circuit

A simple way to control the guard time (using Automatic Control) is with an RC circuit as shown in Figure 11. Resistor R_P is for protection only and limits the current flowing into the GTi pin during power down conditions. The guard time can be calculated as follows.

$$guard_{time} = RC \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{SIH}}\right)$$

$$guard_{time} \approx RC \times 0.6$$

example

$$guard_{time} \approx 150k \times 10u \times 0.6 = 1.45s$$

- V_{SIH} is the logic high going threshold level for the GTi Schmitt Trigger input, see DC Electrical Characteristics

In cases where fast toggling might be expected of the LOS1 input, then an unsymmetrical Guard Time Circuit is recommended. This ensures that reference switching doesn't occur until the full guard time value has expired. An unsymmetrical Guard Time Circuit is shown in Figure 12.

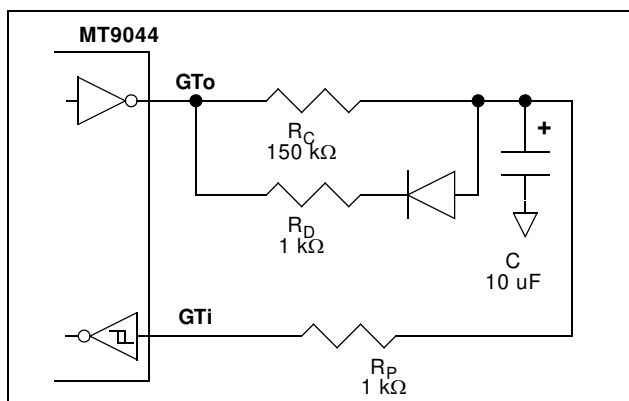


Figure 12 - Unsymmetrical Guard Time Circuit

Figure 13 shows a typical timing example of an unsymmetrical Guard Time Circuit with the MT9044 in Automatic Control.

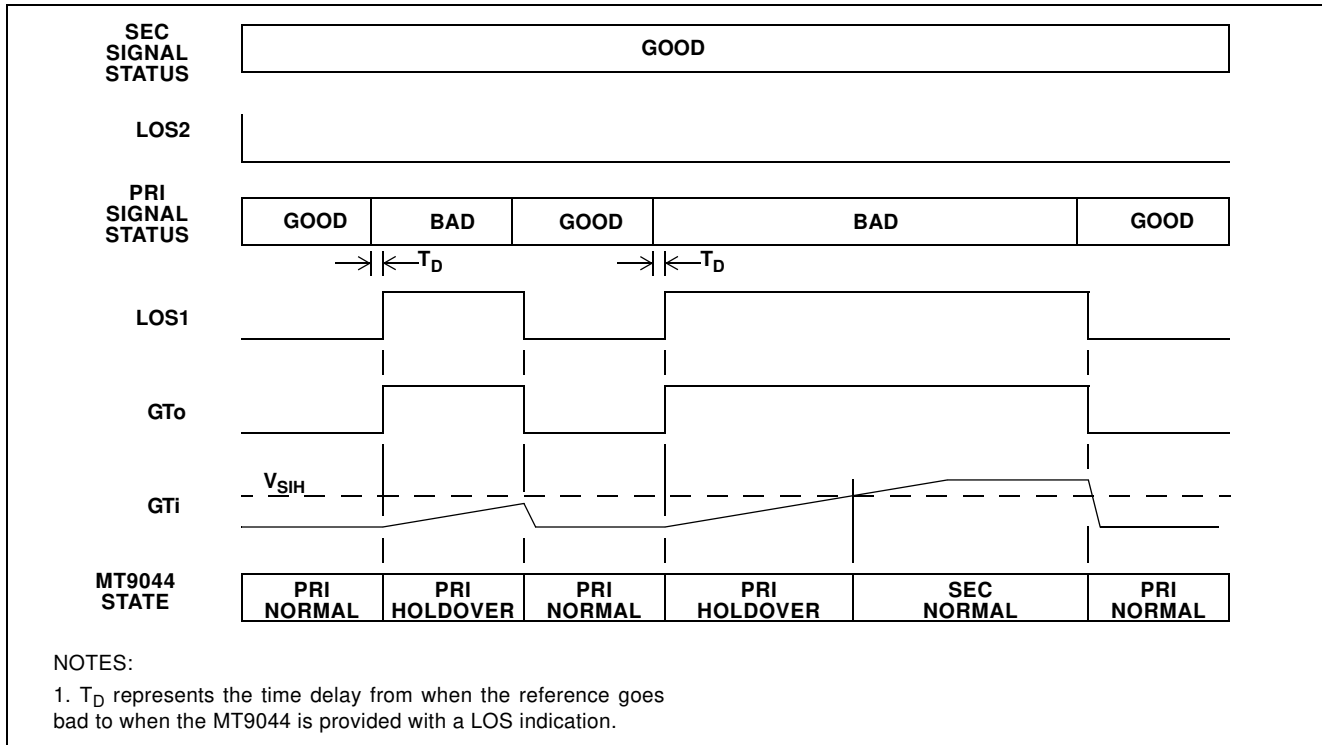


Figure 13 - Automatic Control, Unsymmetrical Guard Time Circuit Timing Example

TIE Correction (using GTi)

When Primary Holdover Mode is entered for short time periods, TIE correction should not be enabled. This will prevent unwanted accumulated phase change between the input and output. This is mainly applicable to Manual Control, since Automatic Control together with the Guard Time Circuit inherently operate in this manner.

For instance, 10 Normal to Holdover to Normal mode change sequences occur, and in each case Holdover was entered for 2s. Each mode change sequence could account for a phase change as large as 350 ns. Thus, the accumulated phase change could be as large as 3.5 us, and, the overall MTIE could be as large as 3.5 us.

$$Phase_{hold} = 0.05ppm \times 2s = 100ns$$

$$Phase_{state} = 50ns + 200ns = 250ns$$

$$Phase_{10} = 10 \times (250ns + 100ns) = 3.5us$$

- 0.05 ppm is the accuracy of Holdover Mode
- 50 ns is the maximum phase continuity of the MT9044 from Normal Mode to Holdover Mode
- 200 ns is the maximum phase continuity of the MT9044 from Holdover Mode to Normal Mode (with or without TIE Corrector Circuit)

When 10 Normal to Holdover to Normal mode change sequences occur without MTIE enabled, and in each case holdover was entered for 2s, each mode change sequence could still account for a phase change as large as 350 ns. However, there would be no accumulated phase change, since the input to output phase is re-aligned after every Holdover to Normal state change. The overall MTIE would only be 350 ns.

Reset Circuit

A simple power up reset circuit with about a 50 μ s reset low time is shown in Figure 14. Resistor R_P is for protection only and limits current into the \overline{RST} pin during power down conditions. The reset low time is not critical but should be greater than 300 ns.

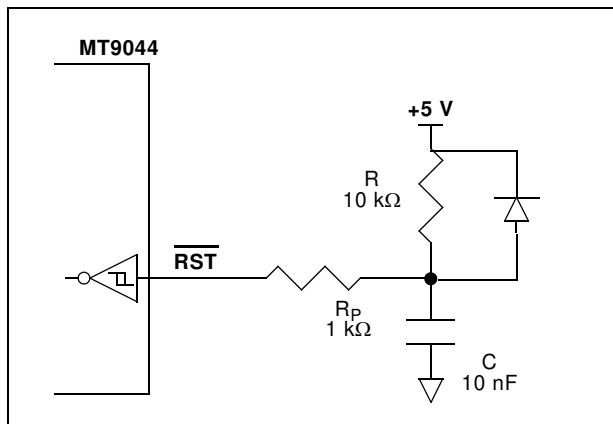


Figure 14 - Power-Up Reset Circuit

Dual T1 Reference Sources with MT9044 in Automatic Control

For systems requiring simple state machine control, the application circuit shown in Figure 15 using Automatic Control may be used.

In this circuit, the MT9044 is operating Automatically, using a Guard Time Circuit, and the LOS1 and LOS2 inputs to determine all mode changes. Since the Guard Time Circuit is set to about 1s, all line interruptions ($LOS1=1$) less than 1s will cause the MT9044 to go from Primary Normal Mode to Holdover Mode and not switch references. For line interruptions greater than 1s, the MT9044 will switch Modes from Holdover to Secondary Normal, provided that the secondary signal is valid ($LOS2=0$). After receiving a good primary signal ($LOS1=0$), the MT9044 will switch back to Primary Normal Mode. For complete Automatic Control state machine details, refer to Table 5 for the State Table, and Figure 8 for the State Diagram.

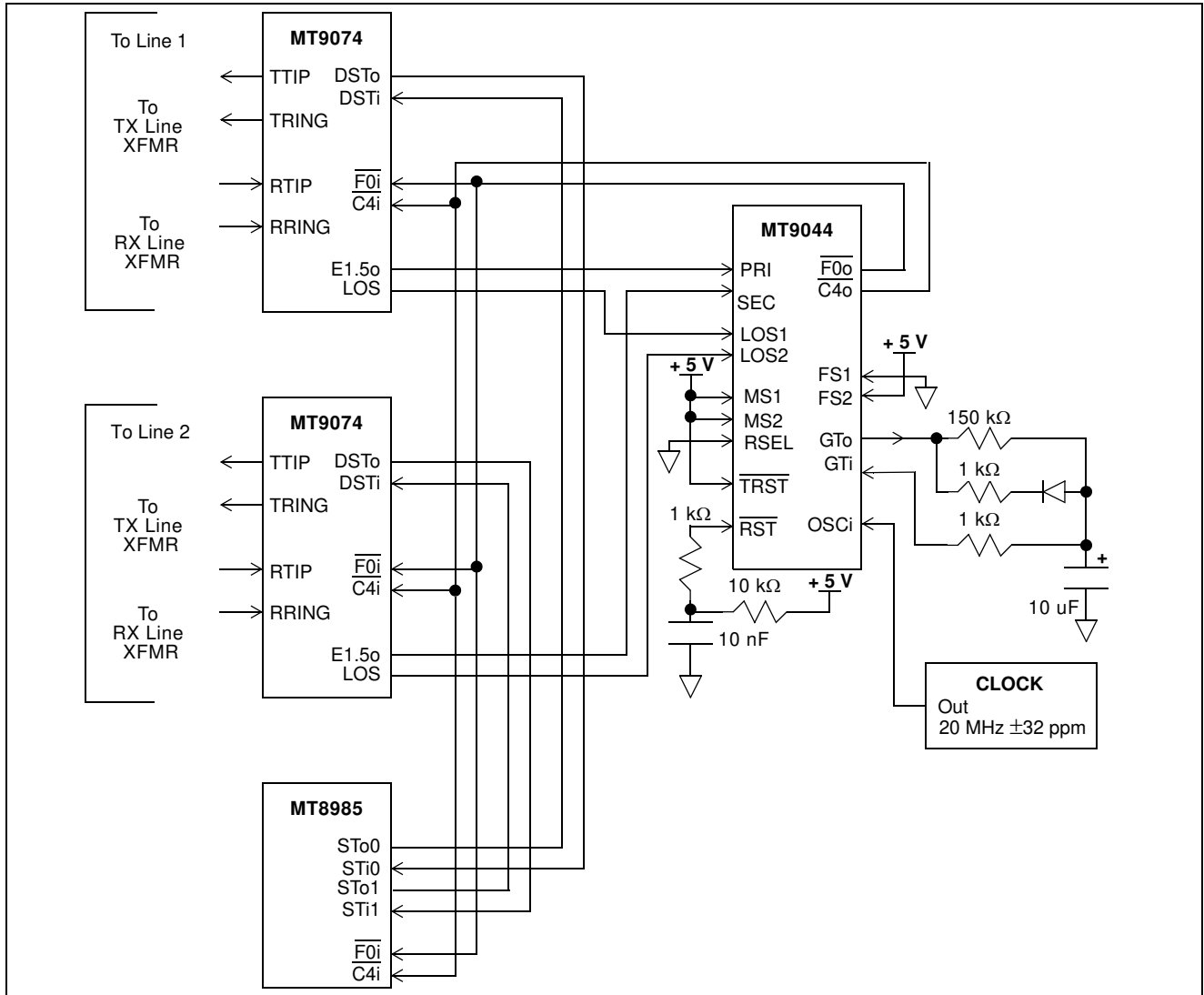


Figure 15 - Dual T1 Reference Sources with MT9044 in 1.544 MHz Automatic Control

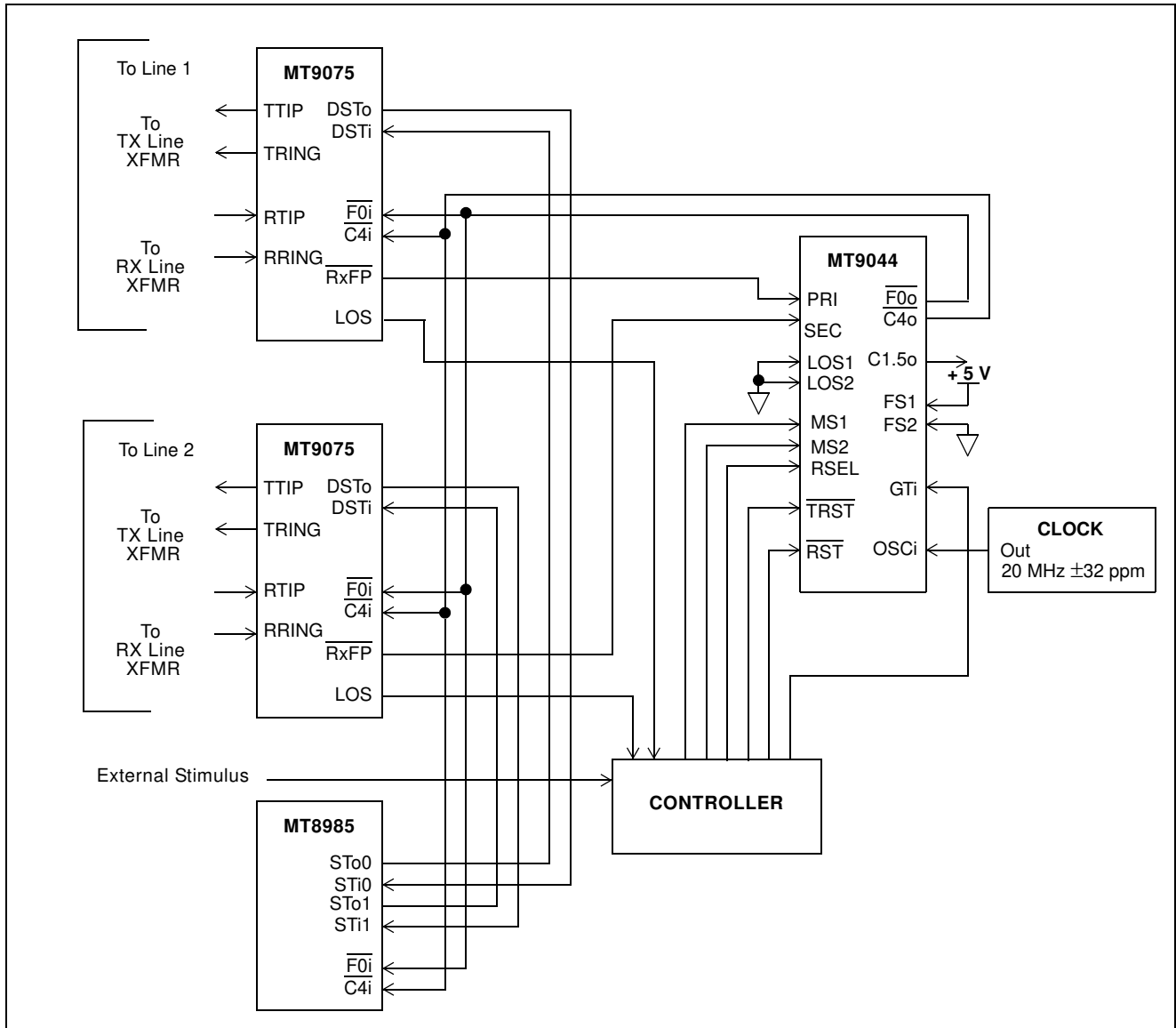


Figure 16 - Dual E1 Reference Sources with MT9044 in 8 kHz Manual Control

Dual E1 Reference Sources with MT9044 in Manual Control

For systems requiring complex state machine control, the application circuit shown in Figure 16 using Manual Control may be used.

In this circuit, the MT9044 is operating Manually and is using a controller for all mode changes. The controller sets the MT9044 modes (Normal, Holdover or Freerun) by controlling the MT9044 mode/control select pins (MS2 and MS1). The input (Primary or Secondary) is selected with the reference select pin (RSEL). TIE correction from Primary Holdover Mode to Primary Normal Mode is enabled and disabled with the guard time input pin (GTi). The input to output phase alignment is re-aligned with the TIE circuit reset pin (\overline{TCLR}), and a complete device reset is done with the \overline{RST} pin.

The controller uses two stimulus inputs (LOS) directly from the MT9075 E1 interfaces, as well as an external stimulus input. The external input may come from a device that monitors the status registers of the E1 interfaces, and outputs a logic one in the event of an unacceptable status condition.